National Semiconductor

ADVANCE INFORMATION

DS90C032
LVDS Quad CMOS Differential Line Receiver

General Description

The DS90C032 is a quad CMOS differential line receiver designed for applications requiring ultra low power dissipation and high data rates. The device is designed to support data rates in excess of 65 MHz utilizing Low Voltage Differential Signaling (LVDS) technology.

The DS90C032 accepts low voltage (330 mV) differential input signals and translates them to CMOS (TTL compatible) output levels. The receiver supports a TRI-STATE® function that may be used to multiplex outputs.

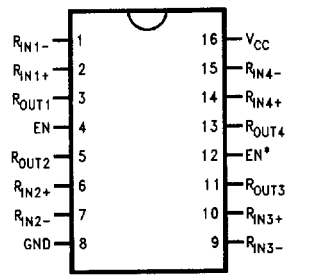
The DS90C032 and companion line driver (DS90C031) provide a new alternative to high power psuedo-ECL devices for high speed point to point interfaces.

Features

- >65 MHz Switching Rates
- Accepts small swing (330 mV) differential signal levels
- Ultra Low Power Dissipation
- 500 ps Maximum Differential Skew
- 3.5 ns Maximum Chip to Chip Skew
- Industrial Operating Temperature Range
- Available in Surface Mount Packaging (SOIC)
- Pin Compatible with DS26C32A, MB570 and 41LF
- Compatible with IEEE P1596.3 SCI LVDS draft standard

Connection Diagram

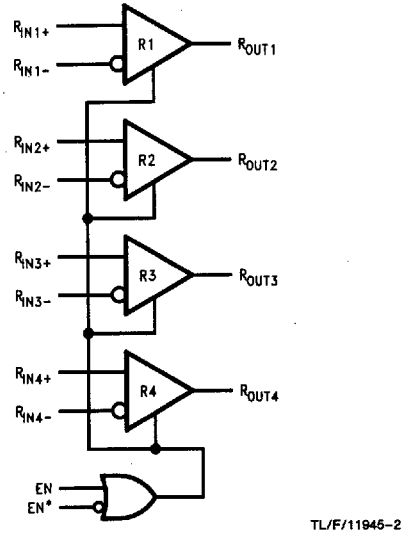
Dual-In-Line



TL/F/11945–1

Order Number
DS90C032M or DS90C032N
See NS Package Number
M16A or N16E

Functional Diagram and Truth Tables



TL/F/11945–2

RECEIVER

ENABLES		INPUTS	OUTPUT
EN	EN*	$R_{IN+} - R_{IN-}$	R_{OUT}
L	H	X	Z
All other combinations of ENABLE inputs		$V_{ID} \geq 0.1V$	H
		$V_{ID} \leq -0.1V$	L

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3V to +6V
Input Voltage (RIN+, RIN−)	−0.3V to (V_{CC} +0.3V)
Enable Input Voltage (EN, EN*)	−0.3V to (V_{CC} +0.3V)
Output Voltage (ROUT)	−0.3V to (V_{CC} +0.3V)
Short Circuit Duration (ROUT)	continuous
Maximum Package Power Dissipation @ +25°C	
M Package	TBDW
N Package	TBDW
Derate M Package	TBD mW/°C above +25°C
Derate N Package	TBD mW/°C above +25°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range Soldering (4 sec.)	+260°C
Maximum Junction Temperature	+150°C

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	+4.5	+5.0	5.5	V
Receiver Input Voltage	GND		2.4	V
Operating Free Air Temperature (T_A)	−40	25	+85	°C

Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified (Note 2).

Symbol	Parameter	Conditions		Pin	Min	Typ	Max	Units
V_{TH}	Differential Input High Threshold	V_{CM} = +1.2V		RIN+, RIN−		+TBD	+100	mV
V_{TL}	Differential Input Low Threshold				−100	−TBD		mV
I_{IN}	Input Current	V_{IN} = +2.4V	V_{CC} = 5.5V			TBD	±10	μA
		V_{IN} = 0V				TBD	±10	μA
V_{OH}	Output High Voltage	I_{OH} = −0.4 mA, V_{ID} = +200 mV		ROUT	3.8	TBD		V
		I_{OH} = −0.4 mA, Input terminated			3.8	TBD		V
V_{OL}	Output Low Voltage	I_{OL} = 2 mA, V_{ID} = −200 mV				TBD	0.3	V
I_{OS}	Output Short Circuit Current	Enabled, V_{OUT} = 0V			TBD	TBD	TBD	mA
I_{OZ}	Output TRI-STATE Current	Disabled, V_{OUT} = 0V or V_{CC}				TBD	±10	μA
V_{IH}	Input High Voltage			EN, EN*	2.0			V
V_{IL}	Input Low Voltage						0.8	V
I_I	Input Current						±10	μA
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA					−1.5	V
I_{CC}	No Load Supply Current	EN, EN* = V_{CC} or GND, Inputs Open		V_{CC}		10	15	mA
	Receivers Enabled	EN, EN* = 2.4 or 0.5, Inputs Open				12	17	mA
I_{CCZ}	No Load Supply Current Receivers Disabled	EN = GND, EN* = V_{CC} Inputs Open				TBD	TBD	mA

Switching Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHLD}	Differential Propagation Delay High to Low	C_L = 5 pF, V_{ID} = 200 mV	1.5	3	5	ns
t_{PLHD}	Differential Propagation Delay Low to High	*Figures 1, 2* (Note 4)	1.5	3	5	ns
t_{SKD}	Differential Skew $\lvert t_{PHLD} - t_{PLHD} \rvert$		0	100	500	ps
t_{SK1}	Channel to Channel Skew			TBD	TBD	ns
t_{SK2}	Chip to Chip Skew	(Note 5)		TBD	3.5	ns
t_{TLH}	Rise Time	*Figures 1, 2*		1.6	2.5	ns
t_{THL}	Fall Time			1.6	2.5	ns
t_{PHZ}	Disable Time High to Z			TBD	TBD	ns
t_{PLZ}	Disable Time Low to Z			TBD	TBD	ns
t_{PZH}	Enable Time Z to High			TBD	TBD	ns
t_{PZL}	Enable Time Z to Low			TBD	TBD	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

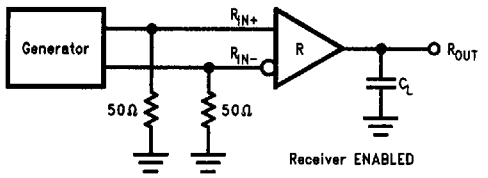
Note 2: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified.

Note 3: All typicals are given for: V_{CC} = +5.0V, T_A = +25°C.

Note 4: AC input test waveforms for test purposes: $t_r = t_f$ = 1 ns (0-100%), V_{ID} = 200 mV.

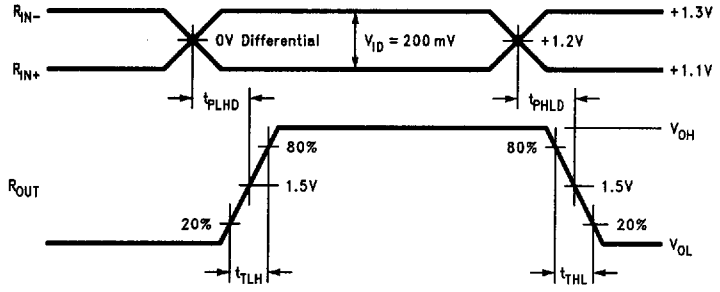
Note 5: Chip to Chip Skew is defined as the difference between the minimum and maximum specified differential propagation delays.

Parameter Measurement Information



TL/F/11945–3

FIGURE 1. Receiver Propagation Delay and Transition Time Test Circuit



TL/F/11945–4

FIGURE 2. Receiver Propagation Delay and Transition Time Waveforms