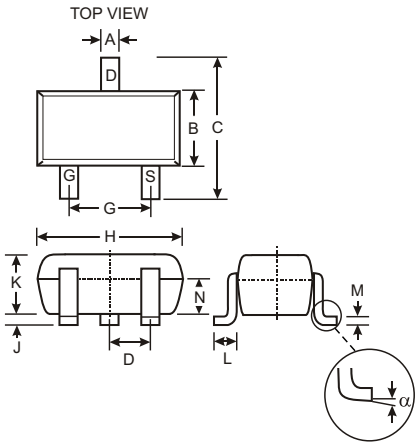
2N7002T

N-CHANNEL ENHANCEMENT MODE FIELD EFFECT TRANSISTOR

NEW PRODUCT

Features

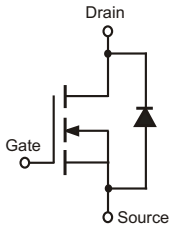
- Low On-Resistance
- Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- Ultra-Small Surface Mount Package
- **Lead Free/RoHS Compliant (Note 2)**
- **Qualified to AEC-Q101 Standards for High Reliability**



SOT-523			
Dim	**Min**	**Max**	**Typ**
A	0.15	0.30	0.22
B	0.75	0.85	0.80
C	1.45	1.75	1.60
D			0.50
G	0.90	1.10	1.00
H	1.50	1.70	1.60
J	0.00	0.10	0.05
K	0.60	0.80	0.75
L	0.10	0.30	0.22
M	0.10	0.20	0.12
N	0.45	0.65	0.50
	0	8	
All Dimensions in mm			

Mechanical Data

- Case: SOT-523
- Case Material: Molded Plastic. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020C
- Terminals: Solderable per MIL-STD-202, Method 208
- Lead Free Plating (Matte Tin Finish annealed over Alloy 42 leadframe).
- Terminal Connections: See Diagram
- Marking: 72 (See Page 3)
- Ordering & Date Code Information, See Page 3
- Weight: 0.002 grams (approximate)



Maximum Ratings @ T_A = 25°C unless otherwise specified

Characteristic		Symbol	Value	Units
Drain-Source Voltage		V_{DSS}	60	V
Drain-Gate Voltage R_{GS} 1.0M		V_{DGR}	60	V
Gate-Source Voltage	Continuous Pulsed	V_{GSS}	±20 ±40	V
Drain Current (Note 1)	Continuous Continuous @ 100°C Pulsed	I_D	115 73 800	mA
Total Power Dissipation (Note 1)		P_d	150	mW
Thermal Resistance, Junction to Ambient		R_{JA}	833	°C/W
Operating and Storage Temperature Range		T_j, T_{STG}	-55 to +150	°C

Note: 1. Device mounted on FR-5 PCB 1.0 x 0.75 x 0.062 inch pad layout as shown on Diodes, Inc. suggested pad layout AP02001, which can be found on our website at http://www.diodes.com/datasheets/ap02001.pdf.
2. No purposefully added lead.

NEW PRODUCT

Electrical Chacteristics

@ T_A = 25 C unless otherwise specified

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 3)						
Drain-Source Breakdown Voltage	BV_{DSS}	60			V	V_{GS} = 0V, I_D = 10 A
Zero Gate Voltage Drain Current @ T_C = 25°C @ T_C = 125°C	I_{DSS}			1.0 500	µA	V_{DS} = 60V, V_{GS} = 0V
Gate-Body Leakage	I_{GSS}			±10	nA	V_{GS} = ±20V, V_{DS} = 0V
ON CHARACTERISTICS (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	1.0		2.0	V	V_{DS} = V_{GS}, I_D = 250 A
Static Drain-Source On-Resistance @ T_j = 25°C @ T_j = 125°C	$R_{DS\ (ON)}$		2.0 4.4	7.5 13.5		V_{GS} = 5.0V, I_D = 0.05A V_{GS} = 10V, I_D = 0.5A
On-State Drain Current	$I_{D(ON)}$	0.5	1.0		A	V_{GS} = 10V, V_{DS} = 7.5V
Forward Transconductance	g_{FS}	80			mS	V_{DS} =10V, I_D = 0.2A
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{iss}		22	50	pF	V_{DS} = 25V, V_{GS} = 0V f = 1.0MHz
Output Capacitance	C_{oss}		11	25	pF	
Reverse Transfer Capacitance	C_{rss}		2.0	5.0	pF	
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	$t_{D(ON)}$		7.0	20	ns	V_{DD} = 30V, I_D = 0.2A, R_L = 150 , V_{GEN} = 10V, R_{GEN} = 25
Turn-Off Delay Time	$t_{D(OFF)}$		11	20	ns	

Note: 3. Short duration test pulse used to minimize self-heating effect.

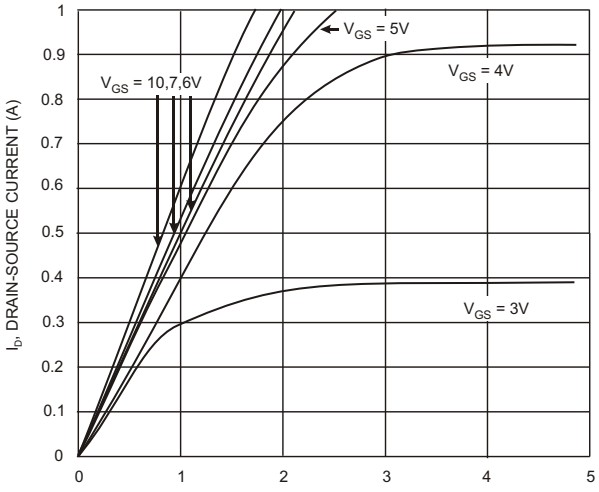


Fig. 1 On-Region Characteristics

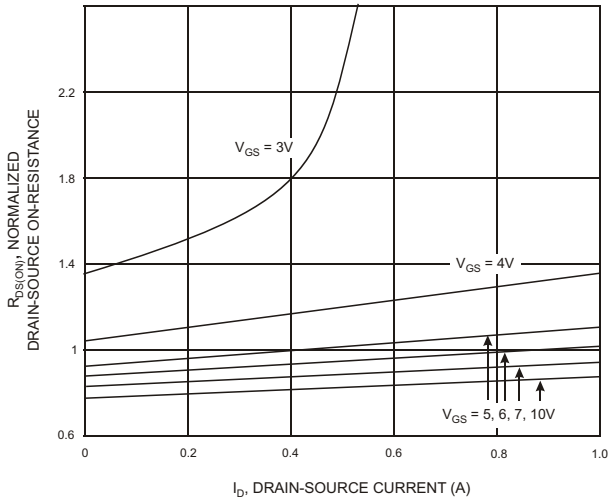


Fig. 2 On-Resistance Variation with Gate Voltage and Drain-Source Current

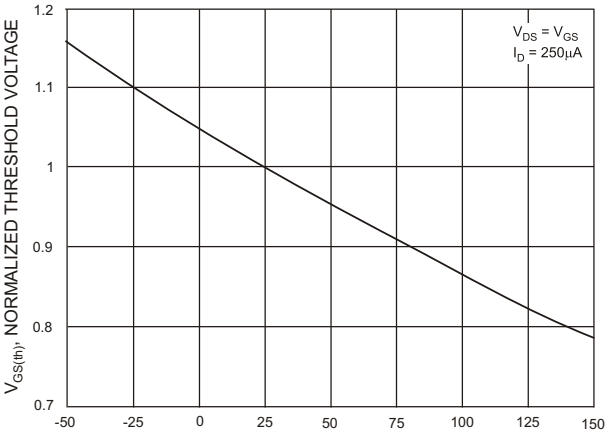


Fig. 3 Gate Threshold Variation with Temperature

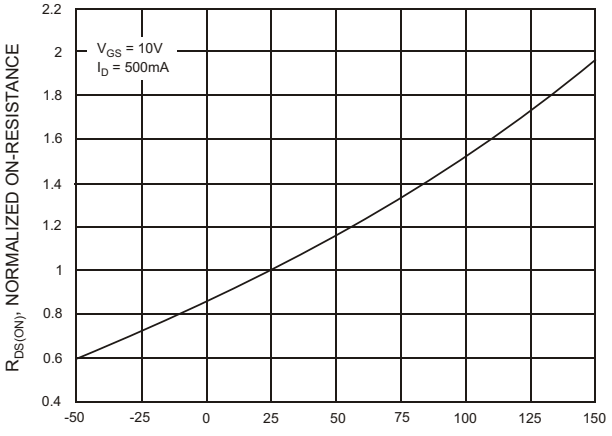


Fig. 4 On-Resistance Variation with Temperature

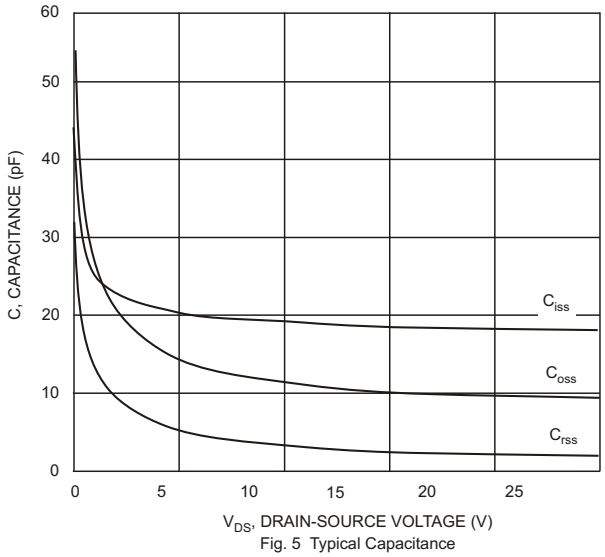


Fig. 5 Typical Capacitance

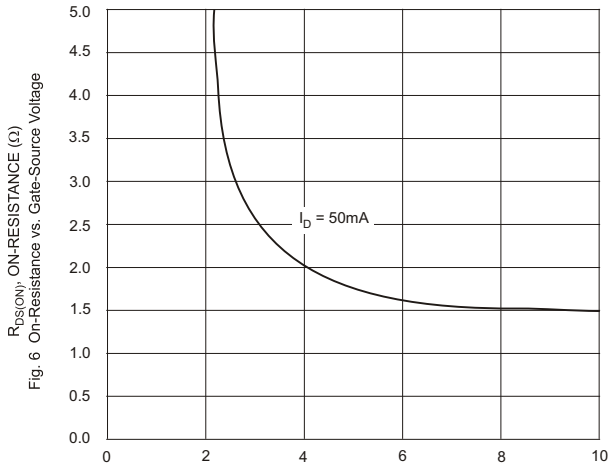


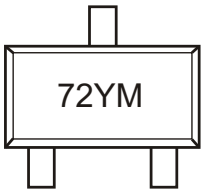
Fig. 6 On-Resistance vs. Gate-Source Voltage

Ordering Information (Note 4)

Device	Packaging	Shipping
2N7002T-7-F	SOT-523	3000/Tape & Reel

Notes: 4. For Packaging Details, go to our website at http://www.diodes.com/datasheets/ap02007.pdf.

Marking Information



72 = Product Type Marking Code
YM = Date Code Marking
Y = Year (ex: N = 2002)
M = Month (ex: 9 = September)

Date Code Key

Year	2002	2003	2004	2005	2006	2007	2008	2009
Code	N	P	R	S	T	U	V	W

Month	Jan	Feb	March	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

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