# 8 Megabit Module — XM28C080S — 1 Meg x 8

## 5 Volt, Byte Alterable E²PROM SIP Module

### FEATURES

- High Density 8 Megabit SIP Module
- Industrial Standard 36 PIN SRAM SIP Pinout
- Low Power CMOS Technology
  - —Active – Less Than 60mA
  - —Standby – Less Than 4mA
- Fully Decoded Addresses
- Access Time of 180ns
- Fast Write Cycle Times
- Standard 256 Byte Page
  - —User Configurable to 512, 1024 or 2048 Bytes
- Software Data Protection
- MultiPlane™ Memory Architecture
  - —Concurrent Read Write™

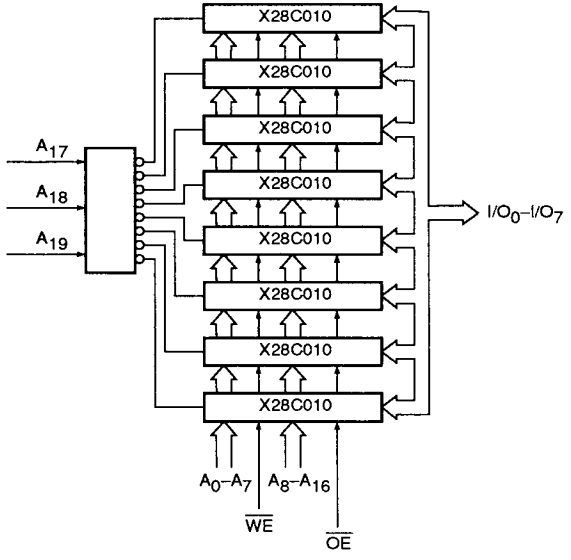
### DESCRIPTION

The XM28C080S is a high density 8 Megabit E²PROM module comprised of eight X28C010 128K x 8 E²PROMs mounted on a FR-4 substrate. The XM28C080S is configured 1 Meg x 8 and is fully decoded. The module is a 36 Pin SIP conforming to the industry standard SRAM pinouts.

The individual memory components are Xicor's X28C010 1 Megabit E²PROMs, featuring the highly reliable Direct Write™ memory cell. All components are fully tested prior to assembly and then the completed module is 100% electrically tested.

The MultiPlane™ memory architecture allows reading of the module while a write operation is currently underway.

### FUNCTIONAL DIAGRAM




3877 FHD F08

6

Direct Write and MultiPlane are trademarks of Xicor, Inc.

## PIN DESCRIPTIONS

### Address ($A_0$–$A_{19}$)

The address inputs selects 8-bit memory location during a read or write operation.

### Chip Enable ($\overline{CE}$)

A LOW on the $\overline{CE}$ input enables read or write operations.

### Output Enable ($\overline{OE}$)

The output enable input is active LOW and when asserted turns on the output buffers of the selected memory component.

### Write Enable ($\overline{WE}$)

The write enable input controls the writing of data to the XM28C080S. Addresses are latched on the high to low transition of $\overline{WE}$ and data is latched on the low to high edge of $\overline{WE}$.

### Input/Output ($I/O_0$–$I/O_7$)

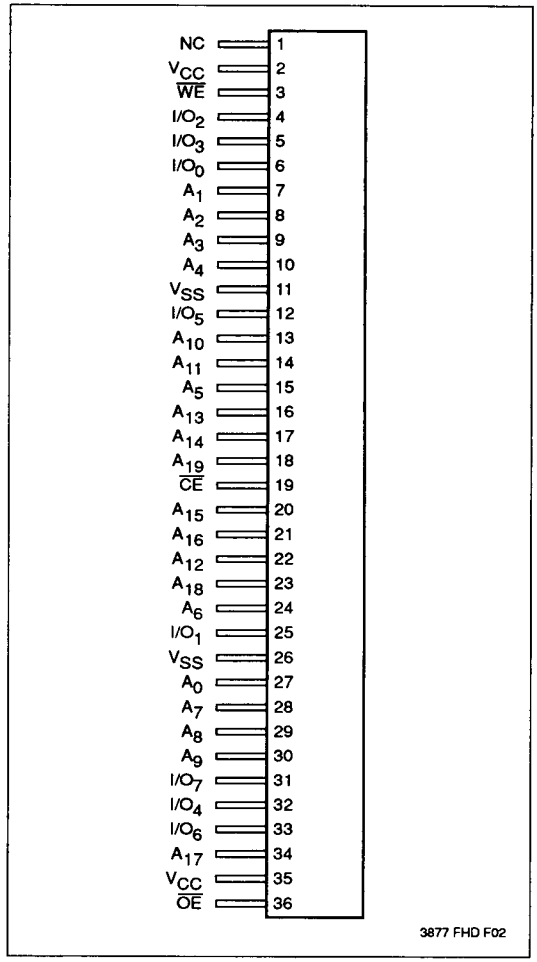
Data is read from or written to the XM28C080S through the I/O pins.

## PIN NAMES

| Symbol | Description |
|---|---|
| $\overline{OE}$ | Output Enable |
| $\overline{CE}$ | Chip Enable |
| $\overline{WE}$ | Write Enable |
| $I/O_0$–$I/O_7$ | Data Input/Output |
| $A_0$–$A_{19}$ | Addresses Inputs |
| $V_{CC}$ | +5V |
| $V_{SS}$ | Ground |

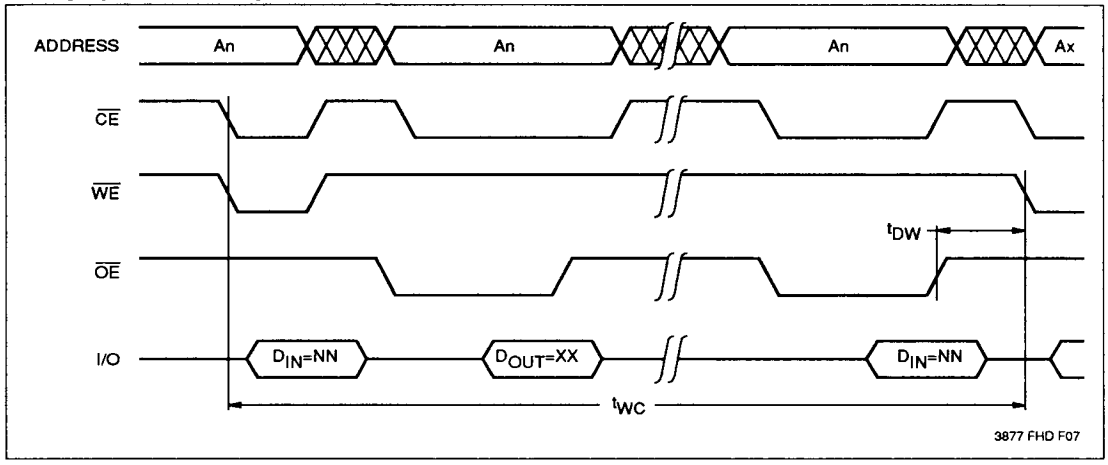
3877 PGM T01

## PIN CONFIGURATION




3877 FHD F02

**Polling Operation Timing**




## DEVICE OPERATION

### Read

Read operations are initiated when both $\overline{OE}$ and $\overline{CE}$ are LOW. Data will be output from the memory location pointed to by the address inputs. The data bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ inputs are HIGH.

### Write

Write operations are initiated when both $\overline{WE}$ and $\overline{CE}$ are LOW and $\overline{OE}$ is HIGH. The module supports both a $\overline{WE}$ and a $\overline{CE}$ controlled write operation. That is, the address latched by the falling edge of either $\overline{WE}$ or $\overline{CE}$, whichever occurs last. The data is latched by the rising edge of either $\overline{WE}$ or $\overline{CE}$, whichever occurs first. A write operation, once initiated, will continue to completion within 10ms.

### Page Write Operation

A page write operation provides for the system a means for writing from two to two-hundred fifty-six bytes sequentially. A page write, no matter how many bytes written, will take no longer than 10ms to complete.

### Polling Operations

E²PROM memories can be written quickly in the write page mode. However, once the data is latched into the memory, the internal write operation can take up to 10ms. The typical write cycle is somewhat less than 10ms and the host system can take advantage of the shorter write cycle time by polling the memory. Polling is performed by the host reading the *last* location written. When the read data compares true with the data written, the internal cycle is complete and the memory is ready for normal read or write operations to resume. Refer to the timing diagram above.

### Software Data Protection (SDP)

The memory components on the module support SDP. SDP, when enabled by the host system, will protect the memory contents from inadvertent writes during the power-up and power-down cycles.

### Setting SDP

The host system must write a three byte command sequence to the module **for each memory component to be protected**. Once SDP is set, the memory will ignore all standard attempts to alter its contents. The host can still write the memory but must first reissue the three byte command sequence immediately followed by the byte or page write operation.

### Resetting SDP

In the event the user needs to reset SDP for testing, they may issue a six byte command sequence. After $t_{WC}$ the memory component will be returned to the standard operating mode. **This operation must be repeated for each component being reset.**

The modules are shipped from Xicor with SDP reset; that is, the module will be in the standard operating mode. If the user decides not to employ the SDP, it is recommended they provide external inadvertent write protection circuitry.

**TABLE 1. SOFTWARE DATA PROTECTION SEQUENCE**

| Step | Operation | $A_0$–$A_{16}$ | Data Pattern | Comments |
|---|---|---|---|---|
| 1 | Write | 15555 | AA | $A_{17}$, $A_{18}$, and $A_{19}$ must be the same for the entire command sequence and any subsequent write operation. |
| 2 | Write | 0AAAA | 55 | |
| 3 | Write | 15555 | A0 | |
| 4 | Write | XXXXX | XX | Optional write operation (byte or page) after opening access. |

3877 PGM T02

***Note:*** *Step 4 is optional. The system may exit the routine after step 3 and the device will enter a write cycle and set the nonvolatile SDP bit. This is a nonvolatile write operation and will take a maximum 10ms to complete. If the system enters step 4 (within $t_{BLC}$) it may write from 1 to 256 bytes to the device addressed by the command sequence.*

**TABLE 2. RESET SOFTWARE DATA PROTECTION SEQUENCE**

| Step | Operation | $A_0$–$A_{16}$ | Data Pattern | Comments |
|---|---|---|---|---|
| 1 | Write | 15555 | AA | $A_{17}$, $A_{18}$, and $A_{19}$ must be the same for the entire command sequence. |
| 2 | Write | 0AAAA | 55 | |
| 3 | Write | 15555 | 80 | |
| 4 | Write | 15555 | AA | |
| 5 | Write | 0AAAA | 55 | |
| 6 | Write | 15555 | 20 | After $t_{WC}$, the selected component will return to the unprotected state. |

3877 PGM T03

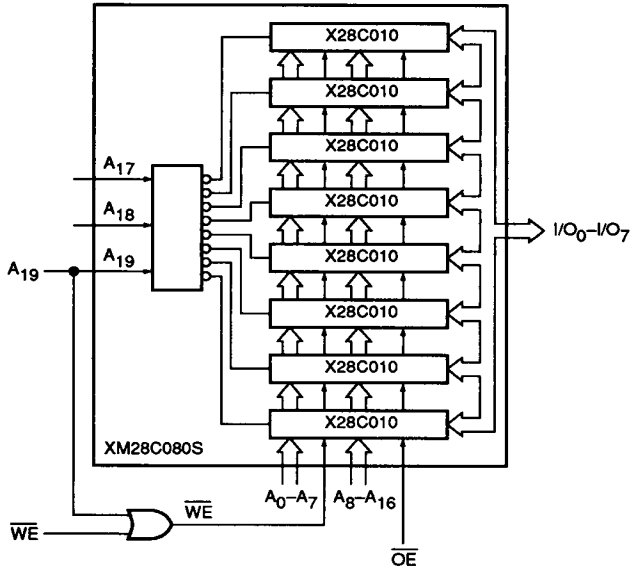
### MultiPlane Architecture

The design of the XM28C080S has implemented a multiplane architecture. That is, there are eight independent 128K x 8 memory spaces or planes, each selected by its own chip enable input via the on-board decoder chip. This architecture can be utilized in a number of ways.

### Separate Data and Program Memory Spaces

The multiplane concept allows the system to write to one plane of the module and still be able to read (continue executing code) from the module, utilizing any plane not performing a write operation.

This concept of separated data and program spaces can be expanded by providing a simple off-module circuit that will disable writes to predetermined portions of memory. A very basic version is shown in the Functional Diagram. Whenever $A_{19}$ is high, the $\overline{WE}$ input is forced high, write protecting one half the module. This half would be reserved for read only program store while the other half would be available for read and write data store.




3877 FHD F01

### Expanded Sequential Page Lengths

A standard system implementation would be decoding externally the module's chip enable and then wiring each address of the module to its corresponding address line in the system. This would effectively provide the system a memory organized as eight separate memory planes with a sequential page address space of 256 bytes.

In an application such as data logging, the most efficient method of logging the data is in a sequential manner. If the data come in bursts that exceed 256 bytes in length a longer page might be desirable. By swapping address lines externally the effective page length can be expanded to 2048 bytes. Refer to Table 3 for matrix illustrating the various page length options.

**TABLE 3. ADDRESS TRANSLATION MATRIX**

| | Module Address Inputs | | | | | Page Size | Effective No. of Planes |
|---|---|---|---|---|---|---|---|
| | $A_0$–$A_7$ | $A_8$–$A_{16}$ | $A_{17}$ | $A_{18}$ | $A_{19}$ | | |
| System Address Lines | $A_0$–$A_7$ | $A_8$–$A_{16}$ | $A_{17}$ | $A_{18}$ | $A_{19}$ | 256 | 8 |
| | $A_0$–$A_7$ | $A_9$–$A_{17}$ | $A_8$ | $A_{18}$ | $A_{19}$ | 512 | 4 |
| | $A_0$–$A_7$ | $A_{10}$–$A_{18}$ | $A_8$ | $A_9$ | $A_{19}$ | 1024 | 2 |
| | $A_0$–$A_7$ | $A_{11}$–$A_{19}$ | $A_8$ | $A_9$ | $A_{10}$ | 2048 | 1 |

3877 PGM T04

***Note:*** *The user should be aware the overall $I_{CC}$ of the module will increase as more individual components on the module are activated. Refer to $I_{CC}$ Active, MultiMode on Page 2.*

**ABSOLUTE MAXIMUM RATINGS***

Temperature Under Bias .....–10°C to +85°C
Storage Temperature .....–55°C to +125°C
Voltage on any Pin with
Respect to Ground .....–0.5V to +6.0V
D.C. Output Current .....5 mA

***COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**RECOMMENDED OPERATING CONDITIONS**

| Temperature | Min. | Max. |
|---|---|---|
| Commercial | 0°C | 70°C |

3877 PGM T05

| Supply Voltage | Limits |
|---|---|
| XM28C080S | 5V ± 10% |

3877 PGM T06

**D.C. OPERATING CHARACTERISTICS** (Over recommended operating conditions unless otherwise specified.)

| Symbol | Parameter | Limits | | Units | Test Conditions |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| $I_{CC}$ | $V_{CC}$ Current (Active) | | 60 | mA | $\overline{CE}$ = $\overline{OE}$ = $V_{IL}$, $\overline{WE}$ = $V_{IH}$, All I/Os = Open, one memory active, all other memories on standby |
| $I_{CC}$ | $V_{CC}$ Current (Active) MultiMode | | 55 + (50 x n) | mA | $\overline{CE}$ = $\overline{OE}$ = $V_{IL}$, $\overline{WE}$ = $V_{IH}$, All I/Os = Open, n memories active (either being read or in write cycle), all other memories standby |
| $I_{SB}$ | $V_{CC}$ Current (Standby) | | 5 | mA | $\overline{CE}$ = $V_{CC}$ – 0.3V, All I/Os = Open, All Other Inputs = Don't Care |
| $I_{LI}$ | Input Leakage Current | | 10 | µA | $V_{IN}$ = GND to $V_{CC}$ |
| $I_{LO}$ | Output Leakage Current | | 10 | µA | $V_{OUT}$ = GND to $V_{CC}$, $\overline{CE}$ = $V_{IH}$ |
| $V_{IL}$ | Input Low Voltage | | 0.8 | V | |
| $V_{IH}$ | Input High Voltage | 2.0 | | V | |
| $V_{OL}$ | Output Low Voltage | | 0.4 | V | $I_{OL}$ = 2.1mA |
| $V_{OH}$ | Output High Voltage | 2.4 | | V | $I_{OH}$ = –400mA |

3877 PGM T07

**POWER-UP TIMING**

| Symbol | Parameter | Max. | Units |
|---|---|---|---|
| $t_{PUR}$ | Power-up to Read Delay | 100 | µs |
| $t_{PUW}$ | Power-up to Write Delay | 5 | ms |

3877 PGM T08

**CAPACITANCE** $T_A$ = 25°C, f = 1 MHz, $V_{CC}$ = 5V

| Symbol | Parameter | Max. | Units | Test Conditions |
|---|---|---|---|---|
| $C_{I/O}$(1) | Input/Output Capacitance | 80 | pF | $V_{I/O}$ = 0V |
| $C_{IN}$(1) | Input Capacitance | 48 | pF | $V_{IN}$ = 0V |

3877 PGM T09

**Note:** (1) These parameters are periodically sampled and not 100% tested.

**A.C. CONDITIONS OF TEST**

| | |
|---|---|
| Input Pulse Levels | 0V to 3.0V |
| Input Rise and Fall Times | 10 ns |
| Input and Output Timing Reference Levels | 1.5V |

3877 PGM T10

**MODE SELECTION**

| $\overline{CE}$ | $\overline{OE}$ | $\overline{WE}$ | Mode | I/O | Power |
|---|---|---|---|---|---|
| L | L | H | Read | $D_{OUT}$ | Active |
| L | H | L | Write | $D_{IN}$ | Active |
| H | X | X | Standby and Write Inhibit | High Z | Standby |
| X | L | X | Write Inhibit | — | — |
| X | X | H | Write Inhibit | — | — |

3877 PGM T11

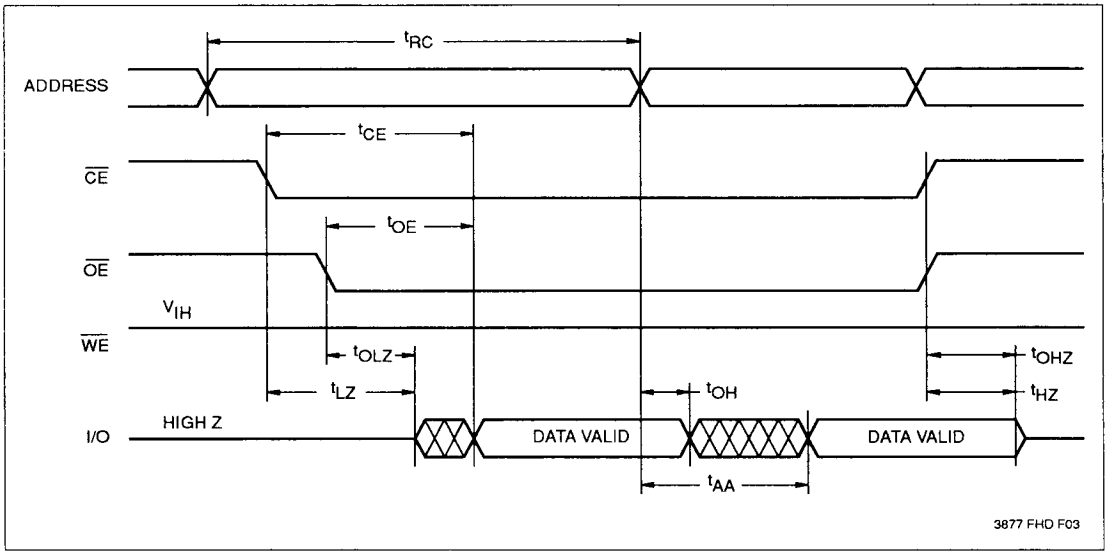
**A.C. CHARACTERISTICS** (Over the recommended operating conditions unless otherwise specified.)

**Read Cycle Limits**

| Symbol | Parameter | XM28C080S-18 | | XM28C080S-25 | | Units |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| $t_{RC}$ | Read Cycle Time | 180 | | 250 | | ns |
| $t_{CE}$ | $\overline{CE}$ Access Time | | 180 | | 250 | ns |
| $t_{AA}$ | Address Access Time | | 180 | | 250 | ns |
| $t_{OE}$ | $\overline{OE}$ Access Time | | 65 | | 65 | ns |
| $t_{LZ}$ | $\overline{CE}$ LOW to Active Output | 0 | | 0 | | ns |
| $t_{OLZ}$ | $\overline{OE}$ LOW to Active Output | 0 | | 0 | | ns |
| $t_{HZ}$ | $\overline{CE}$ HIGH to High Z Delay | | 65 | | 65 | ns |
| $t_{OHZ}$ | $\overline{OE}$ HIGH to High Z Delay | | 65 | | 65 | ns |
| $t_{OH}$ | Output Hold | 0 | | 0 | | ns |

3877 PGM T12

**Figure Title**

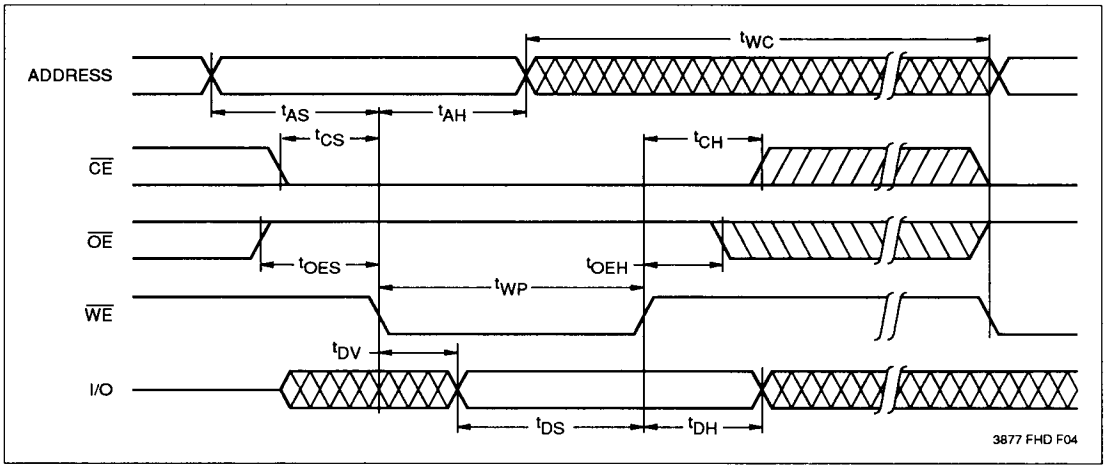


**Write Cycle Limits**

| Symbol | Parameter | Min. | Max. | Units |
|---|---|---|---|---|
| $t_{WC}$ | Write Cycle Time | | 10 | ms |
| $t_{AS}$ | Address Setup Time | 0 | | ns |
| $t_{AH}$ | Address Hold Time | 50 | | ns |
| $t_{CS}$ | Write Setup Time | 15 | | ns |
| $t_{CH}$ | Write Hold Time | 0 | | ns |
| $t_{CW}$ | Chip Enable Pulse Width | 100 | | ns |
| $t_{OES}$ | OE High Setup Time | 10 | | ns |
| $t_{OEH}$ | OE High Hold Time | 10 | | ns |
| $t_{WP}$ | WE Pulse Width | 100 | | ns |
| $t_{WPH}$ | WE High Recovery | 100 | | ns |
| $t_{DV}$ | Data Valid | | 1 | µs |
| $t_{DS}$ | Data Setup | 50 | | ns |
| $t_{DH}$ | Data Hold | 10 | | ns |
| $t_{DW}$ | Delay to Next Write | 1 | | µs |
| $t_{BLC}$ | Byte Load Cycle | 0.20 | 200 | µs |

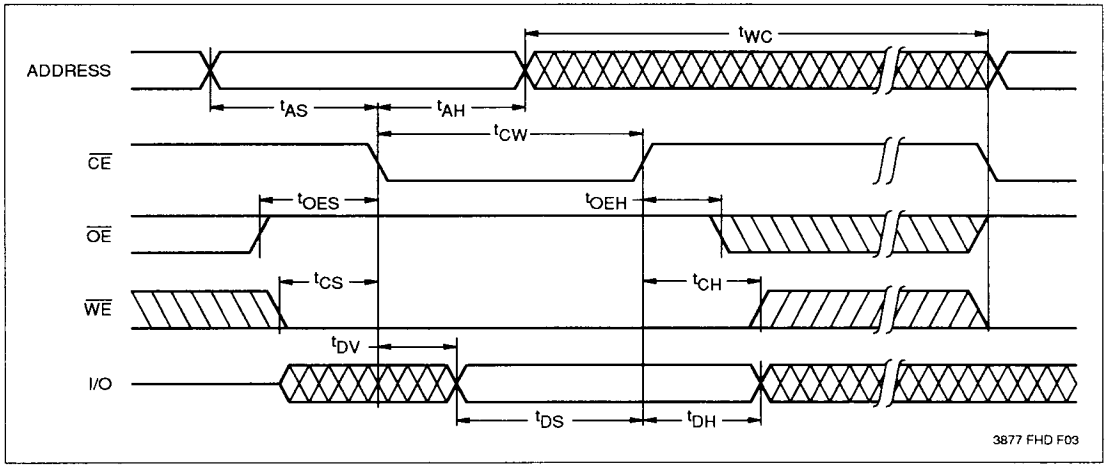
3877 PGM T13

**$\overline{WE}$ Controlled Write Cycle**

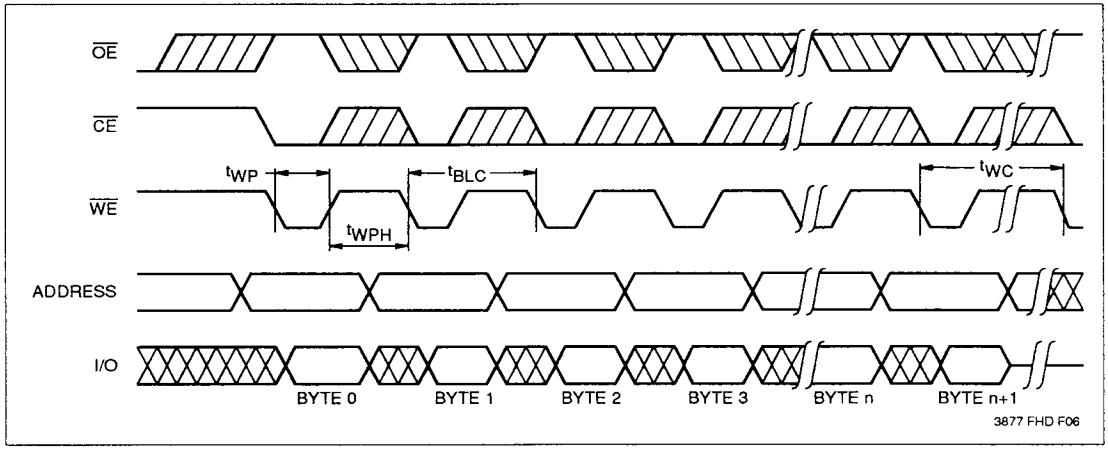



6

### $\overline{CE}$ Controlled Write Cycle




### Page Write Cycle



**SYMBOL TABLE**

| WAVEFORM | INPUTS | OUTPUTS |
|---|---|---|
|  | Must be steady | Will be steady |
|  | May change from Low to High | Will change from Low to High |
|  | May change from High to Low | Will change from High to Low |
|  | Don't Care: Changes Allowed | Changing: State Not Known |
|  | N/A | Center Line is High Impedance |