NEC

MOS INTEGRATED CIRCUIT
μPD4632312-X

32M-BIT CMOS MOBILE SPECIFIED RAM
2M-WORD BY 16-BIT
EXTENDED TEMPERATURE OPERATION

Description

The μPD4632312-X is a high speed, low power, 33,554,432 bits (2,097,152 words by 16 bits) CMOS mobile specified RAM featuring low power static RAM compatible function and pin configuration.

The μPD4632312-X is fabricated with advanced CMOS technology using one-transistor memory cell.

The μPD4632312-X is packed in 77-pin TAPE FBGA.

Features

- 2,097,152 words by 16 bits organization
- Fast access time: 85, 95, 105 ns (MAX.)
- Fast page access time: 35, 40, 45 ns (MAX.)
- Byte data control: /LB (I/O0 - I/O7), /UB (I/O8 - I/O15)
- Low voltage operation
  (B version: V_{CC} = 2.6 to 3.1 V,
  C version: V_{CC} = 2.3 to 2.7 V,
  BE version: V_{CC} = 2.6 to 3.1 V (Chip), $V_{CC}Q$ = 1.65 to 1.95 V (I/O),
  CE version: V_{CC} = 2.3 to 2.7 V (Chip), $V_{CC}Q$ = 1.65 to 1.95 V (I/O))
- Operating ambient temperature: T_A = –25 to +85 °C
- Output Enable input for easy application
- Chip Enable input: /CS pin
- Standby Mode input: MODE pin
- Standby Mode1: Normal standby (Memory cell data hold valid)
- Standby Mode2: Density of memory cell data hold is variable

Product name	Access time ns (MAX.)	Operating supply voltage V		Operating ambient temperature °C	Supply current					
					At operating mA (MAX.)	At standby μA (MAX.) Density of data hold				
		Chip	I/O			32M bits	16M bits	8M bits	4M bits	0M bit
μPD4632312-BxxX	80 Note	2.7 to 3.1	–	–25 to +85	35	100	70	60	50	10
	85	2.6 to 3.1								
μPD4632312-CxxX	95	2.3 to 2.7								
μPD4632312-BExxX	95	2.6 to 3.1	1.65 to 1.95							
μPD4632312-CExxX	105	2.3 to 2.7								

Note Under Development

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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

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The mark ★ shows major revised points.

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Ordering Information

Part number	Package	Access time ns (MAX.)	Operating supply voltage V		Operating temperature °C	Remark
			Chip	I/O		
μPD4632312F9-B85X-BT3	77-pin TAPE FBGA (12 x 7)	85	2.6 to 3.1	–	–25 to +85	B version
μPD4632312F9-C95X-BT3		95	2.3 to 2.7			C version
μPD4632312F9-BE95X-BT3		95	2.6 to 3.1	1.65 to 1.95		BE version
μPD4632312F9-CE10X-BT3		105	2.3 to 2.7			CE version

Pin Configuration

/xxx indicates active low signal.

77-pin TAPE FBGA (12 x 7)

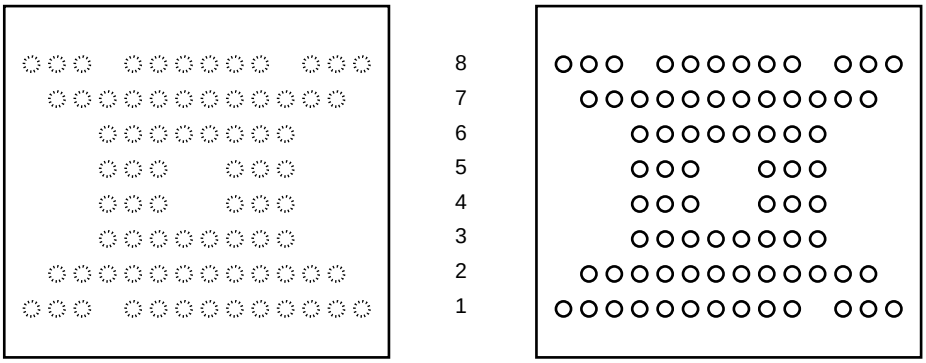
[μPD4632312F9-BxxX-BT3]

[μPD4632312F9-CxxX-BT3]

[μPD4632312F9-BExxX-BT3]

[μPD4632312F9-CExxX-BT3]

Top View **Bottom View**



Top View

	A	B	C	D	E	F	G	H	J	K	L	M	N	P
8	NC	NC	NC		A15	NC	NC	A16	NC	GND		NC	NC	NC
7		NC	NC	A11	A12	A13	A14	NC	I/O15	I/O7	I/O14	NC	NC	
6				A8	A19	A9	A10	I/O6	I/O13	I/O12	I/O5			
5				/WE	MODE	A20			I/O4	V_{CC}	$V_{CC}Q$			
4				NC	NC	NC			I/O3	NC	I/O11			
3				/LB	/UB	A18	A17	I/O1	I/O9	I/O10	I/O2			
2		NC	NC	A7	A6	A5	A4	GND	/OE	I/O0	I/O8	NC	NC	
1	NC	NC	NC		A3	A2	A1	A0	NC	/CS	NC	NC	NC	NC

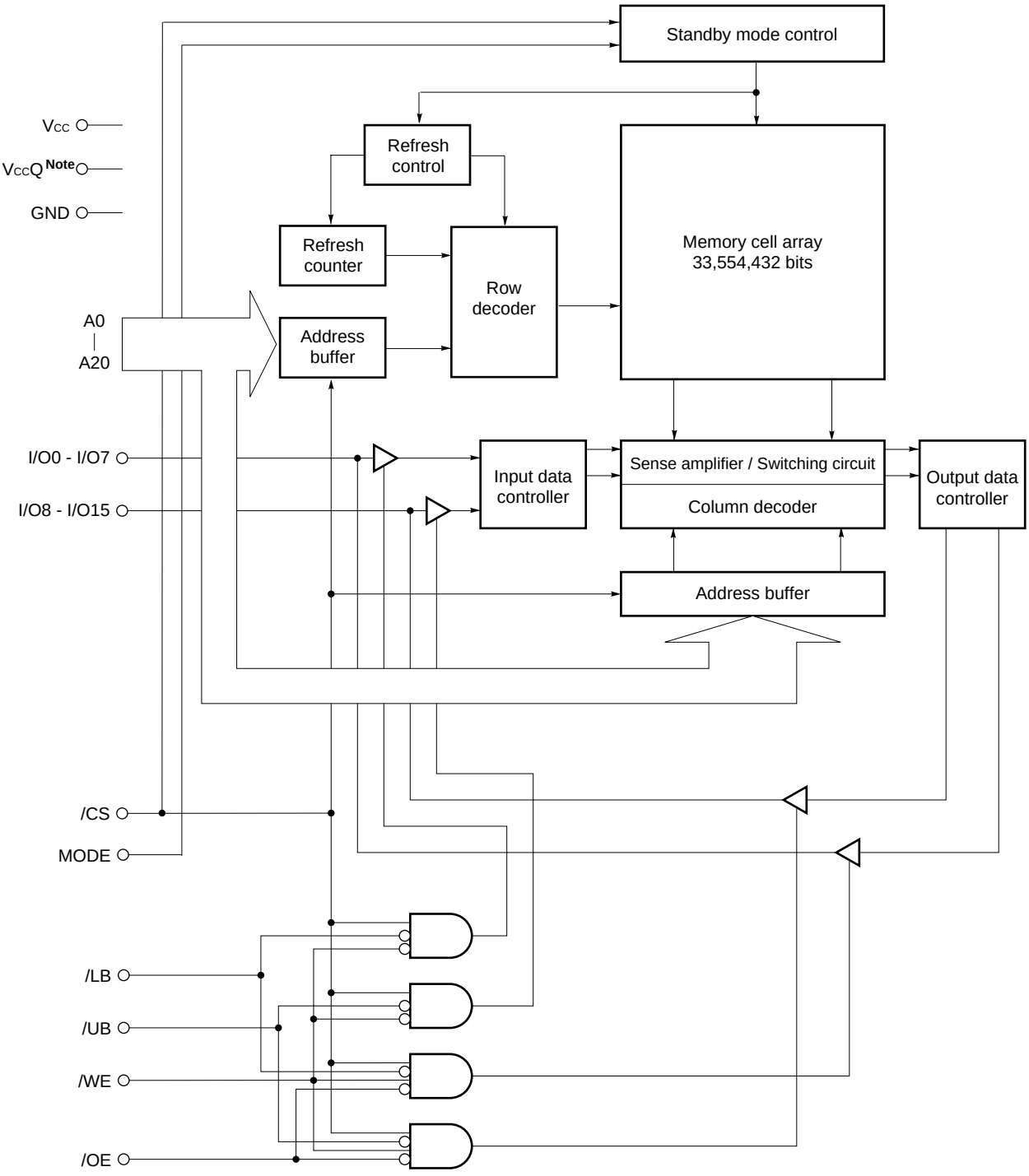
A0 - A20	: Address inputs	/LB, /UB	: Byte data select
I/O0 - I/O15	: Data inputs / outputs	V_{CC}	: Power supply
/CS	: Chip Select	$V_{CC}Q$ Note1	: Input / Output power supply
MODE	: Standby mode	GND	: Ground
/WE	: Write enable	NC Note2	: No Connection
/OE	: Output enable		

Notes 1. B, C version : NC

2. Some signals can be applied because this pin is not internally connected.

Remark Refer to **Package Drawing** for the index mark.

Block Diagram



★ **Note** BE, CE versions only.

Truth Table

/CS	MODE	/OE	/WE	/LB	/UB	Mode	I/O		Supply current
							I/O0 - I/O7	I/O8 - I/O15	
H	H	×	×	×	×	Not selected (Standby Mode 1)	High impedance	High impedance	I_{SB1}
★ H	L	×	×	×	×	Not selected (Standby Mode 2) Note1	High impedance	High impedance	I_{SB2}
L	H	H	H	×	×	Output disable	High impedance	High impedance	I_{CCA}
		L	H	L	L	Word read	D_{OUT}	D_{OUT}	
				L	H	Lower byte read	D_{OUT}	High impedance	
				H	L	Upper byte read	High impedance	D_{OUT}	
				H	H	Output disable	High impedance	High impedance	
		×	L	L	L	Word write	D_{IN}	D_{IN}	
				L	H	Lower byte write	D_{IN}	High impedance	
				H	L	Upper byte write	High impedance	D_{IN}	
				H	H	Write-abort Note2	High impedance	High impedance	

Caution MODE pin must be fixed to High except Standby Mode 2.

★ **Notes 1.** During normal operation, make /CS = V_{IH}, MODE = V_{IL}, the device enters the Standby Mode 2. However, make /CS = V_{IH} or V_{IL}, and MODE = V_{IL} at power application, the device enters the Standby Mode 2.

2. Write data can not be written to the memory cell.

Remark ×: V_{IH} or V_{IL}, H: V_{IH}, L: V_{IL},

CONTENTS

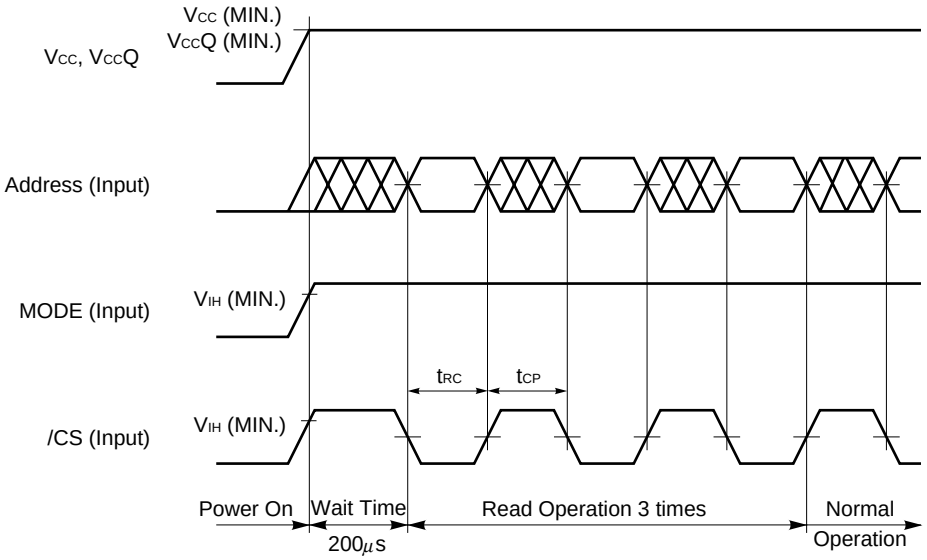
1. Initialization

The μPD4632312-X is initialized in the power-on sequence according to the following.

(1) To stabilize internal circuits, before turning on the power, a 200 μs or longer wait time must precede any signal toggling.

(2) After the wait time, read operation must be performed at least 3 times. After that, it can be normal operation.

Figure1-1. Initialization Timing Chart



Cautions 1. Following power application, make MODE and /CS high level during the wait time interval.

2. Following power application, make MODE high level during the wait time and three read operations.

3. The read operation must satisfy the specs described on page 17 (Read Cycle).

4. The address is don't care (V_{IH} or V_{IL}) during read operation.

5. Read operation must be executed with toggled the /CS pin.

6. To prevent bus contention, it is recommended to set /OE to high level.

7. Do not input data to the I/O pins if /OE is low level during a read operation.

2. Partial Refresh

2.1 Standby Mode

In addition to the regular standby mode (Standby Mode 1) with a 32M bits density, Standby Mode 2, which performs partial refresh, is also provided.

2.2 Density Switching

In Standby Mode 2, the densities that can be selected for performing refresh are 16M bits, 8M bits, 4M bits, and 0M bit.

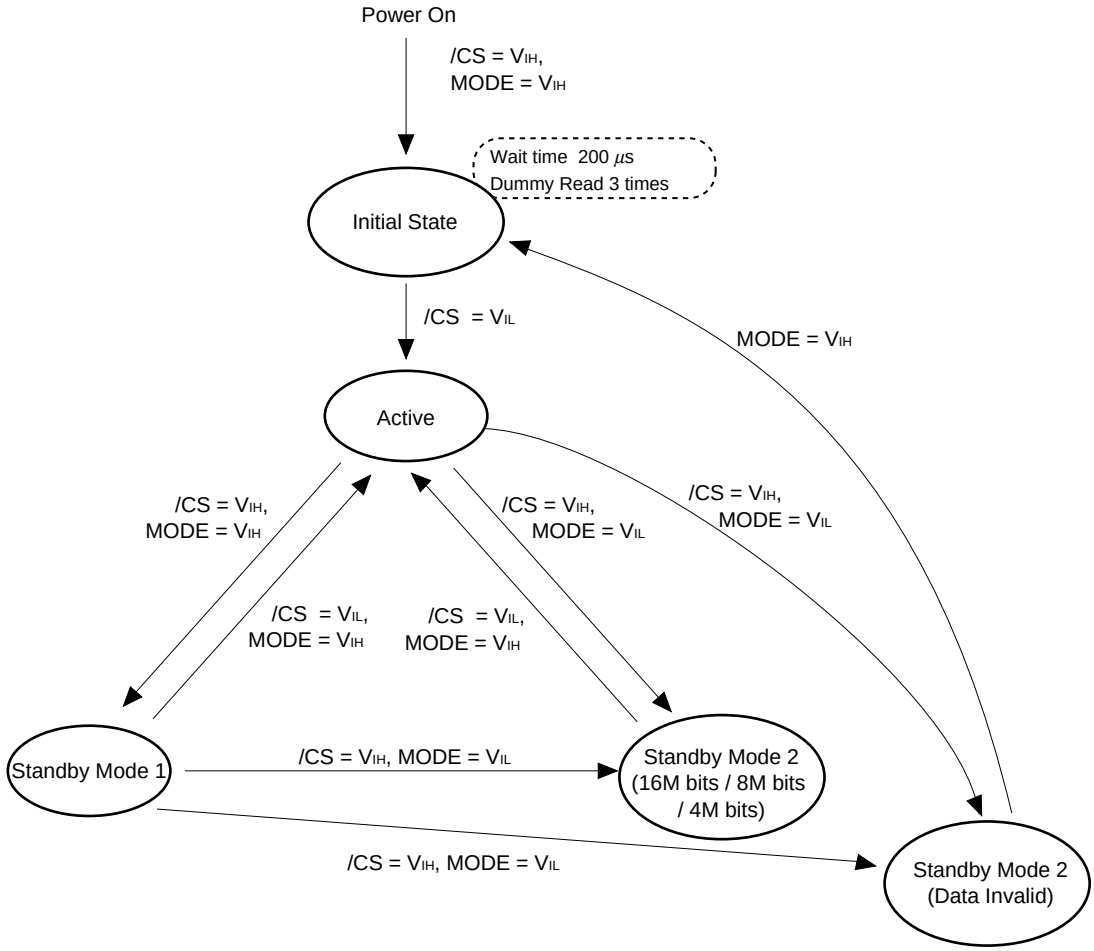
The density for performing refresh can be set with the mode register. (For how to perform mode register settings, refer to section **4. Mode Register Settings**.)

2.3 Standby Mode Status Transition

In Standby Mode 1, both /CS and MODE are high level, and in Standby Mode 2, /CS is high level and MODE is low level. In Standby Mode 2, if 0M bit is set as the density, it is necessary to perform initialization the same way as after applying power, in order to return to normal operation from Standby Mode 2. When the density has been set to 16M bits, 8M bits, or 4M bits in Standby Mode 2, it is not necessary to perform initialization to return to normal operation from Standby Mode 2.

For the timing charts, refer to **Figure 6-26. Standby Mode Timing Chart**, **Figure 6-27. Standby Mode 2 (Data Invalid) Entry / Recovery Timing Chart**.

Figure 2-1. Standby Mode State Machine



2.4 Addresses for Which Partial Refresh Is Supported

Data hold density	Correspondence address
16M bits	000000H to 0FFFFFH
8M bits	000000H to 07FFFFH
4M bits	000000H to 03FFFFH

3. Page Read Operation

3.1 Features of Page Read Operation

Features	4 Word Mode	8 Word Mode
Page length	4 words	8 words
Page read-corresponding addresses	A1, A0	A2, A1, A0
Page read start address	Don't care	(A2, A1, A0) = (V_{IL}, V_{IL}, V_{IL})
Page direction	Don't care	Sequential increment
Interrupt during page read operation	Enabled Note	Prohibited

Note An interrupt is output when /CS = H or in case A2 or a higher address changes.

3.2 Page Length

Four words and eight words are supported as the page lengths. The page length is set with the Mode register. Once the page length is set in the mode register, this setting is retained until it is set again.
(For how to perform mode register settings, refer to section **4. Mode Register Settings**.)

3.3 Page-Corresponding Addresses

The four-word page read-enabled addresses are A1 and A0. Fix addresses other than A1 and A0 during four -word page read. The eight-word page read-enabled addresses are A2, A1, and A0. Fix addresses other than A2, A1, and A0 during 8-word page read operation.

3.4 Page Start Address

Since random page read is supported for four-word pages, any address can be used as the page start address. Random page read is not supported for eight-word pages. Since the page read start addresses are only (A2, A1, A0) = (V_{IL}, V_{IL}, V_{IL}), it is not possible to start page read from any address other than (A2, A1, A0) = (V_{IL}, V_{IL}, V_{IL}).

3.5 Page Direction

Since random page read is possible for four-word pages, there is not restriction on the page direction.
Random page read is not supported for eight-word pages. The page direction in this case is sequential increment.

3.6 Interrupt during Page Read Operation

When generating an interrupt during four-word page read, either make /CS high level or change A2 and higher addresses. Generating an interrupt during eight-word read is prohibited.

3.7 Eight-Word Start Page Read Operation Prohibition

When an eight-word page read has been started, starting a page read with write-modify-read is prohibited. To start page read, do so from normal read.

Also, when an eight-word page read has been started, the /OE pin cannot be toggled.

For the timing chart, refer to **Figure 6-9. 8 Words Page Read Start after Write Modify Read Cycle Timing Chart**, **Figure 6-11. 8 Words 2 Continuous Read Cycles Timing Chart.**

3.8 Cautions for Eight-Word Page Read Operation

To perform normal read (A20 to A3: fixed) from normal read of (A2, A1, A0) = (V_{IL}, V_{IL}, V_{IL}) to (A2, A1, A0) = (V_{IL}, V_{IL}, V_{IH}) with the eight-word page set with the mode register, be sure to toggle /OE for normal read (A2, A1, A0) = (V_{IL}, V_{IL}, V_{IL}). At this time, observe the /OE to address setup time (t_{OAS}) and /OE pulse width (t_{OP}) standard value.

When /OE is fixed to low level with normal read (A20 to A3: fixed) from normal read of (A2, A1, A0) = (V_{IL}, V_{IL}, V_{IL}) to (A2, A1, A0) = (V_{IL}, V_{IL}, V_{IH}), eight-word page read starts.

Also, when performing a read operation to (A2, A1, A0) = (V_{IL}, V_{IL}, V_{IH}) (A20 to A3 are fixed) from when (A2, A1, A0) = (V_{IL}, V_{IL}, V_{IL}) are in a write-abort state (/WE = L, however, write data cannot be written to the memory cell because /LB, /UM = H), an 8-word page read operation is started.

For the timing chart, refer to **Figure 6-6. 8 Words Page Read Cycle Timing Chart**, **Figure 6-12. 8 Words Normal Read Cycle Timing Chart and Figure 6-13 8 Words Write-Abort to Read Cycle Timing Chart**.

4. Mode Register Settings

The page length and partial refresh density can be set using the mode register. Since the initial value of the mode register at power application is undefined, be sure to set the mode register after initialization at power application. When not using page read, set the mode register to random-accessible 4-word page read mode. When not using partial refresh, set the mode register to any value. Partial refresh mode will not be entered unless /CS = H, MODE = L, regardless of the register setting.

Once the page length and partial refresh density have been set in the mode register, these settings are retained until they are set again, while applying the power supply. However, the mode register setting will become undefined if the power is turned off, so set the mode register again after power application.

4.1 Mode Register Setting Method

The mode register setting mode can be entered by successively writing two specific data after two continuous reads of the highest address (1FFFFFH). The mode register setting is a continuous four-cycle operation (two read cycles and two write cycles).

Commands are written to the command register. The command register is used to latch the addresses and data required for executing commands, and it does not have an exclusive memory area.

For the timing chart and flow chart, refer to **Figure 6-24. Mode Register Setting Timing Chart**, **Figure 6-25. Mode Register Setting Flow Chart**.

Table 4-1. shows the commands and command sequences.

Table 4-1. Command sequence

Command sequence		1st bus cycle (Read cycle)		2nd bus cycle (Read cycle)		3rd bus cycle (Write cycle)		4th bus cycle (Write cycle)	
Partial refresh density	Page length	Address	Data	Address	Data	Address	Data	Address	Data
16M bits	4 words	1FFFFFH	—	1FFFFFH	—	1FFFFFH	00H	1FFFFFH	00H
	8 words	1FFFFFH	—	1FFFFFH	—	1FFFFFH	00H	1FFFFFH	04H
8M bits	4 words	1FFFFFH	—	1FFFFFH	—	1FFFFFH	00H	1FFFFFH	01H
	8 words	1FFFFFH	—	1FFFFFH	—	1FFFFFH	00H	1FFFFFH	05H
4M bits	4 words	1FFFFFH	—	1FFFFFH	—	1FFFFFH	00H	1FFFFFH	02H
	8 words	1FFFFFH	—	1FFFFFH	—	1FFFFFH	00H	1FFFFFH	06H
0M bit	4 words	1FFFFFH	—	1FFFFFH	—	1FFFFFH	00H	1FFFFFH	03H
	8 words	1FFFFFH	—	1FFFFFH	—	1FFFFFH	00H	1FFFFFH	07H

4th bus cycle (Write cycle)

I/O	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mode Register setting	0	0	0	0	0	0	0	0	0	0	0	0	0	PL	PD	

Page length	0	4 words
	1	8 words

	I/O1	I/O0	Density
Partial refresh density	0	0	16M bits
	0	1	8M bits
	1	0	4M bits
	1	1	0M bit

4.2 Cautions for Setting Mode Register

Since, for the mode register setting, the internal counter status is judged by toggling /CS and /OE, toggle /CS at every cycle during entry (read cycle twice, write cycle twice), and toggle /OE like /CS at the first and second read cycles.

If incorrect addresses or data are written, or if addresses or data are written in the incorrect order, the setting of the mode register are not performed correctly.

When the highest address (1FFFFFH) is read consecutively three or more times, the mode register setting entries are cancelled.

Once the page length and partial refresh density have been set in the mode register, these settings are retained until they are set again.

For the timing chart and flow chart, refer to **Figure 6-24. Mode Register Setting Timing Chart**, **Figure 6-25. Mode Register Setting Flow Chart**.

5. Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating		Unit
			μPD4632312-BxxX, μPD4632312-CxxX	μPD4632312-BExxX, μPD4632312-CExxX	
Supply voltage	V_{CC}		–0.5 Note to +4.0	–0.5 Note to +4.0	V
Input / Output supply voltage	V_{CCQ}		–	–0.5 Note to +4.0	V
Input / Output voltage	V_T		–0.5 Note to V_{CC} + 0.4 (4.0 V MAX.)	–0.5 Note to V_{CCQ} + 0.4 (4.0 V MAX.)	V
Operating ambient temperature	T_A		–25 to +85	–25 to +85	°C
Storage temperature	T_{stg}		–55 to +125	–55 to +125	°C

Note –1.0 V (MIN.) (Pulse width: 30 ns)

Caution Exposing the device to stress above those listed in Absolute Maximum Rating could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	μPD4632312 -BxxX		μPD4632312 -CxxX		μPD4632312 -BExxX		μPD4632312 -CExxX		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Supply voltage	V_{CC}		2.6	3.1	2.3	2.7	2.6	3.1	2.3	2.7	V
Input / Output supply voltage	V_{CCQ}		–	–	–	–	1.65	1.95	1.65	1.95	V
High level input voltage	V_{IH}		0.8V_{CC}	V_{CC}+0.3	0.8V_{CC}	V_{CC}+0.3	0.8V_{CCQ}	V_{CCQ}+0.3	0.8V_{CCQ}	V_{CCQ}+0.3	V
Low level input voltage	V_{IL}		–0.3 Note	0.2V_{CC}	–0.3 Note	0.2V_{CC}	–0.3 Note	0.2V_{CCQ}	–0.3 Note	0.2V_{CCQ}	V
Operating ambient temperature	T_A		–25	+85	–25	+85	–25	+85	–25	+85	°C

Note –0.5 V (MIN.) (Pulse width: 30 ns)

Capacitance (T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	V_{IN} = 0 V			8	pF
Input / Output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V			10	pF

Remarks 1. V_{IN}: Input voltage

$V_{I/O}$: Input / Output voltage

2. These parameters are not 100% tested.

DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted) (1/2)

Parameter	Symbol	Test condition	Density of data hold	μPD4632312-BxxX, μPD4632312-CxxX			Unit
				MIN.	TYP.	MAX.	
Input leakage current	I_{LI}	V_{IN} = 0 V to V_{CC}		–1.0		+1.0	μA
I/O leakage current	I_{LO}	$V_{I/O}$ = 0 V to V_{CC}, /CS = V_{IH} or /WE = V_{IL} or /OE = V_{IH}		–1.0		+1.0	μA
Operating supply current	I_{CCA}	/CS = V_{IL}, Minimum cycle time, $I_{I/O}$ = 0 mA				35	mA
Standby supply current	I_{SB1}	/CS ≥ V_{CC} – 0.2 V, MODE ≥ V_{CC} – 0.2 V	32M bits			100	μA
	I_{SB2}	/CS ≥ V_{CC} – 0.2 V, MODE ≤ 0.2 V	16M bits			70	
			8M bits			60	
			4M bits			50	
			0M bit			10	
High level output voltage	V_{OH}	I_{OH} = –0.5 mA		0.8V_{CC}			V
Low level output voltage	V_{OL}	I_{OL} = 1 mA				0.2V_{CC}	V

Remarks 1. V_{IN}: Input voltage

$V_{I/O}$: Input / Output voltage

2. These DC characteristics are in common regardless of product classifications.

DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted) (2/2)

Parameter	Symbol	Test condition	Density of data hold	μPD4632312-BExxX, μPD4632312-CExxX			Unit
				MIN.	TYP.	MAX.	
Input leakage current	I_{LI}	V_{IN} = 0 V to $V_{CC}Q$		–1.0		+1.0	μA
I/O leakage current	I_{LO}	$V_{I/O}$ = 0 V to $V_{CC}Q$, /CS = V_{IH} or /WE = V_{IL} or /OE = V_{IH}		–1.0		+1.0	μA
Operating supply current	I_{CCA}	/CS = V_{IL}, Minimum cycle time, $I_{I/O}$ = 0 mA				35	mA
Standby supply current	I_{SB1}	/CS ≥ V_{CC} – 0.2 V, MODE ≥ V_{CC} – 0.2 V	32M bits			100	μA
	I_{SB2}	/CS ≥ V_{CC} – 0.2 V, MODE ≤ 0.2 V	16M bits			70	
			8M bits			60	
			4M bits			50	
			0M bit			10	
High level output voltage	V_{OH}	I_{OH} = –0.5 mA		0.8$V_{CC}Q$			V
Low level output voltage	V_{OL}	I_{OL} = 1 mA				0.2$V_{CC}Q$	V

Remarks 1. V_{IN}: Input voltage

$V_{I/O}$: Input / Output voltage

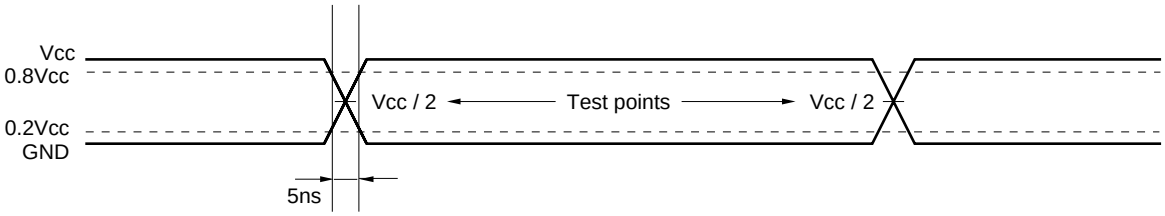
2. These DC characteristics are in common regardless of product classifications.

AC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

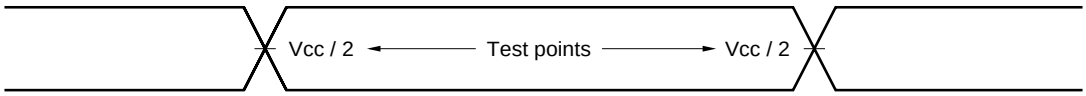
AC Test Conditions

[μPD4632312-B85X, μPD4632312-C95X]

Input Waveform (Rise and Fall Time ≤ 5 ns)

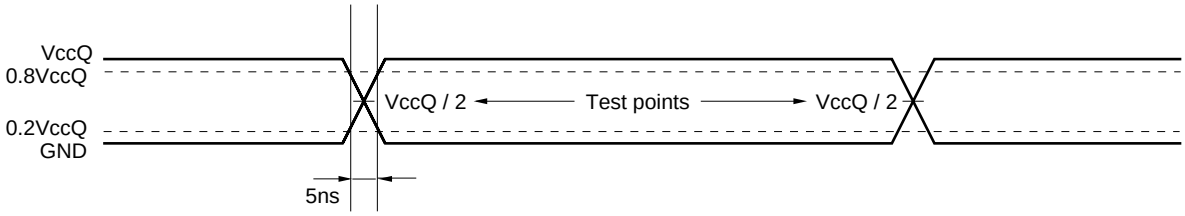


Output Waveform

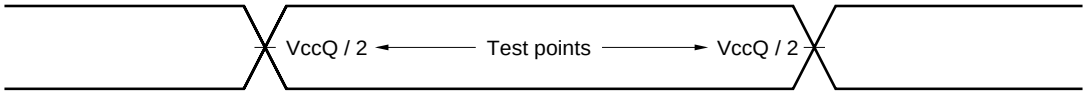


[μPD4632312-BE95X, μPD4632312-CE10X]

Input Waveform (Rise and Fall Time ≤ 5 ns)



Output Waveform



Output Load

AC characteristics directed with the note should be measured with the output load shown in Figure 5-1, Figure 5-2.

Figure 5-1. (B, C version)

C_L: 30 pF

5 pF (t_{CLZ}, t_{OLZ}, t_{BLZ}, t_{CHZ}, t_{OHZ}, t_{BHZ}, t_{WHZ}, t_{OW})

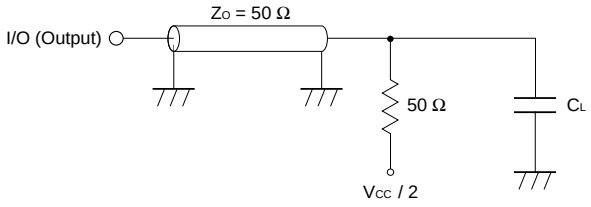
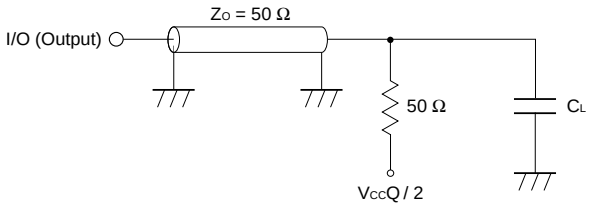


Figure 5-2. (BE, CE version)

C_L: 30 pF

5 pF (t_{CLZ}, t_{OLZ}, t_{BLZ}, t_{CHZ}, t_{OHZ}, t_{BHZ}, t_{WHZ}, t_{OW})



Read Cycle

Parameter	Symbol	μPD4632312 -B85X		μPD4632312 -C95X		μPD4632312 -BE95X		μPD4632312 -CE10X		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	85	10,000	95	10,000	95	10,000	105	10,000	ns	1
Identical address read cycle time	t_{RC1}	85	10,000	95	10,000	95	10,000	105	10,000	ns	2
Address skew time	t_{SKEW}		15		15		15		15	ns	3
/CS pulse width	t_{CP}	10		10		10		10		ns	
Address access time	t_{AA}		85		95		95		105	ns	4
/CS access time	t_{ACS}		85		95		95		105	ns	
/OE to output valid	t_{OE}		35		45		45		50	ns	5
/LB, /UB to output valid	t_{BA}		35		45		45		50	ns	
Output hold from address change	t_{OH}	10		10		10		10		ns	
/CS to output in low impedance	t_{CLZ}	10		10		10		10		ns	
/OE to output in low impedance	t_{OLZ}	5		5		5		5		ns	
/LB, /UB to output in low impedance	t_{BLZ}	5		5		5		5		ns	
/CS to output in high impedance	t_{CHZ}		25		25		25		25	ns	
/OE to output in high impedance	t_{OHZ}		25		25		25		25	ns	
/LB, /UB to output in high impedance	t_{BHZ}		25		25		25		25	ns	

Notes 1. One read cycle (t_{RC}) must satisfy the minimum value ($t_{RC(MIN.)}$) and maximum value ($t_{RC(MAX.)}$ = 10 μs). t_{RC} indicates the time from the /CS low level input point or address change start point, whichever is later, to the /CS high level input point or the next address change start point, whichever is earlier. As a result, there are the following four conditions for t_{RC}.

1) Time from address change start point to /CS high level input point (address access)
2) Time from address change start point to next address change start point (address access)
3) Time from /CS low level input point to next address change start point (/CS access)
4) Time from /CS low level input point to /CS high level input point (/CS access)

2. The identical address read cycle time (t_{RC1}) is the cycle time of one read operation when performing continuous read operations toggling /OE , /LB, and /UB with the address fixed and /CS low level. Perform settings so that the sum (t_{RC}) of the identical address read cycle times (t_{RC1}) is 10 μs or less.

3. t_{SKEW} indicates the following three types of time depending on the condition.

1) When switching /CS from high level to low level, t_{SKEW} is the time from the /CS low level input point until the next address is determined.
2) When switching /CS from low level to high level, t_{SKEW} is the time from the address change start point to the /CS high level input point.
3) When /CS is fixed to low level, t_{SKEW} is the time from the address change start point until the next address is determined.

Since specs are defined for t_{SKEW} only when /CS is active, t_{SKEW} is not subject to limitations when /CS is switched from high level to low level following address determination, or when the address is changed after /CS is switched from low level to high level.

4. Regarding t_{AA} and t_{ACS}, only t_{AA} is satisfied during address access (refer to 1) and 2) of **Note 1**), and only t_{ACS} is satisfied during /CS access (refer to 3) of **Note 1**).

5. Regarding t_{BA} and t_{OE}, only t_{BA} is satisfied if /OE becomes active later than /UB and /LB, and only t_{OE} is satisfied if /UB and /LB become active before /OE.

Page Read Cycle

Parameter	Symbol	μPD4632312 -B85X		μPD4632312 -C95X		μPD4632312 -BE95X		μPD4632312 -CE10X		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Page read cycle time	t_{PRC}	40		45		40		45		ns	
Page access time	t_{PAA}		35		40		40		45	ns	
Normal to page read cycle time	t_{NPRC}		10,000		10,000		10,000		10,000	ns	1
/OE to address setup time	t_{OAS}	–5		–5		–5		–5		ns	2
/OE pulse width	t_{OP}	10		10		10		10		ns	

Notes 1. Normal to page read cycle time (t_{NPRC}) is the total cycle time for one 4 word page read and one 8 word page read. Perform settings to that (t_{NPRC}) is 10 μs or less.

2. /OE to address setup time (t_{OAS}) and /OE pulse width (t_{OP}) are effective only when 8 word page read is set. (Refer to section **3.8. Cautions for Eight-Word Page Read Operation**.)

Standby Mode Entry / Exit

Parameter	Symbol	MIN.	MAX.	Unit	Note
/CS High to MODE Low	t_{CM}	0		ns	
MODE High to /CS Low	t_{MC}	30		ns	

Cautions 1. Make MODE and /CS high level during the wait time interval.

2. Make MODE high level during the wait time and three read operations.

3. The read operation must satisfy the specs described on page 17 (Read Cycle).

4. The address is don't care (V_{IH} or V_{IL}) during read operation.

5. Read operation must be executed with toggled the /CS pin.

6. To prevent bus contention, it is recommended to set /OE to high level.

7. Do not input data to the I/O pins if /OE is low level during a read operation.

Write Cycle

Parameter	Symbol	μPD4632312 -B85X		μPD4632312 -C95X		μPD4632312 -BE95X		μPD4632312 -CE10X		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write cycle time	t_{WC}	85	10,000	95	10,000	95	10,000	105	10,000	ns	1
Identical address write cycle time	t_{WC1}	85	10,000	95	10,000	95	10,000	105	10,000	ns	2
Address skew time	t_{SKEW}		15		15		15		15	ns	3
/CS to end of write	t_{CW}	40		50		50		55		ns	4
/LB, /UB to end of write	t_{BW}	30		35		35		40		ns	
Address valid to end of write	t_{AW}	35		40		40		45		ns	
Write pulse width	t_{WP}	30		35		35		40		ns	
Write recovery time	t_{WR}	20		20		20		20		ns	5
/CS pulse width	t_{CP}	10		10		10		10		ns	
Address setup time	t_{AS}	0		0		0		0		ns	
Byte write hold time	t_{BWH}	20		20		20		20		ns	
Data valid to end of write	t_{DW}	20		30		30		40		ns	
Data hold time	t_{DH}	0		0		0		0		ns	
/OE to output in low impedance	t_{OLZ}	5		5		5		5		ns	
/WE to output in high impedance	t_{WHZ}		25		25		25		25	ns	
/OE to output in high impedance	t_{OHZ}		25		25		25		25	ns	
Output active from end of write	t_{OW}	5		5		5		5		ns	

Notes 1. One write cycle (t_{WC}) must satisfy the minimum value ($t_{WC(MIN.)}$) and the maximum value ($t_{WC(MAX.)}$ = 10 μs). t_{WC} indicates the time from the /CS low level input point or address change start point, whichever is after, to the /CS high level input point or the next address change start point, whichever is earlier. As a result, there are the following four conditions for t_{WC}.

1) Time from address change start point to /CS high level input point
2) Time from address change start point to next address change start point
3) Time from /CS low level input point to next address change start point
4) Time from /CS low level input point to /CS high level input point

2. The identical address read cycle time (t_{WC1}) is the cycle time of one write cycle when performing continuous write operations with the address fixed and /CS low level, changing /LB and /UB at the same time, and toggling /WE, as well as when performing a continuous write toggling /LB and /UB. Make settings so that the sum (t_{WC}) of the identical address write cycle times (t_{WC1}) is 10 μs or less.

3. t_{SKEW} indicates the following three types of time depending on the condition.

1) When switching /CS from high level to low level, t_{SKEW} is the time from the /CS low level input point until the next address is determined.
2) When switching /CS from low level to high level, t_{SKEW} is the time from the address change start point to the /CS high level input point.
3) When /CS is fixed to low level, t_{SKEW} is the time from the address change start point until the next address is determined.

Since specs are defined for t_{SKEW} only when /CS is active, t_{SKEW} is not subject to limitations when /CS is switched from high level to low level following address determination, or when the address is changed after /CS is switched from low level to high level.

4. Definition of write start and write end

	/CS	/WE	/LB, /UB	Status
Write start pattern 1	H to L	L	L	If /WE, /LB, /UB are low level, time when /CS changes from high level to low level
Write start pattern 2	L	H to L	L	If /CS, /LB, /UB are low level, time when /WE changes from high level to low level
Write start pattern 3	L	L	H to L	If /CS, /WE are low level, time when /LB or /UB changes from high level to low level
Write end pattern 1	L	L to H	L	If /CS, /WE, /LB, /UB are low level, time when /WE changes from low level to high level
Write end pattern 2	L	L	L to H	When /CS, /WE, /LB, /UB are low level, time when /LB or /UB changes from low level to high level

5. Definition of write end recovery time (t_{WR})

1) Time from write end to address change start point, or from write end to /CS high level input point
2) When /CS, /LB, /UB are low level and continuously written to the identical address, time from /WE high level input point to /WE low level input point
3) When /CS, /WE are low level and continuously written to the identical address, time from /LB or /UB high level input point, whichever is later, to /LB or /UB low level input point, whichever is earlier.
4) When /CS is low level and continuously written to the identical address, time from write end to point at which /WE , /LB, or /UB starts to change from high level to low level, whichever is earliest.

Read Write Cycle

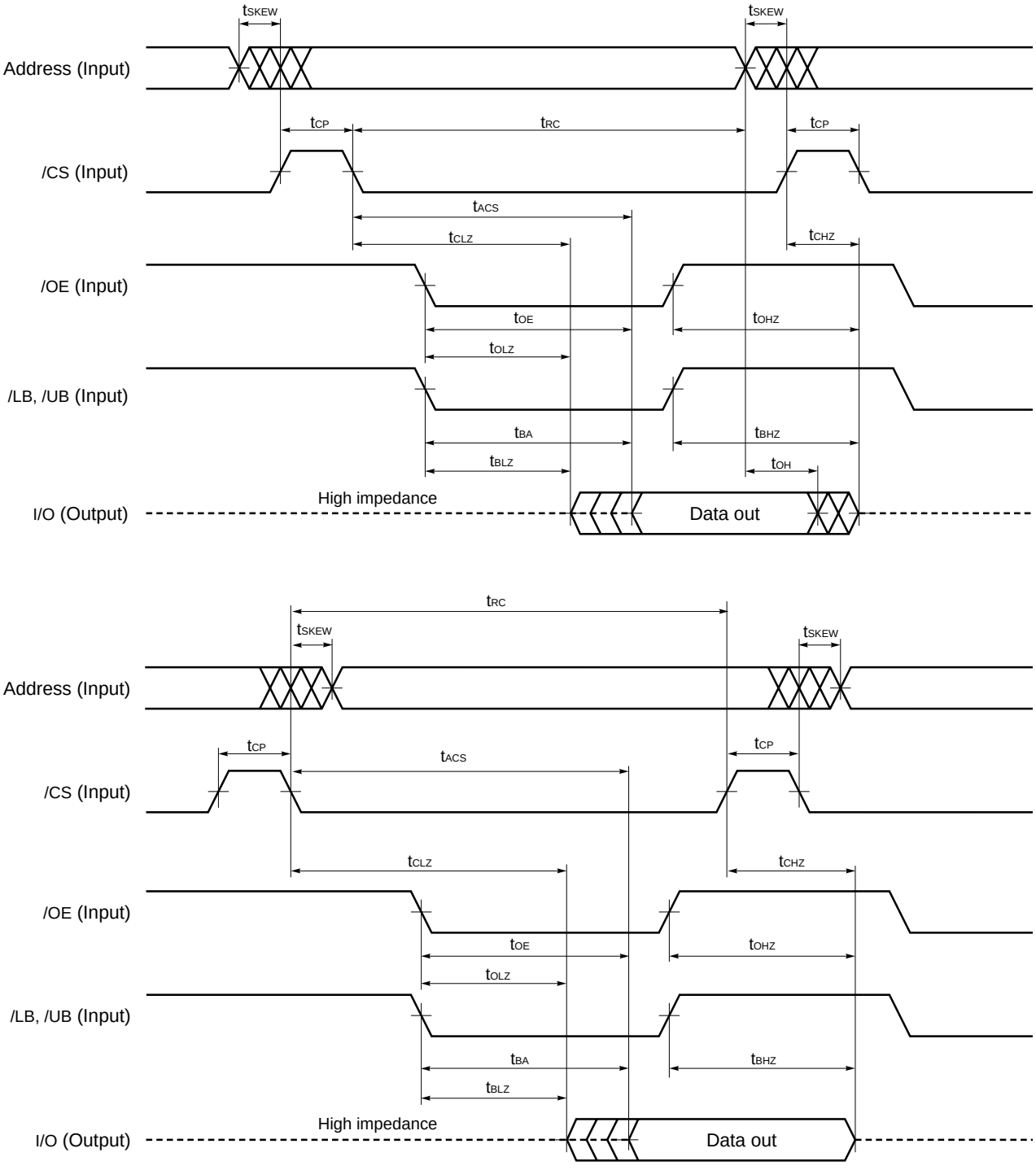
Parameter	Symbol	MIN.	MAX.	Unit	Note
Read write cycle time	t_{RWC}		10,000	ns	1, 2
Byte write setup time	t_{BWS}	20		ns	
Byte read setup time	t_{BRS}	20		ns	

Notes 1. Make settings so that the sum (t_{RWC}) of the identical address read cycle time (t_{RC1}) and the identical address write cycle time (t_{WC1}) is 10 μs or less when a write is performed at the identical address using /UB following a read using /LB with /CS low level, or when a write is performed using /LB following a read using /UB.

2. Make settings so that the sum (t_{RWC}) of the identical address read cycle time (t_{RC1}) and the identical address write cycle time (t_{WC1}) is 10 μs or less when a read is performed at the identical address using /UB following a write using /LB with /CS low level, or when a read is performed using /LB following a write using /UB.

6. Timing Charts

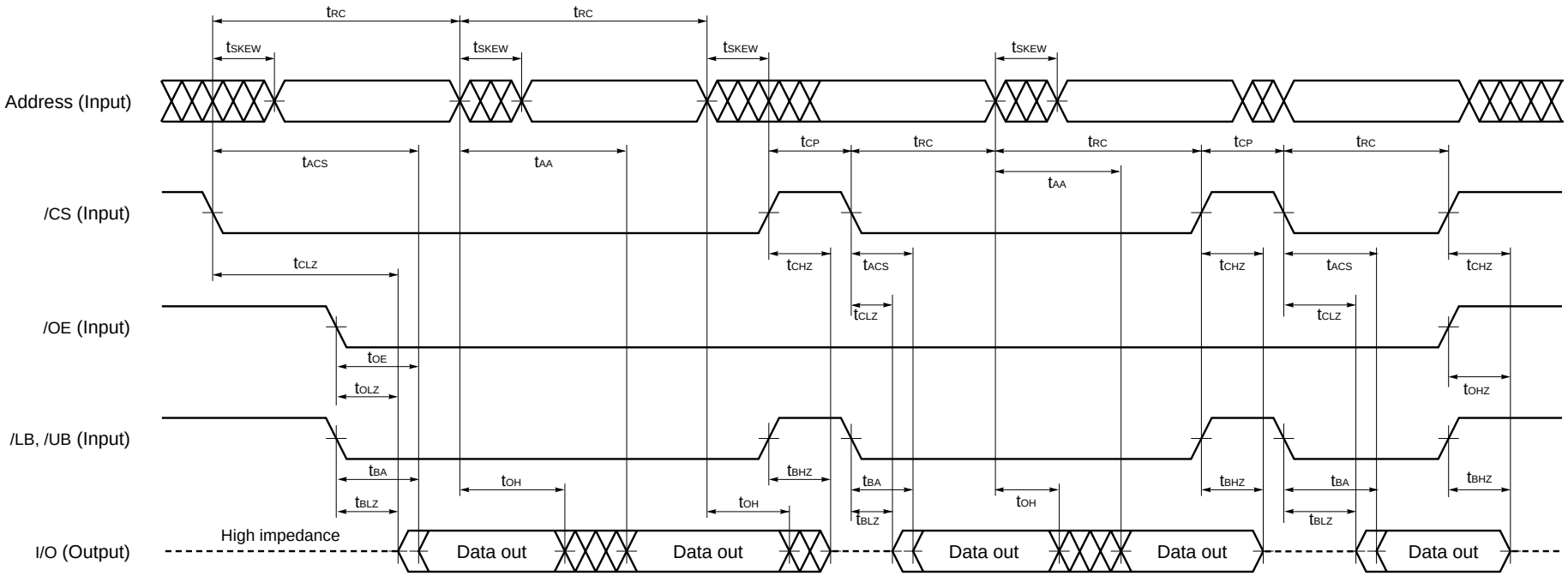
Figure 6-1. Read Cycle Timing Chart 1



Caution If the address is changed using a value that is either lower than the minimum value or higher than the maximum value for the read cycle time (t_{RC}), none of the data can be guaranteed.

Remark In read cycle, /WE should be fixed to High.

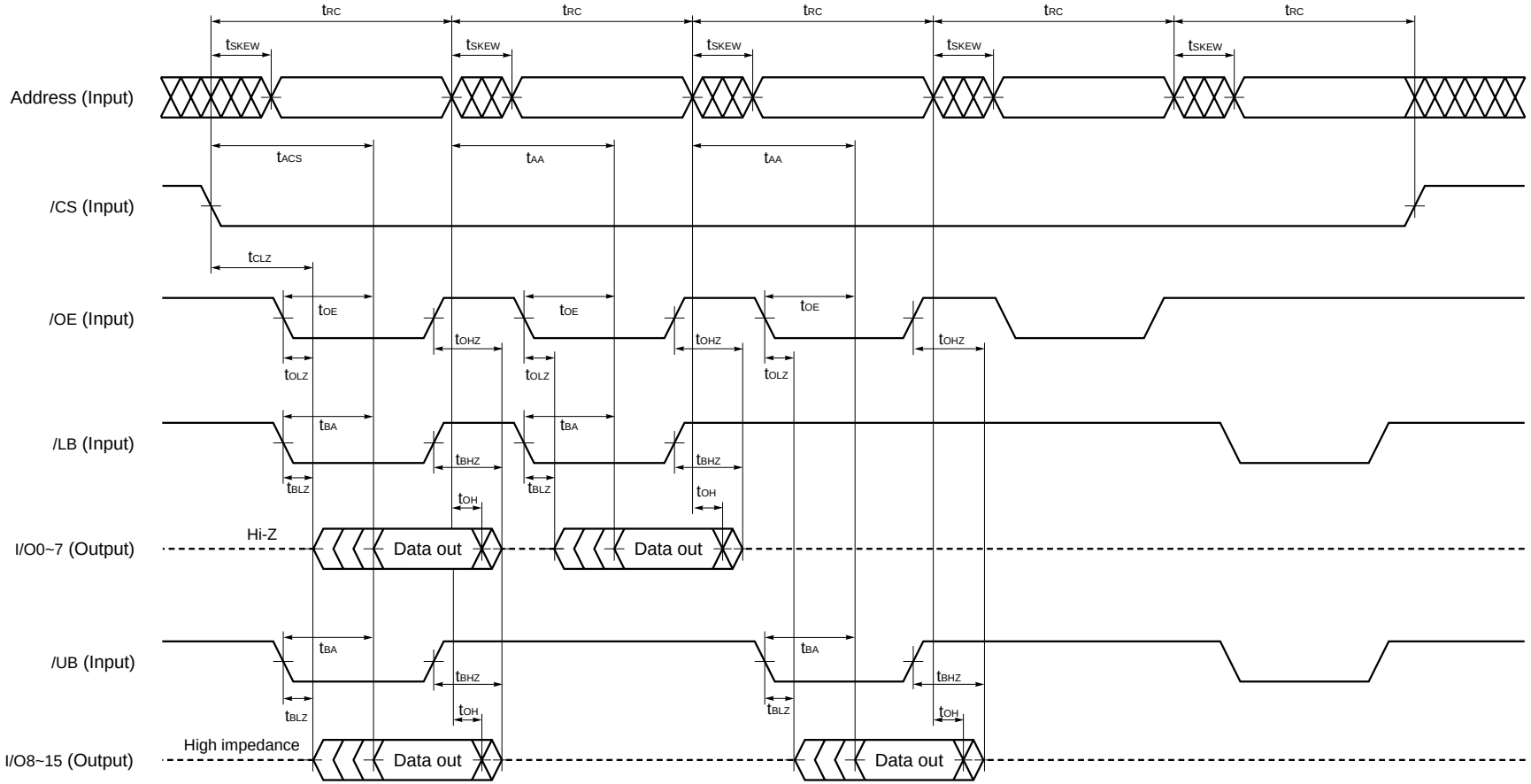
Figure 6-2. Read Cycle Timing Chart 2



Caution If the address is changed using a value that is either lower than the minimum value or higher than the maximum value for the read cycle time (t_{RC}), none of the data can be guaranteed.

Remark In read cycle, /WE should be fixed to High.

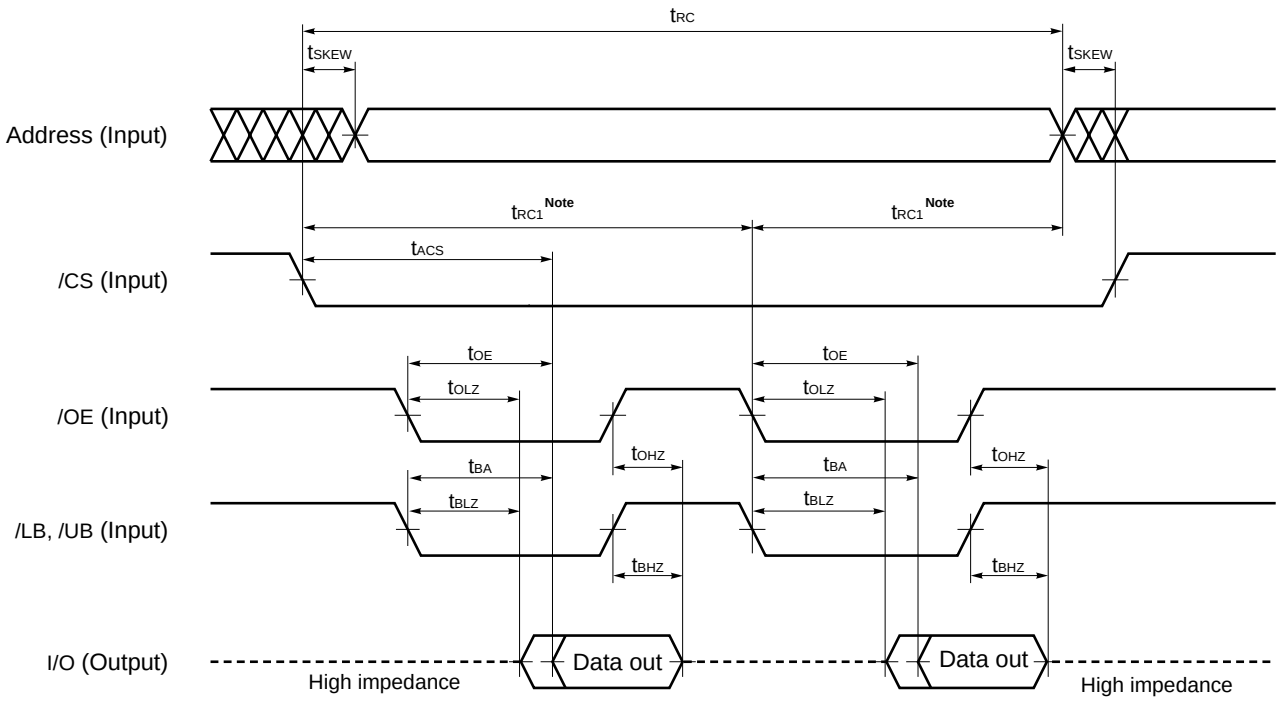
Figure 6-3. Read Cycle Timing Chart 3



Caution If the address is changed using a value that is either lower than the minimum value or higher than the maximum value for the read cycle time (t_{RC}), none of the data can be guaranteed.

Remark In read cycle, /WE should be fixed to High.

Figure 6-4. Read Cycle Timing Chart 4



Caution If the address is changed using a value that is either lower than the minimum value or higher than the maximum value for the read cycle time (t_{RC}), none of the data can be guaranteed.

Note To perform a continuous read toggling /OE, /UB, and /LB with /CS low level at an identical address, make settings so that the sum (t_{RC}) of the identical address read cycle times (t_{RC1}) is 10 μs or less.

Remark In read cycle, /WE should be fixed to High.

Figure 6-5. 4 Words Page Read Cycle Timing Chart

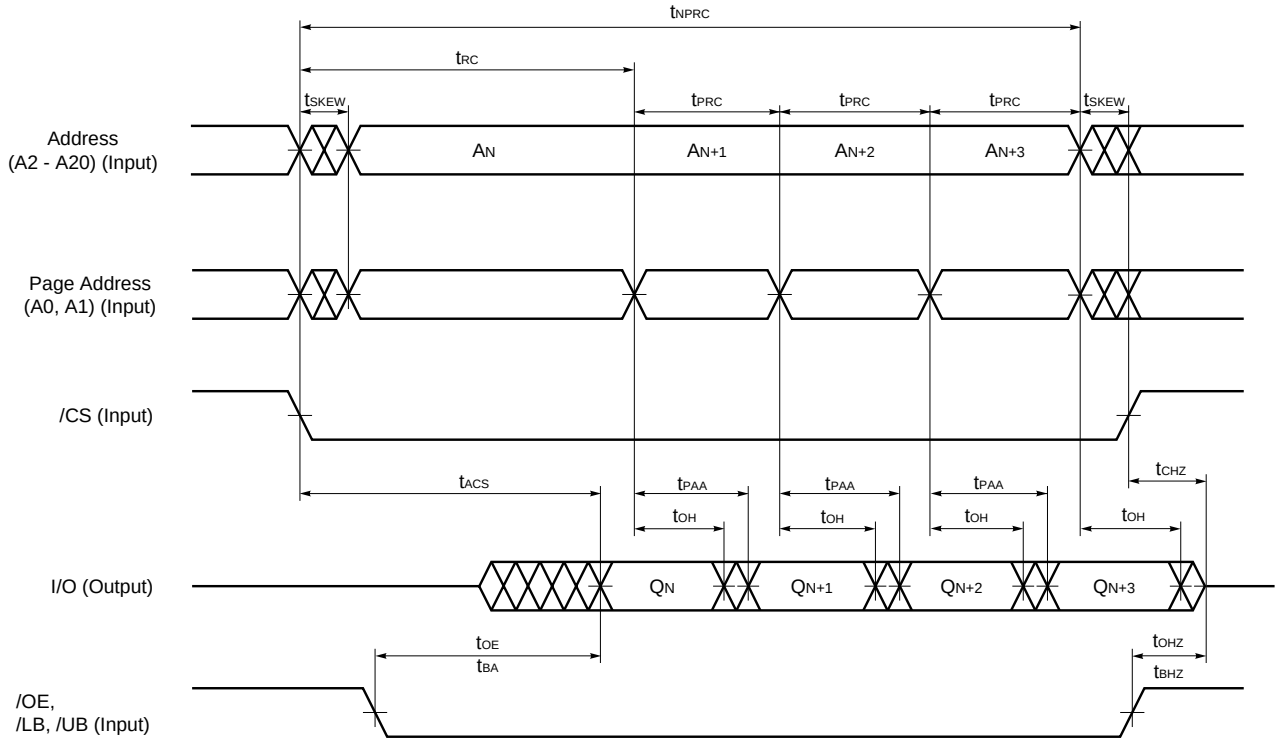


Figure 6-6. 8 Words Page Read Cycle Timing Chart

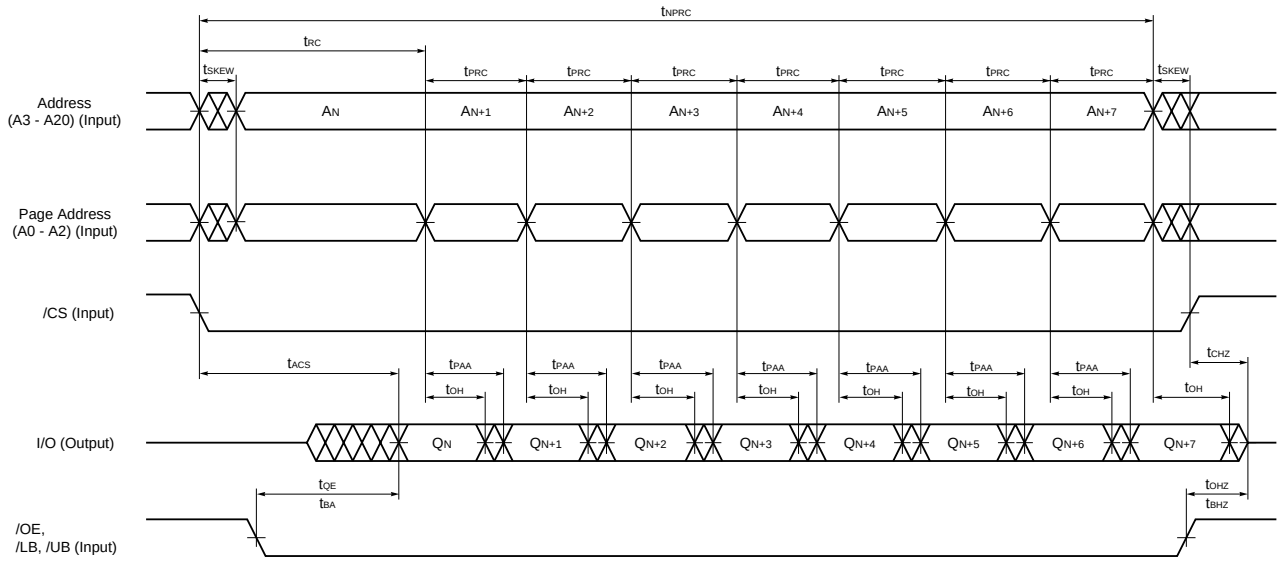
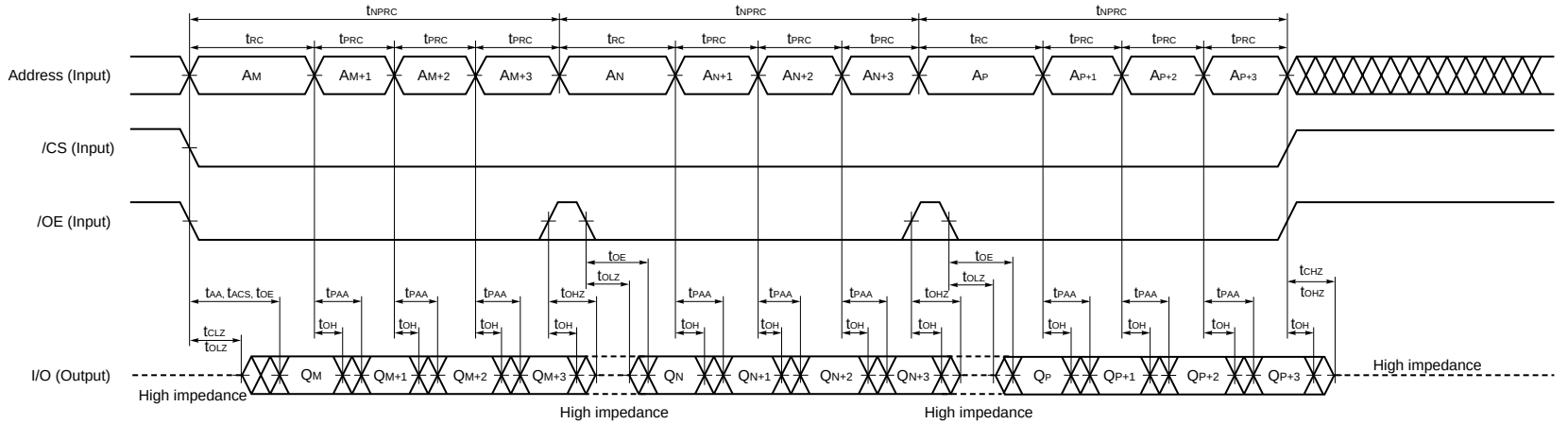


Figure 6-7. 4 / 8 Words Continuous Page Read Cycle Timing Chart

4 word page read continuous operation



8 word page read continuous operation

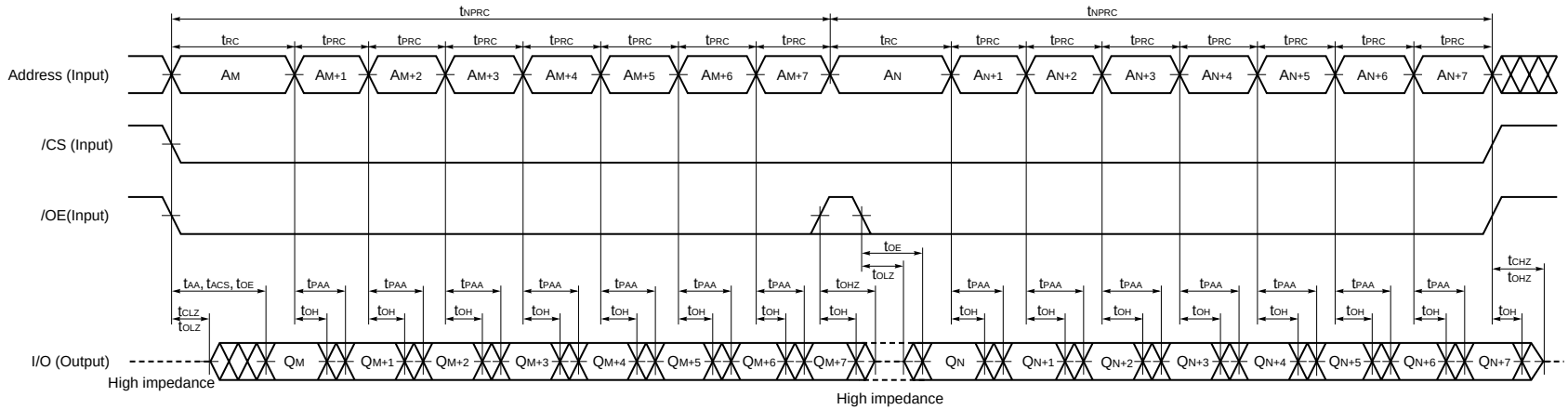
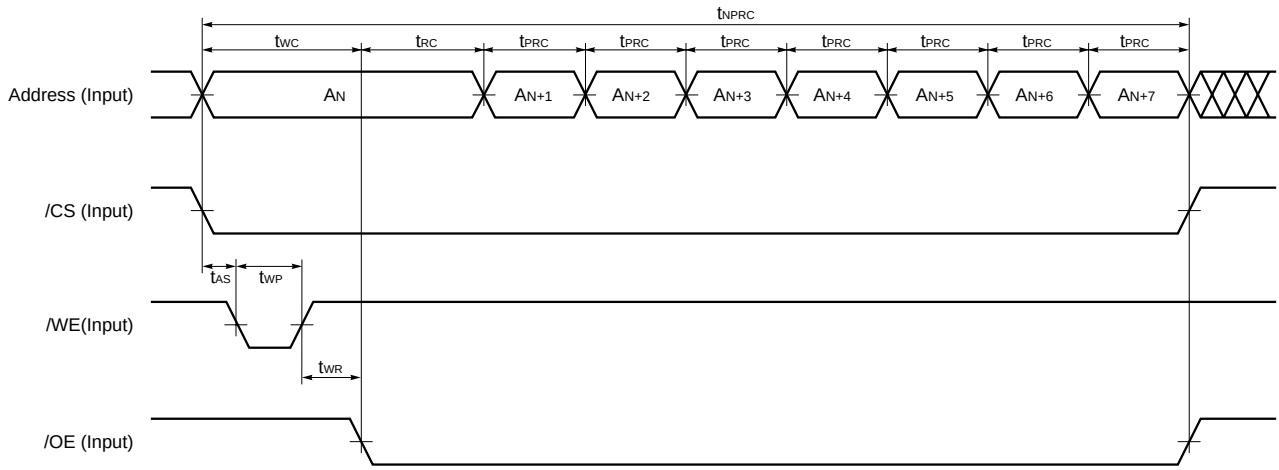


Figure 6-8. Prohibition of 8 Words Page Read Start after Write Modify Read Cycle Timing Chart



Caution 8 words page read cannot be started with write modify read.

8 words page read can be started by unselecting /CS after writing to A_N and then reading A_N again.

Figure 6-9. 8 Words Page Read Start after Write Modify Read Timing Chart

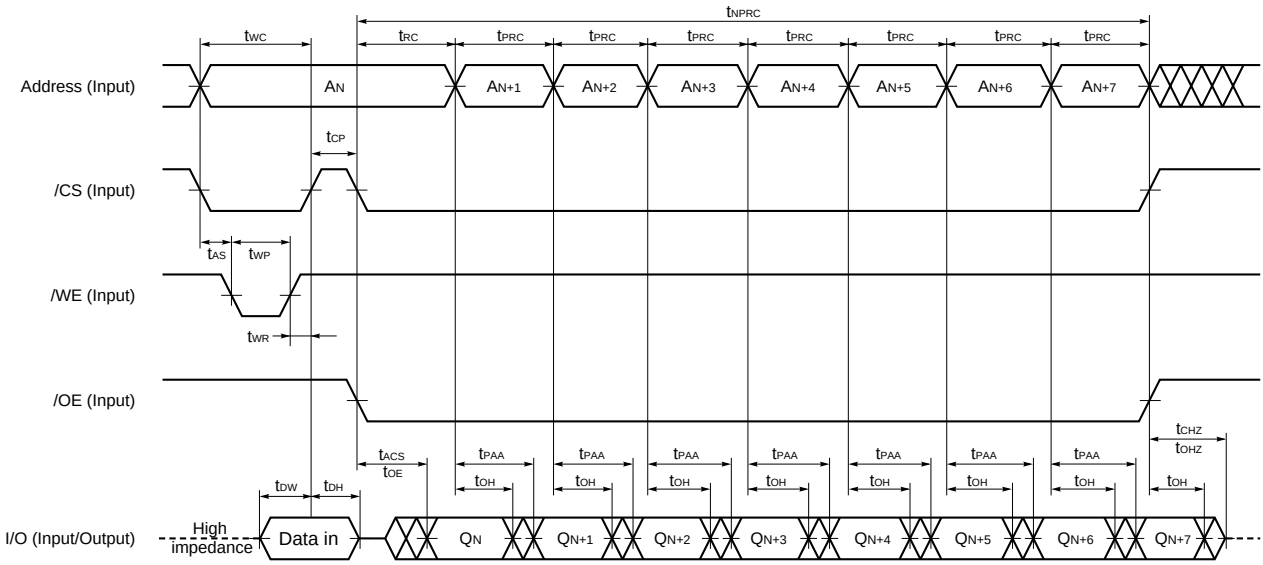


Figure 6-10. Prohibition of 8 Words 2 Continuous Read Cycles Timing Chart

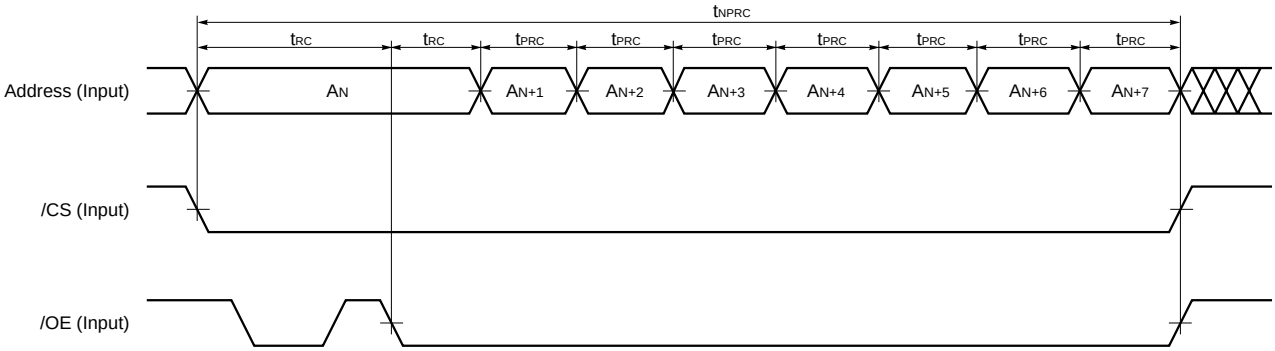


Figure 6-11. 8 Words 2 Continuous Read Cycles Timing Chart

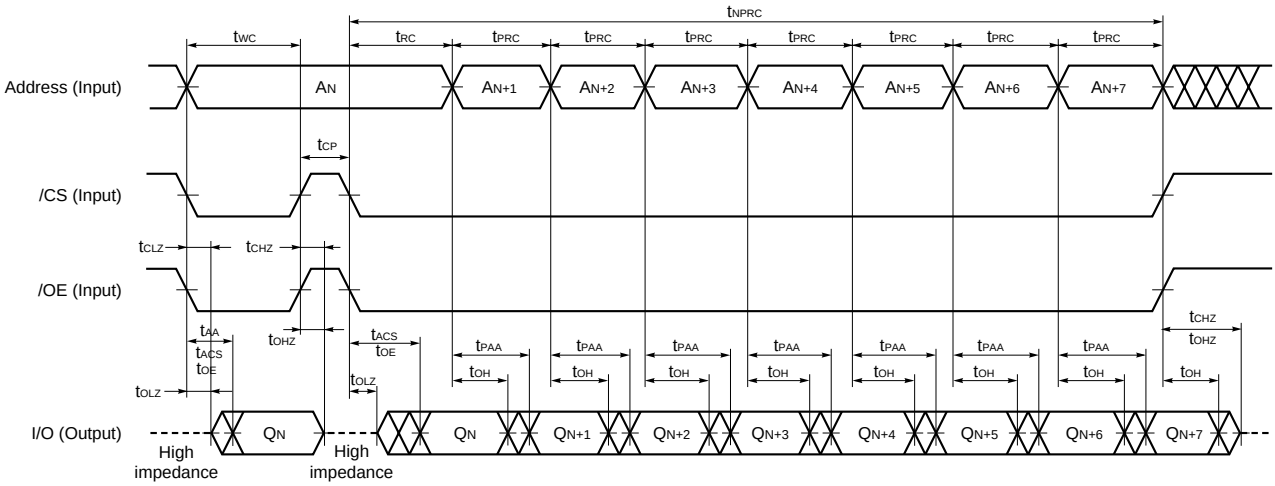
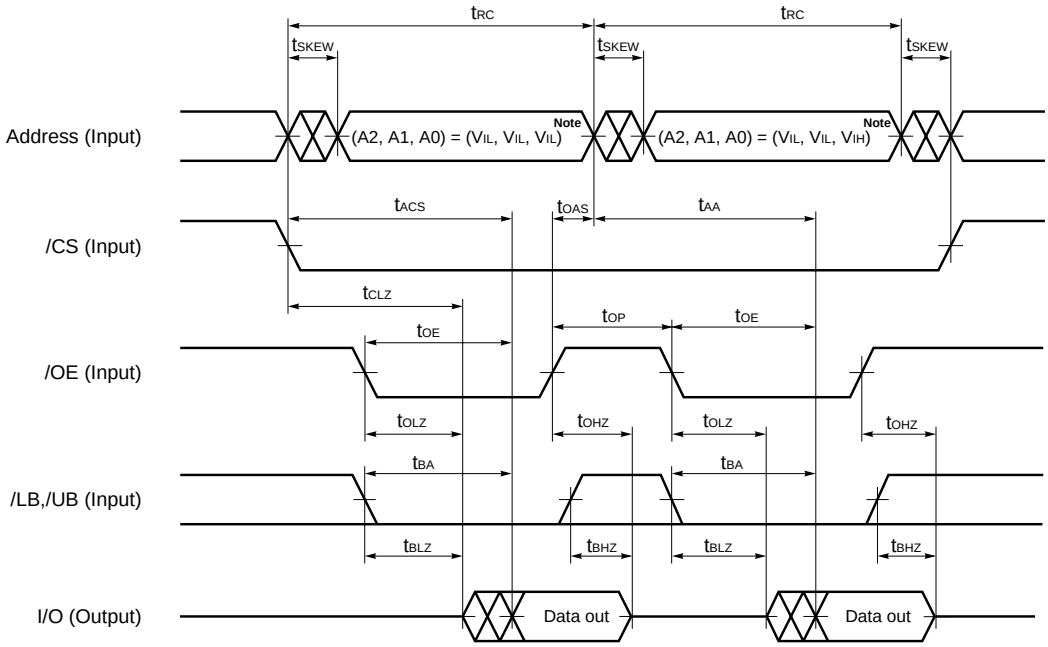


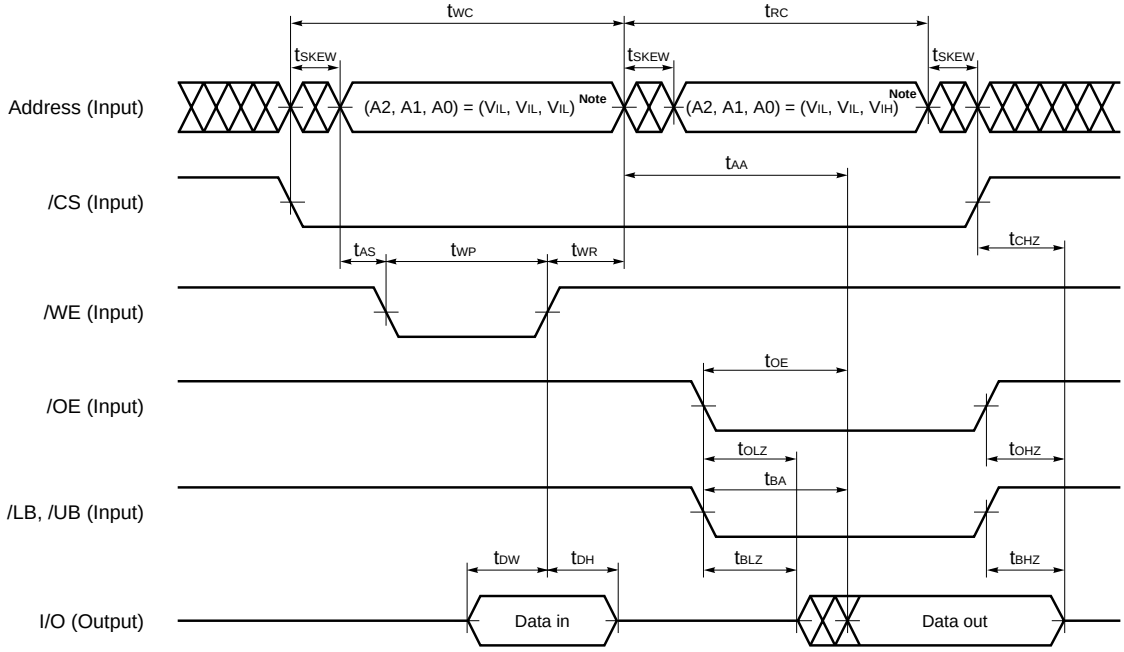
Figure 6-12. 8 Words Normal Read Cycle Timing Chart



Caution Always toggle /OE. If /OE is fixed to low level, page read starts.

Note A3 and higher address do not change. (A20 to A3) addresses are constant.

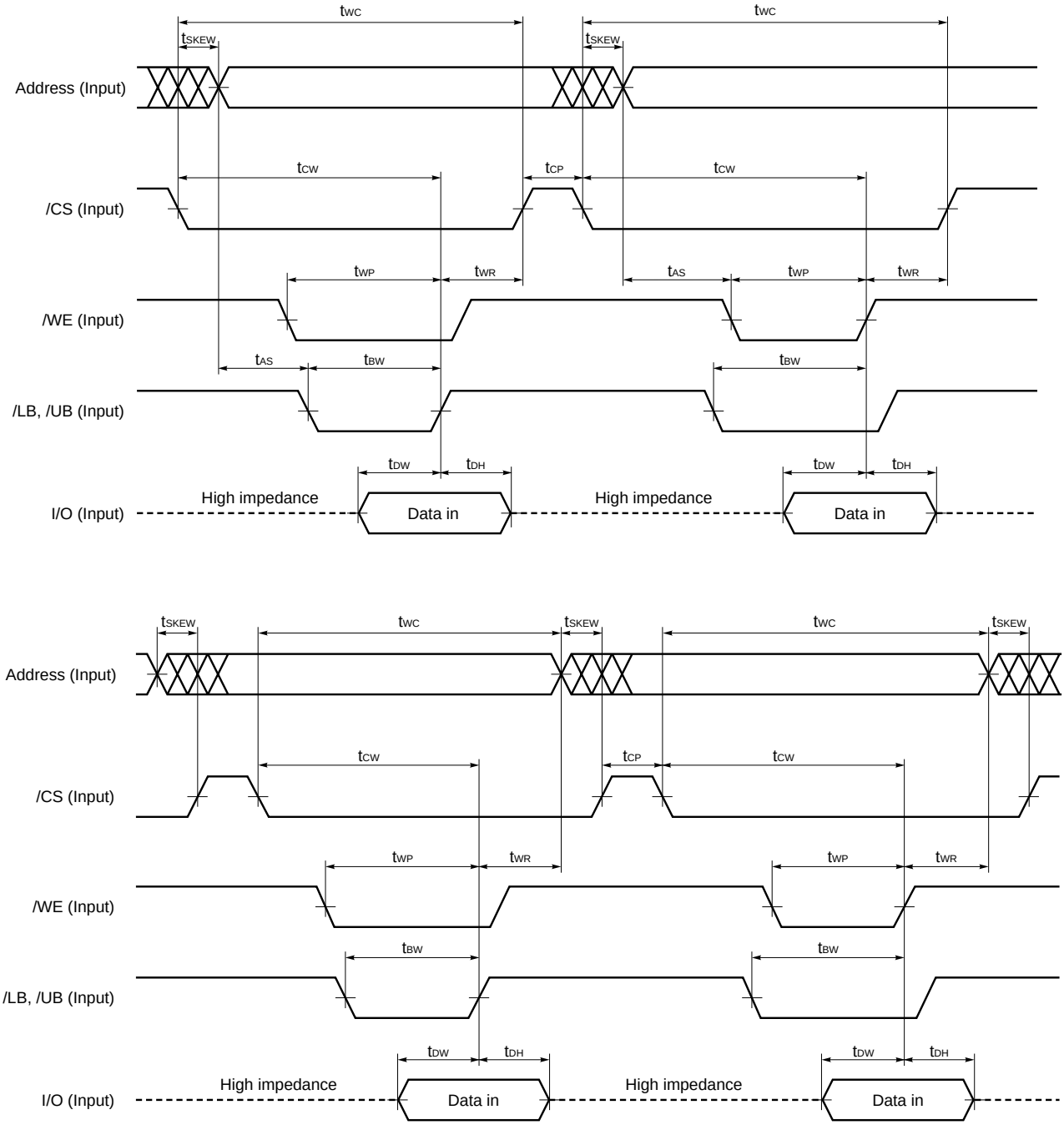
Figure 6-13. 8 Words Write-Abort to Read Cycle Timing Chart



Caution When performing a read operation to (A2, A1, A0) = (V_{IL}, V_{IL}, V_{IH}) from when (A2, A1, A0) = (V_{IL}, V_{IL}, V_{IL}) are in a write-abort state, it is recognized as a page read.

Note A3 and higher address do not change. (A20 toA3) addresses are constant.

Figure 6-14. Write Cycle Timing Chart 1



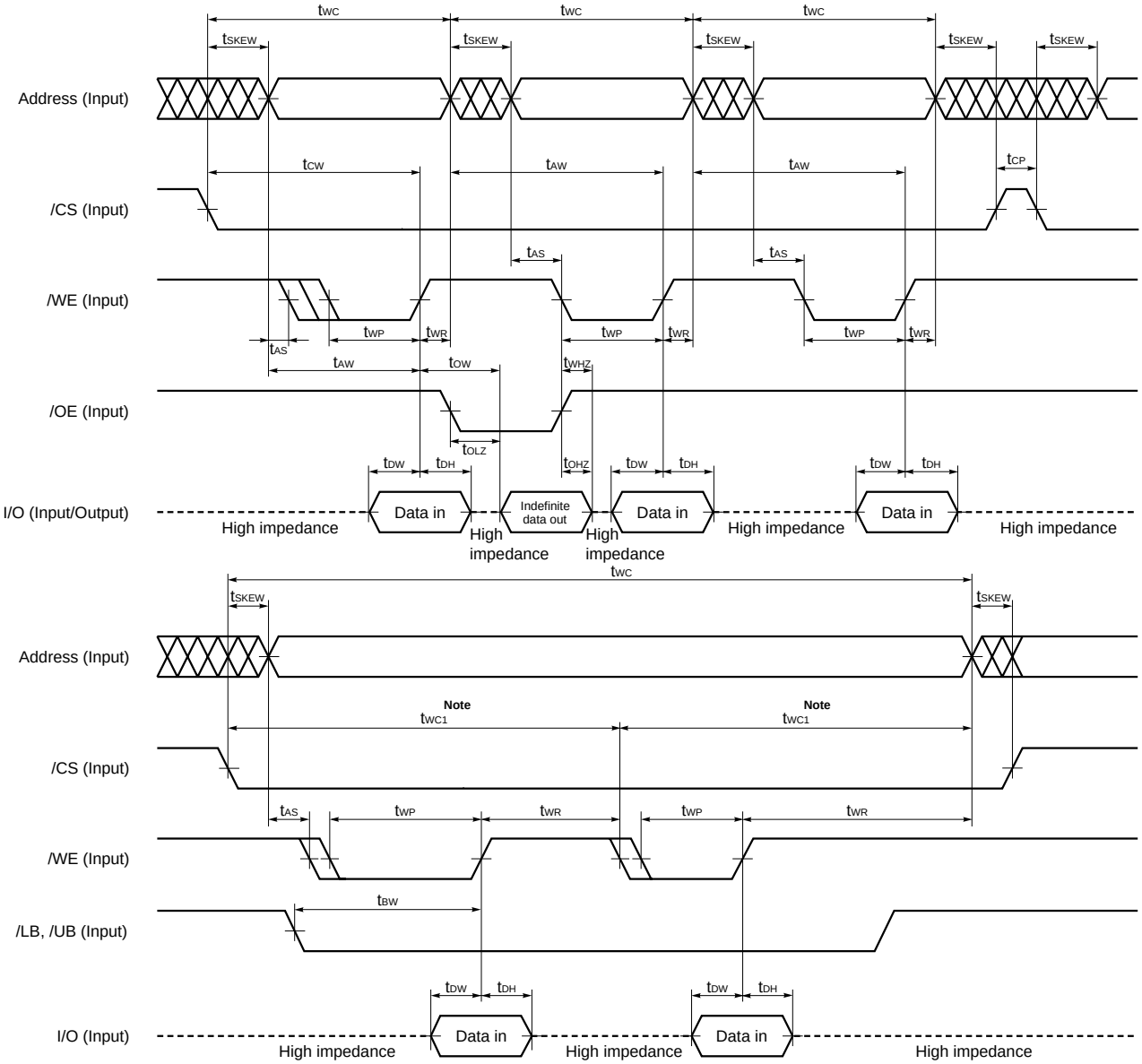
Cautions 1. During address transition, at least one of pins /CS, /WE should be inactivated.

2. Do not input data to the I/O pins while they are in the output state.

3. If the address is changed using a value that is either lower than the minimum value or higher than the maximum value for the write cycle time (t_{WC}), none of the data can be guaranteed.

Remark Write operation is done during the overlap time of a Low /CS, /WE, /LB and/or /UB.

Figure 6-15. Write Cycle Timing Chart 2 (/WE Controlled)



Cautions 1. During address transition, at least one of pins /CS, /WE should be inactivated.

2. Do not input data to the I/O pins while they are in the output state.

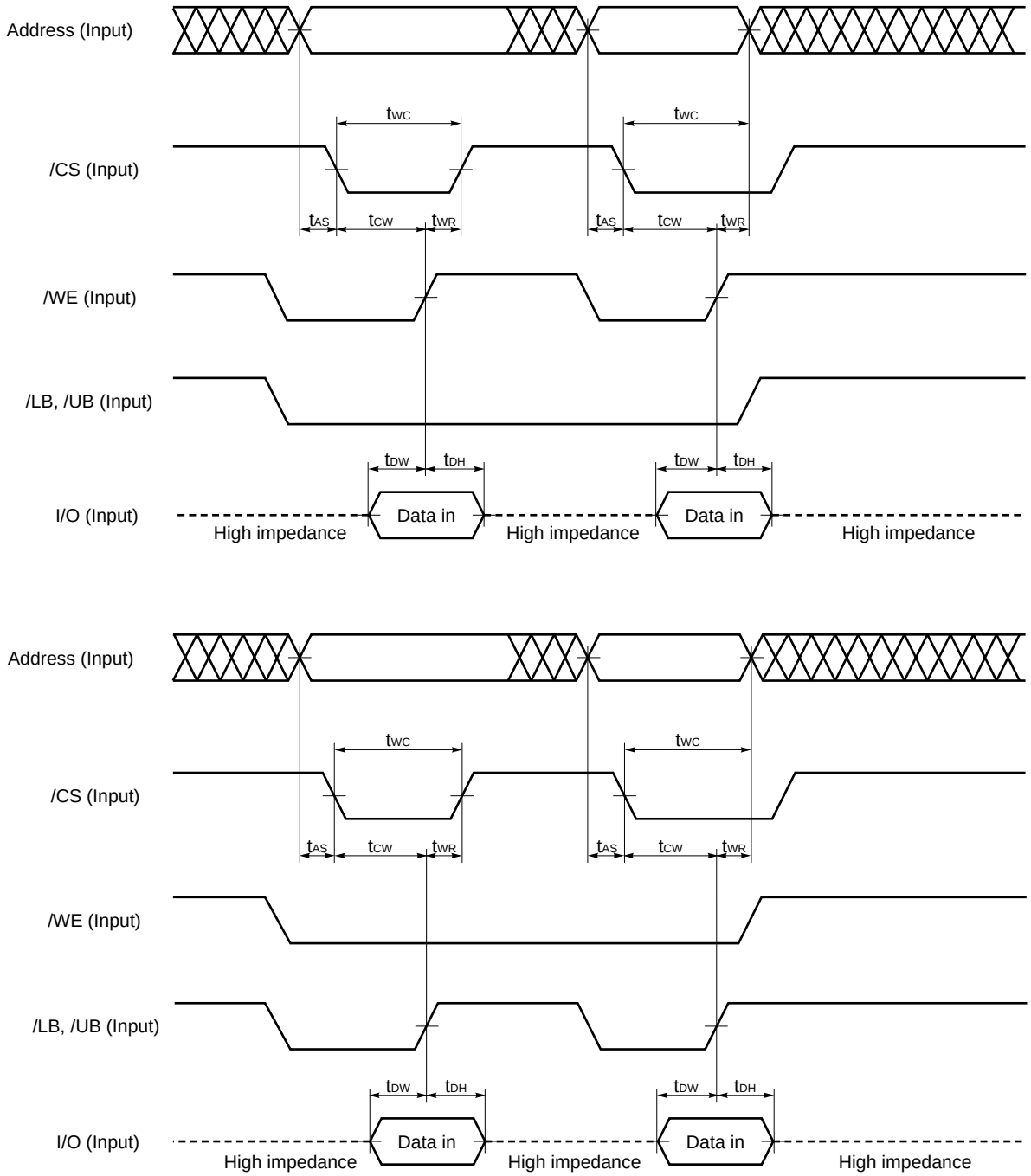
3. If the address is changed using a value that is either lower than the minimum value or higher than the maximum value for the write cycle time (t_{WC}), none of the data can be guaranteed.

Note If /LB and /UB are changed at the same time with /CS low level and a continuous write operation toggling /WE is performed, make settings so that the sum (t_{WC}) of the identical address write cycle time (t_{WC1}) is 10 μs or less.

Remarks 1. Write operation is done during the overlap time of a Low /CS, /WE, /LB and/or /UB.

2. When /WE is at Low, the I/O pins are always high impedance. When /WE is at High, read operation is executed. Therefore /OE should be at High to make the I/O pins high impedance.

Figure 6-16. Write Cycle Timing Chart 3 (/CS Controlled)



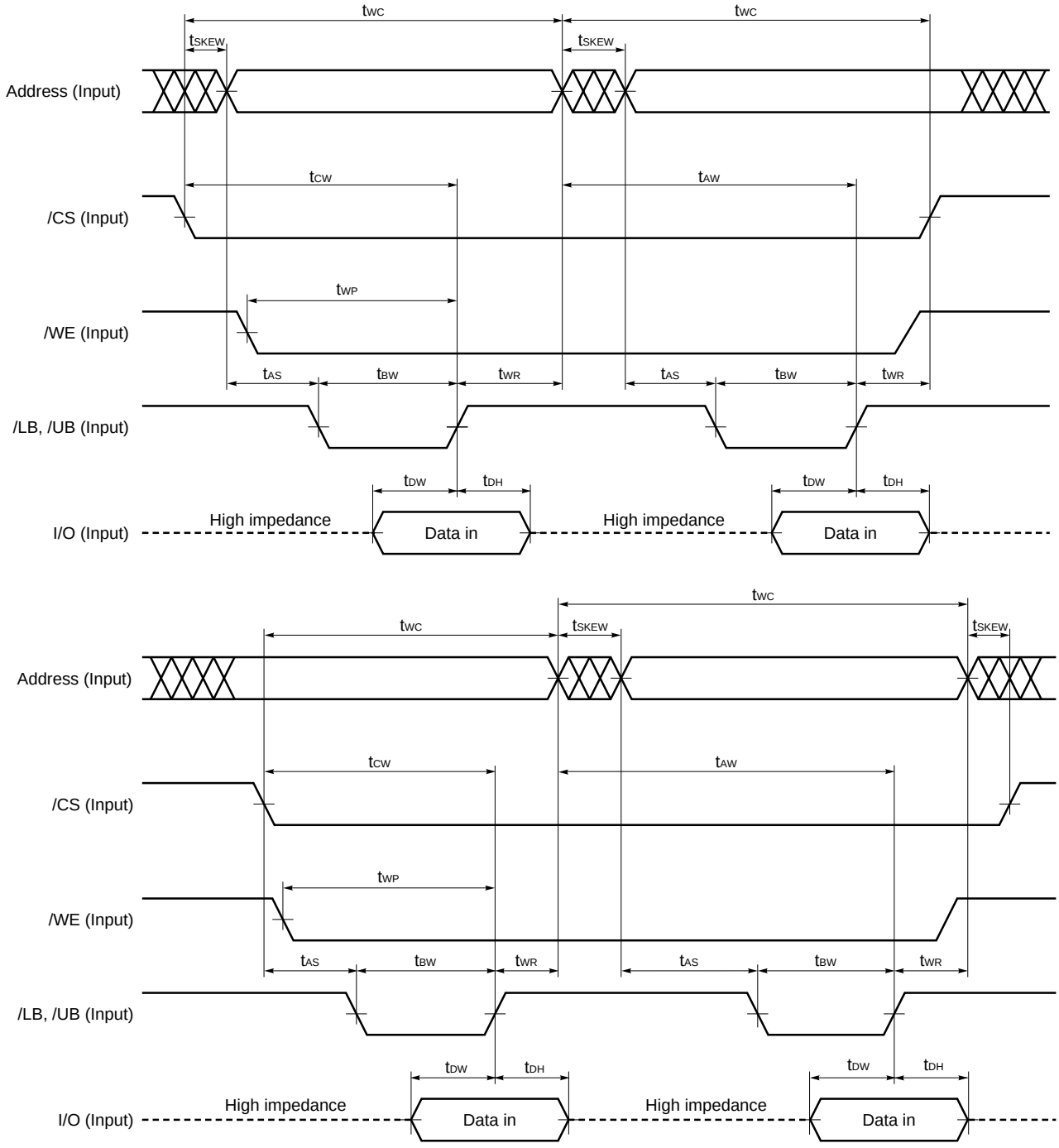
Cautions 1. During address transition, at least one of pins /CS, /WE should be inactivated.

2. Do not input data to the I/O pins while they are in the output state.

3. If the address is changed using a value that is either lower than the minimum value or higher than the maximum value for the write cycle time (t_{WC}), none of the data can be guaranteed.

Remark Write operation is done during the overlap time of a Low /CS, /WE, /LB and/or /UB.

Figure 6-17. Write Cycle Timing Chart 4 (/LB, /UB Controlled 1)



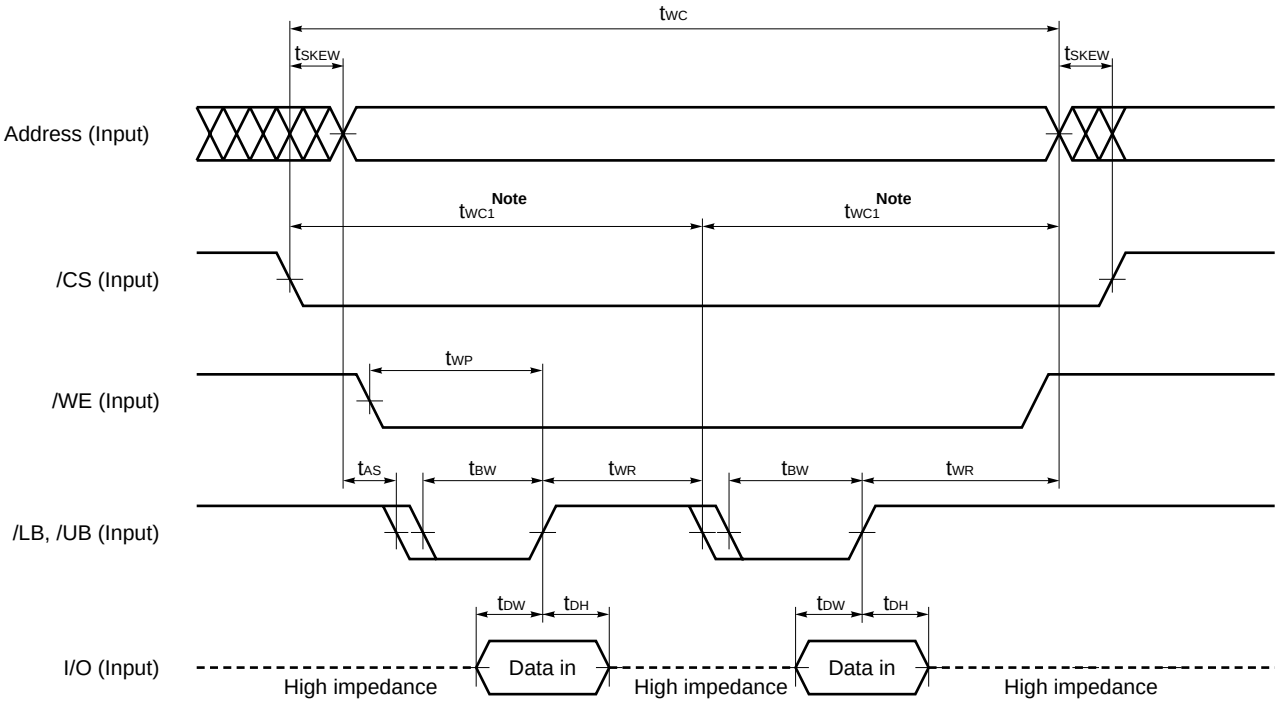
Cautions 1. During address transition, at least one of pins /CS, /WE should be inactivated.

2. Do not input data to the I/O pins while they are in the output state.

3. If the address is changed using a value that is either lower than the minimum value or higher than the maximum value for the write cycle time (t_{WC}), none of the data can be guaranteed.

Remark Write operation is done during the overlap time of a Low /CS, /WE, /LB and/or /UB.

Figure 6-18. Write Cycle Timing Chart 5 (/LB, /UB Controlled 2)



Cautions 1. During address transition, at least one of pins /CS, /WE should be inactivated.

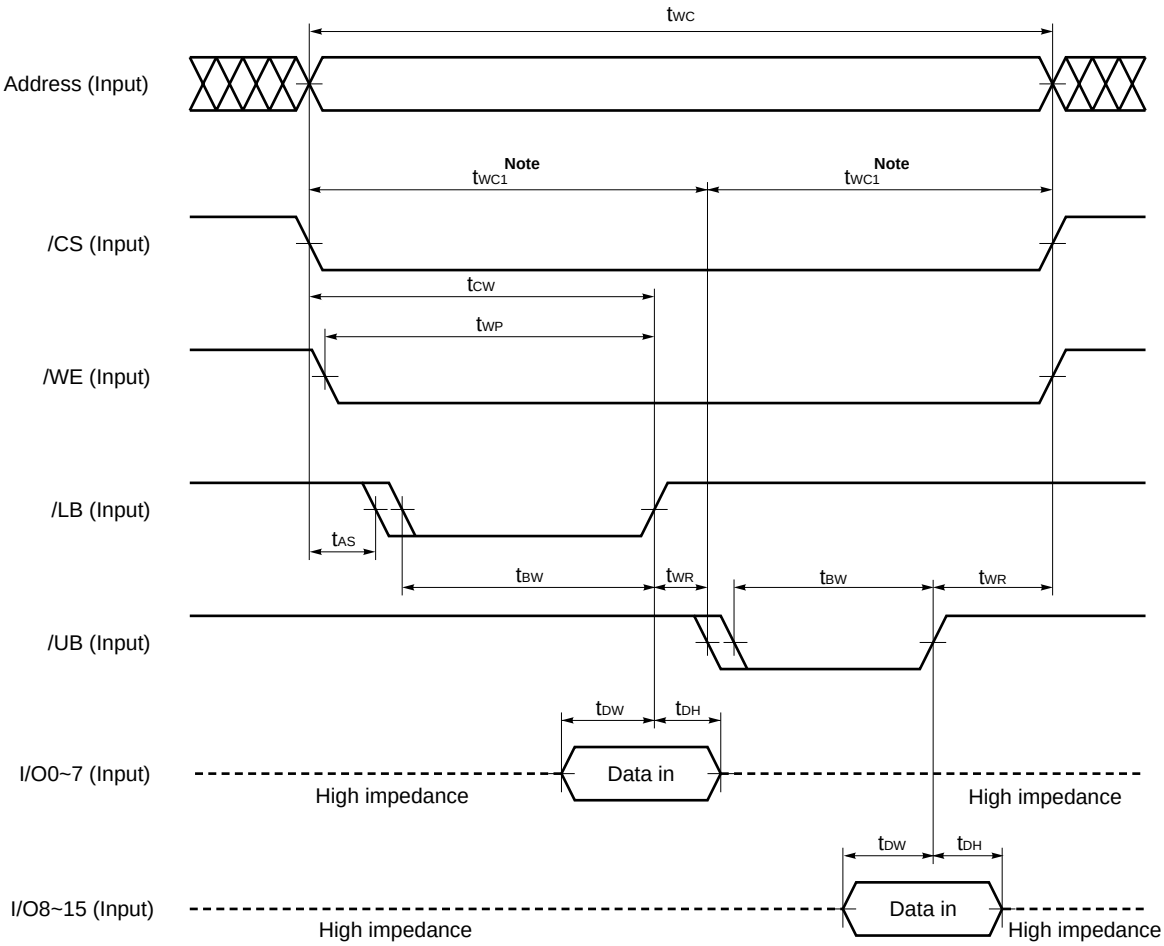
2. Do not input data to the I/O pins while they are in the output state.

3. If the address is changed using a value that is either lower than the minimum value or higher than the maximum value for the write cycle time (t_{WC}), none of the data can be guaranteed.

Note If /LB and /UB are changed at the same time with /CS low level and a continuous write operation toggling /WE is performed, make settings so that the sum (t_{WC}) of the identical address write cycle time (t_{WC1}) is 10 μs or less.

Remark Write operation is done during the overlap time of a Low /CS, /WE, /LB and/or /UB.

Figure 6-19. Write Cycle Timing Chart 6 (/LB, /UB Independent Controlled 1)



Cautions 1. During address transition, at least one of pins /CS, /WE should be inactivated.

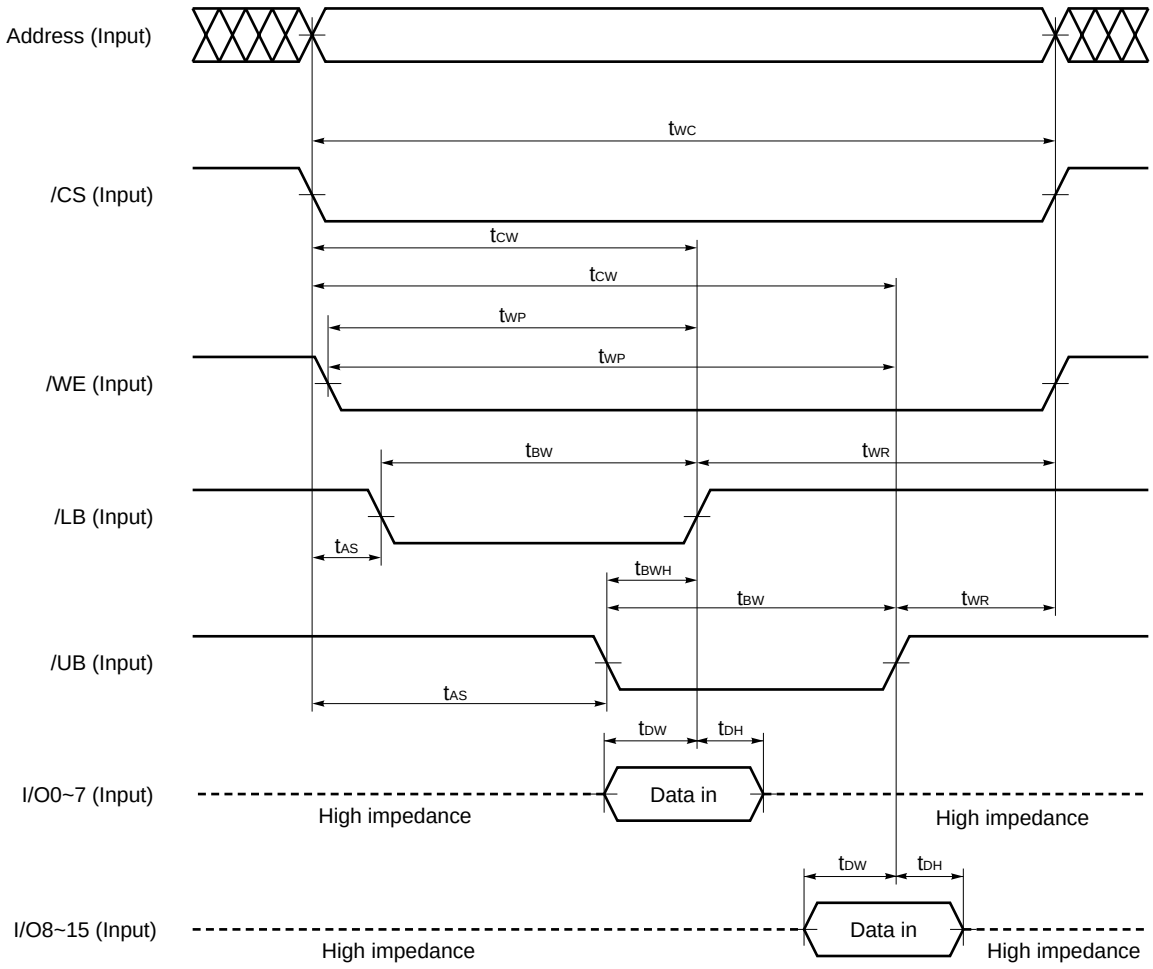
2. Do not input data to the I/O pins while they are in the output state.

3. If the address is changed using a value that is either lower than the minimum value or higher than the maximum value for the write cycle time (t_{WC}), none of the data can be guaranteed.

Note If /LB and /UB are changed at the same time with /CS low level and a continuous write operation toggling /WE is performed, make settings so that the sum (t_{WC}) of the identical address write cycle time (t_{WC1}) is 10 μs or less.

Remark Write operation is done during the overlap time of a Low /CS, /WE, /LB and/or /UB.

Figure 6-20. Write Cycle Timing Chart 7 (/LB, /UB Independent Controlled 2)



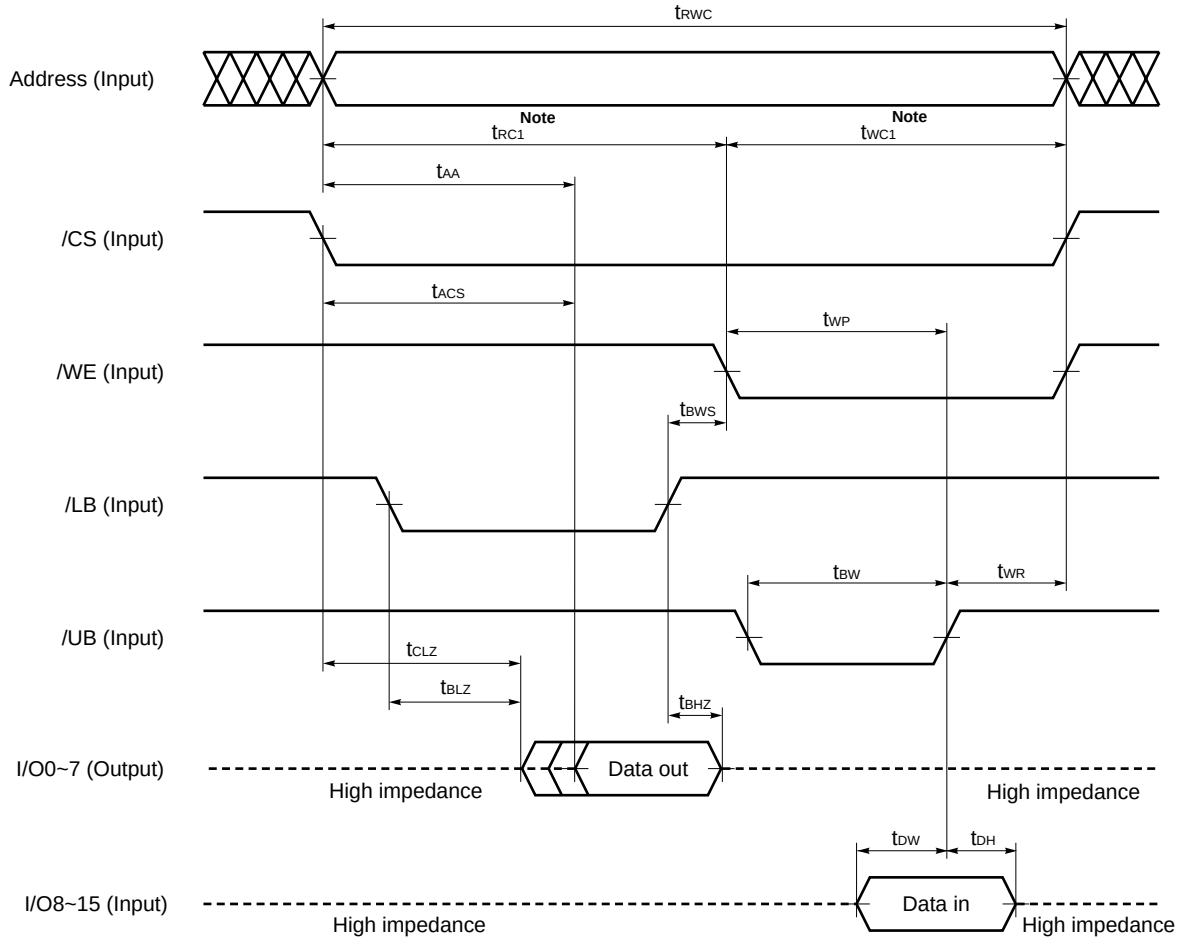
Cautions 1. During address transition, at least one of pins /CS, /WE should be inactivated.

2. Do not input data to the I/O pins while they are in the output state.

3. If the address is changed using a value that is either lower than the minimum value or higher than the maximum value for the write cycle time (t_{WC}), none of the data can be guaranteed.

Remark Write operation is done during the overlap time of a Low /CS, /WE, /LB and/or /UB.

Figure 6-21. Read Write Cycle Timing Chart 1 (/LB, /UB Independent Controlled 1)



Cautions 1. During address transition, at least one of pins /CS, /WE should be inactivated.

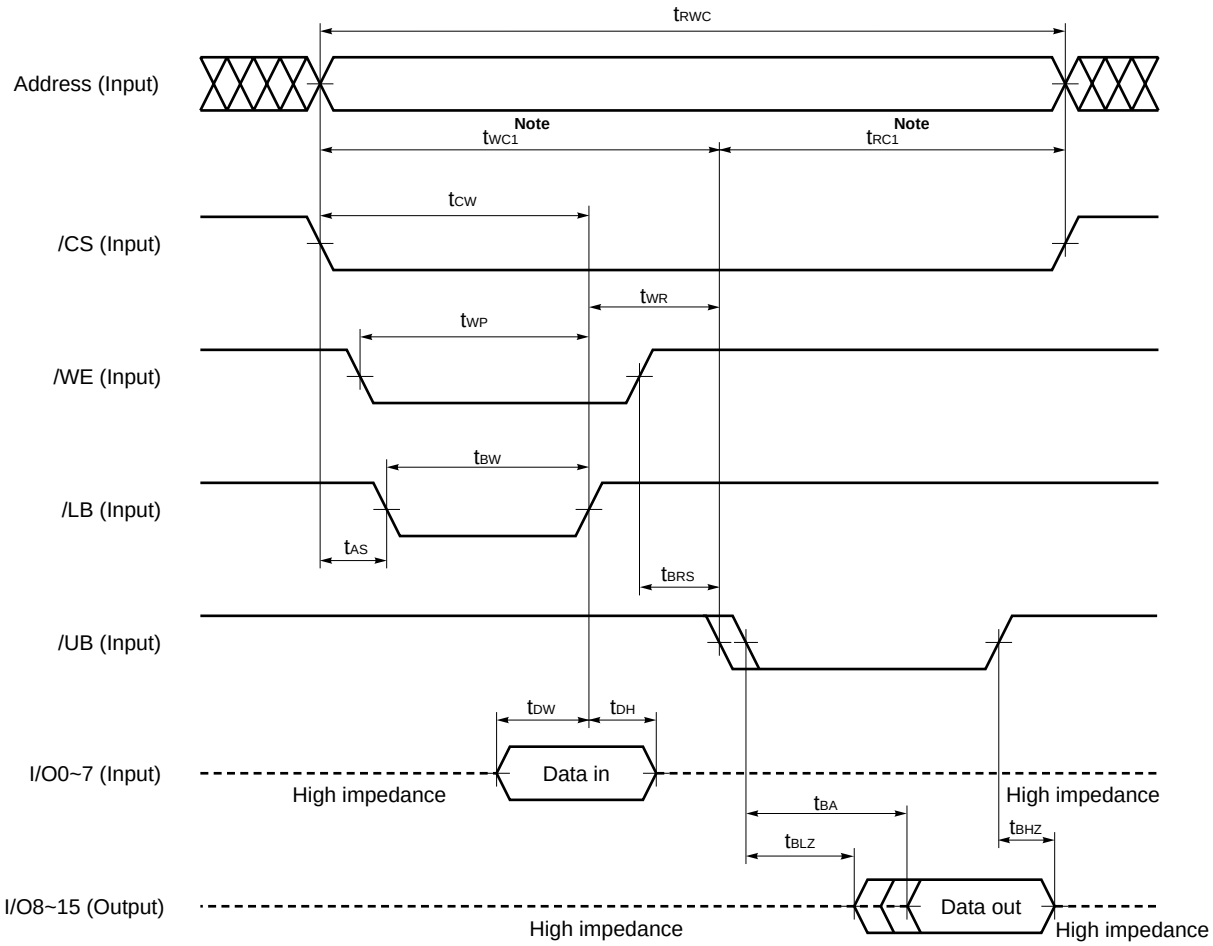
2. Do not input data to the I/O pins while they are in the output state.

3. If the address is changed using a value that is either lower than the minimum value or higher than the maximum value for the identical address read cycle time (t_{RC1}) and the identical address write cycle time (t_{WC1}), none of the data can be guaranteed.

Note Make settings so that the sum (t_{RWC}) of the identical address read cycle time (t_{RC1}) and the identical address write cycle time (t_{WC1}) is 10 μs or less when a write is performed at the identical address using /UB following a read using /LB with /CS low level, or when a write is performed using /LB following a read using /UB.

Remark Write operation is done during the overlap time of a Low /CS, /WE, /LB and/or /UB.

Figure 6-22. Read Write Cycle Timing Chart 2 (/LB, /UB Independent Controlled 2)



Cautions 1. During address transition, at least one of pins /CS, /WE should be inactivated.

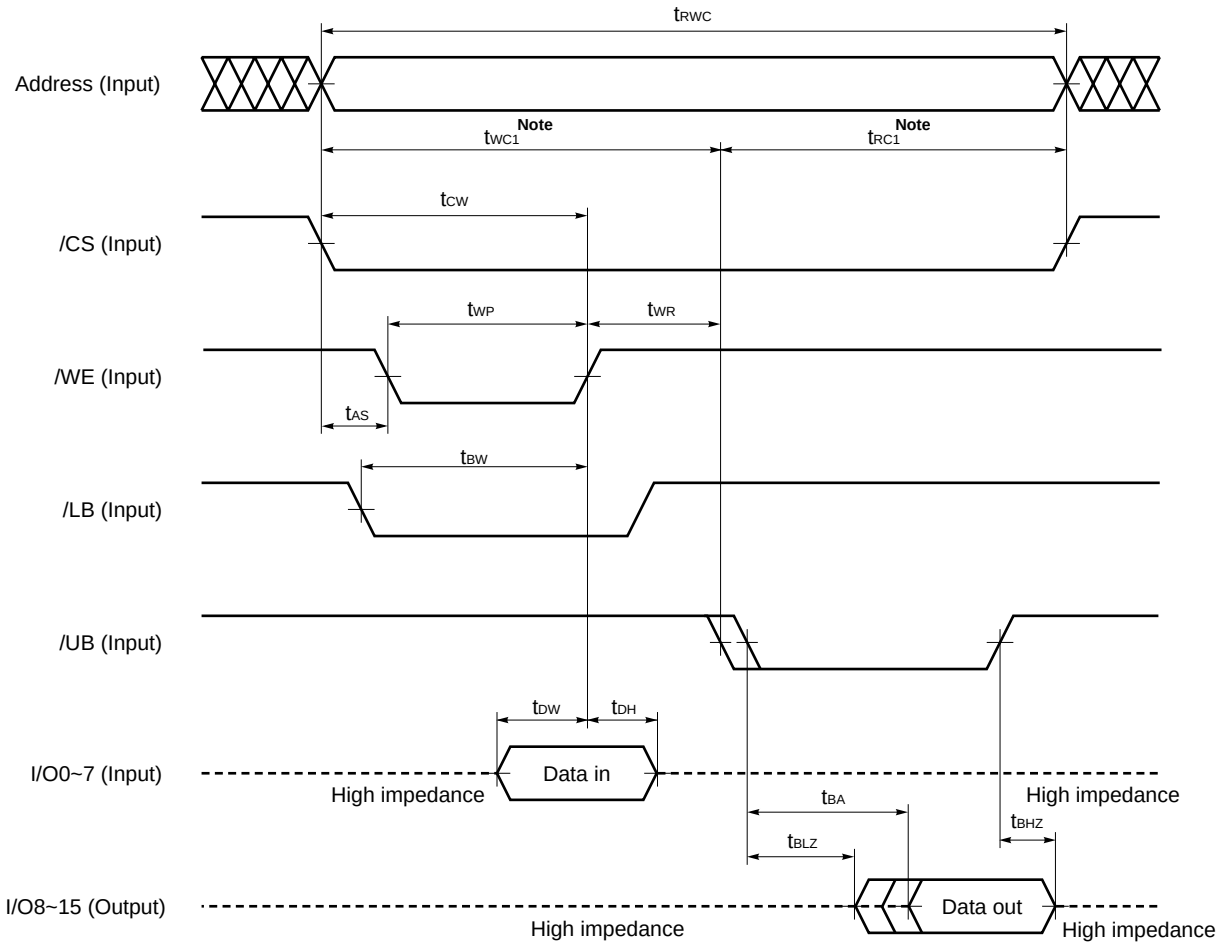
2. Do not input data to the I/O pins while they are in the output state.

3. If the address is changed using a value that is either lower than the minimum value or higher than the maximum value for the identical address read cycle time (t_{RC1}) and the identical address write cycle time (t_{WC1}), none of the data can be guaranteed.

Note Make settings so that the sum (t_{RWC}) of the identical address read cycle time (t_{RC1}) and the identical address write cycle time (t_{WC1}) is 10 μs or less when a write is performed at the identical address using /UB following a read using /LB with /CS low level, or when a write is performed using /LB following a read using /UB.

Remark Write operation is done during the overlap time of a Low /CS, /WE, /LB and/or /UB.

Figure 6-23. Read Write Cycle Timing Chart 3 (/LB, /UB Independent Controlled 3)



Cautions 1. During address transition, at least one of pins /CS, /WE should be inactivated.

2. Do not input data to the I/O pins while they are in the output state.

3. If the address is changed using a value that is either lower than the minimum value or higher than the maximum value for the identical address read cycle time (t_{RC1}) and the identical address write cycle time (t_{WC1}), none of the data can be guaranteed.

Note Make settings so that the sum (t_{RWC}) of the identical address read cycle time (t_{RC1}) and the identical address write cycle time (t_{WC1}) is 10 μs or less when a write is performed at the identical address using /UB following a read using /LB with /CS low level, or when a write is performed using /LB following a read using /UB.

Remark Write operation is done during the overlap time of a Low /CS, /WE, /LB and/or /UB.

Figure 6-24. Mode Register Setting Timing Chart

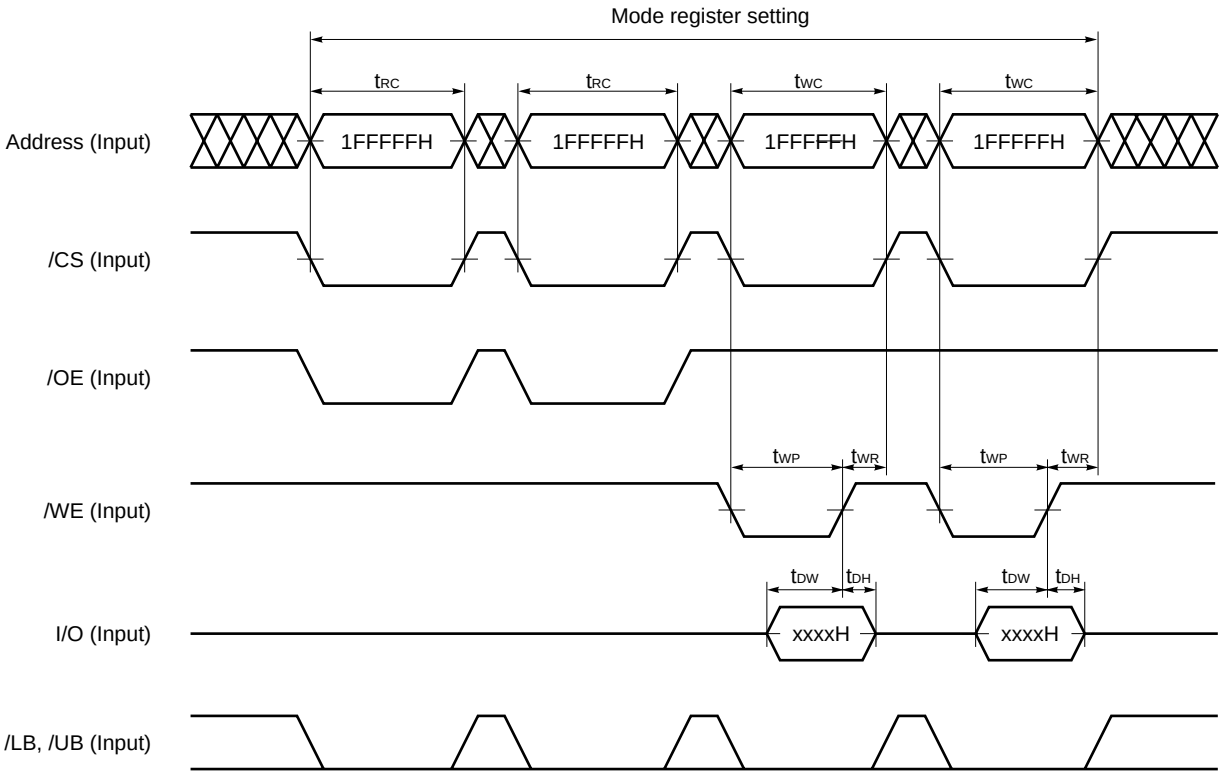
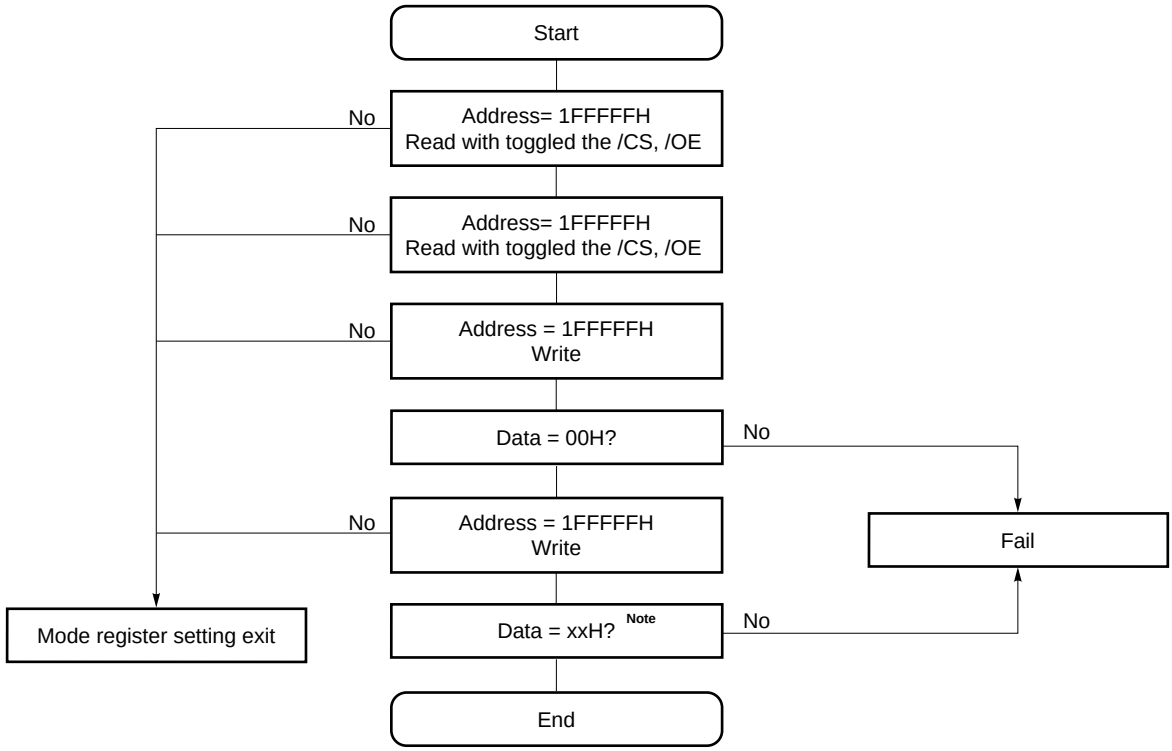


Figure 6-25. Mode Register Setting Flow Chart



Note xxH = 00H, 01H, 02H, 03H, 04H, 05H, 06H, 07H

Figure 6-26. Standby Mode Timing Chart

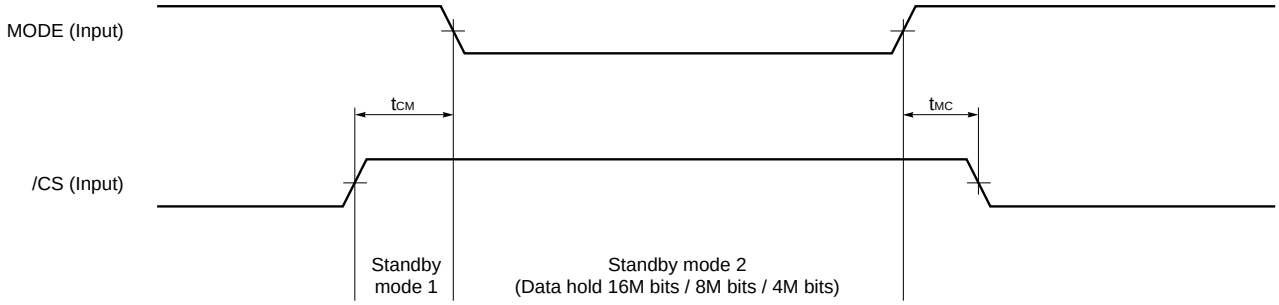
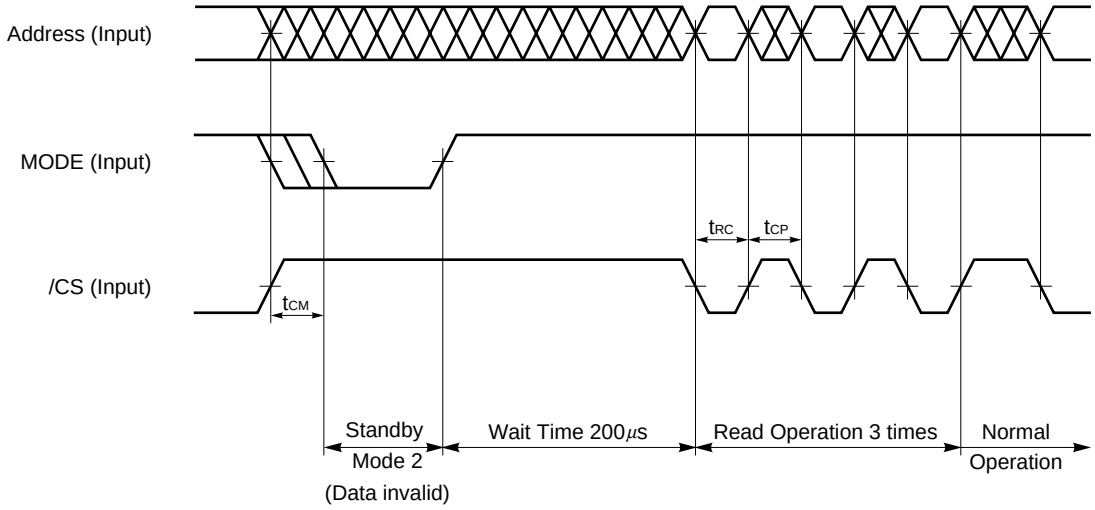
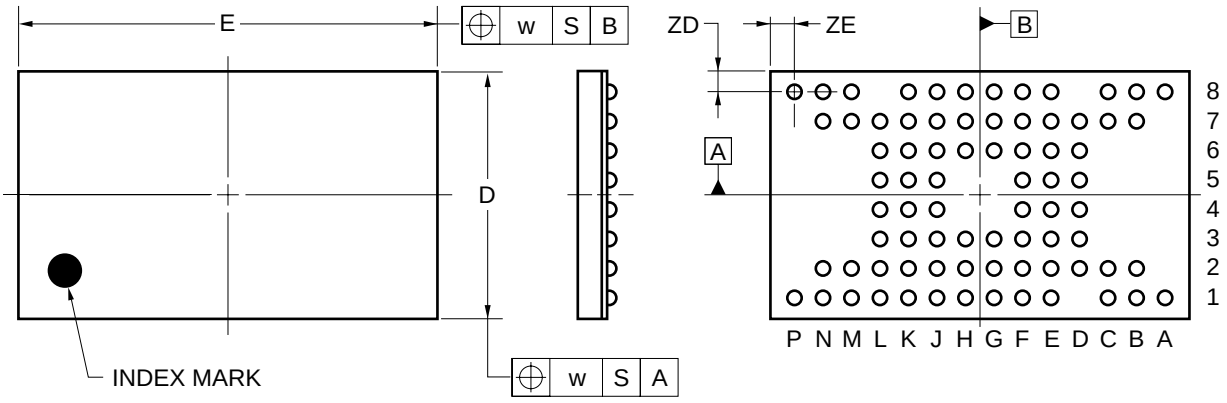


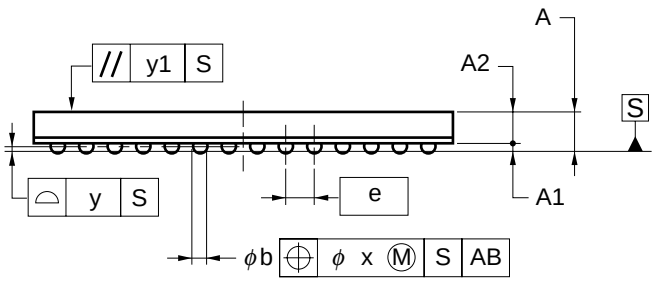
Figure 6-27. Standby Mode 2 (Data Invalid) Entry / Recovery Timing Chart



7. Package Drawing

77-PIN TAPE FBGA (12x7)





ITEM	MILLIMETERS
D	7.0±0.1
E	12.0±0.1
w	0.2
A	1.1±0.1
A1	0.26±0.05
A2	0.84
e	0.8
b	0.45±0.05
x	0.08
y	0.1
y1	0.1
ZD	0.7
ZE	0.8

P77F9-80-BT3

8. Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the μPD4632312-X.

Types of Surface Mount Device

μPD4632312F9-BxxX-BT3: 77-pin TAPE FBGA (12 x 7)

μPD4632312F9-CxxX-BT3: 77-pin TAPE FBGA (12 x 7)

μPD4632312F9-BExxX-BT3: 77-pin TAPE FBGA (12 x 7)

μPD4632312F9-CExxX-BT3: 77-pin TAPE FBGA (12 x 7)

9. Revision History

Edition/ Date	Page		Type of revision	Location	Description (Previous edition → This edition)
	This edition	Previous edition			
6th edition/ Jan.2002	Throughout		Modification		Preliminary Data Sheet → Data Sheet
	p.9	p.9	Modification	2.4 Addresses for Which Partial Refresh Is Supported	5cross beam → 6cross beam
7th edition/ Mar. 2002	p.4	p.4	Addition	Block Diagram	Note
	p.5	p.5	Modification	Truth Table	Standby Mode 2 : /CS = ×→H Notes 1 revision

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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