

SINGLE-CHIP MICROCONTROLLER

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The μPD17102 is a four-bit single chip microcontroller which has a built-in LCD controller, D/A converter, and operational amplifier. This CPU uses the μPD17000 architecture, allowing data transfer and operation between data memory areas or between data memory areas and peripheral circuits with only one instruction. It also supports 16-bit (1-word) instructions.

FEATURES

- μPD17000 architecture
- Program memory (ROM) : 4K bytes (2048 x 16 bits)
- Data memory (RAM) : 208 words (208 x 4 bits)
- Command execution time : 2.0 μs (8 MHz, ceramic/crystal oscillator)
- Interrupting function (Internal: 3, and external: 2)
- 8-bit timer/counter : 2 channels (built-in modulo)
- 8-bit serial interface
- 2-channel complete CMOS operational amplifier
(Two operation modes available: NORMAL and SAMPLE/HOLD)
- 4-channel multiplexer input comparator
- 6-bit D/A converter
- Feasible to realize the 4-channel 6-bit A/D conversion function using the above-mentioned comparator and D/A converter
- LCD controller/driver
(14SEGMENT x 2COMMON, 13SEGMENT x 3COMMON, and 12SEGMENT x 4COMMON)
- Zero-cross detection selectable
- Standby function (Stop/Halt)

USE:

Electronic rice cooker and blood pressure meter, etc.

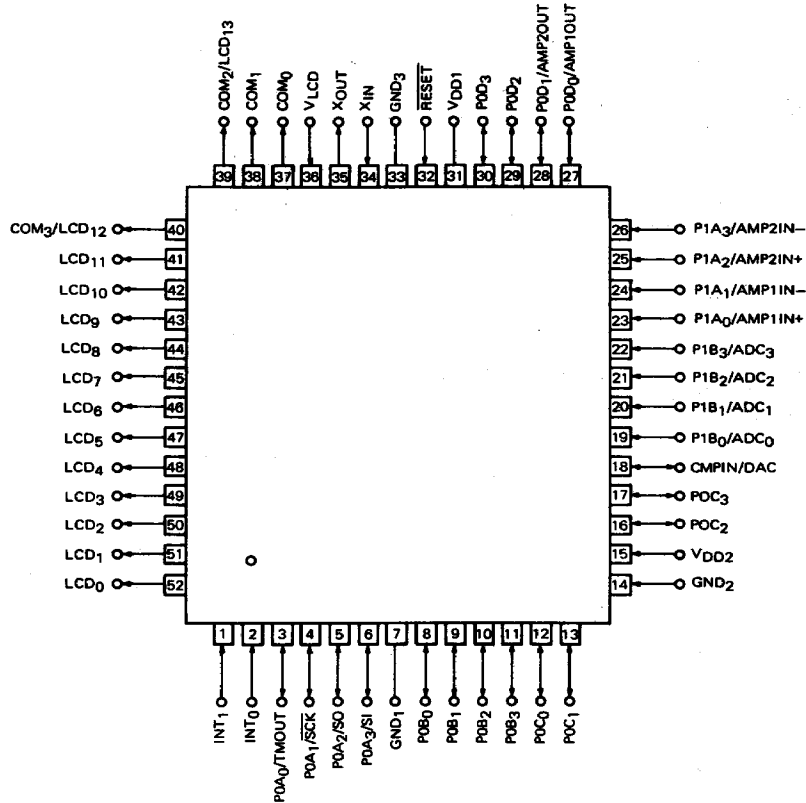
ORDERING INFORMATION

Order Code	Package
μPD17102G-XXX-00	52-pin plastic QFP (bent lead)
μPD17102G-XXX-03	52-pin plastic QFP (straight lead)

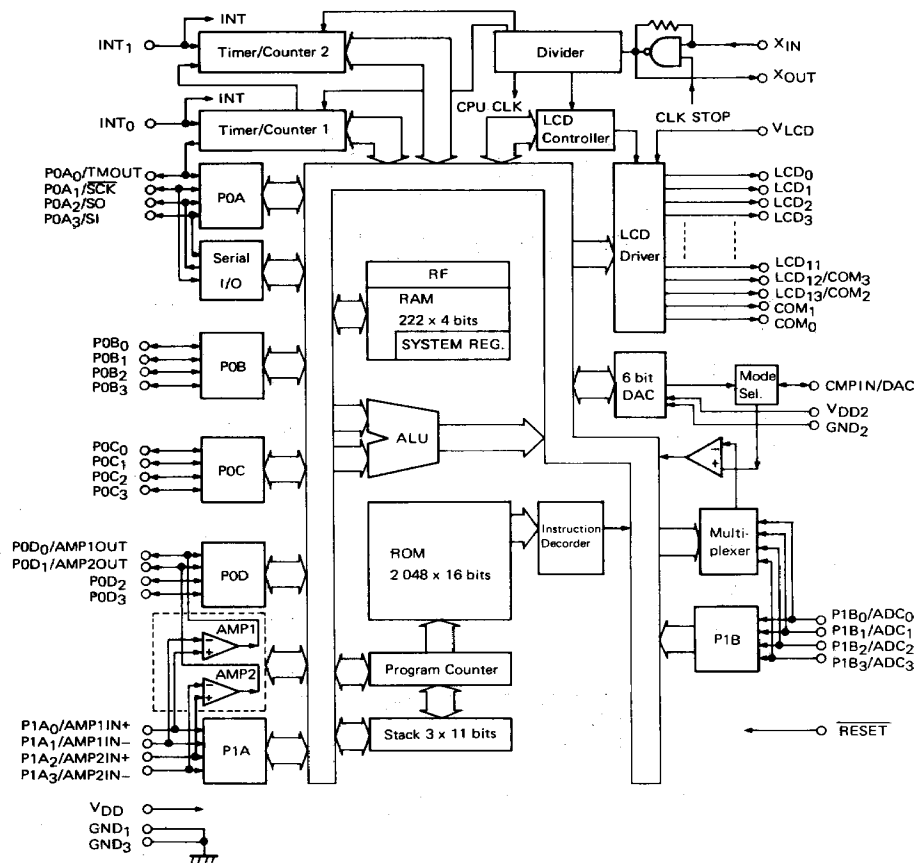
OUTLINE OF FUNCTIONS

- μPD17000 architecture
- Program memory (ROM) : 4K bytes (2048 x 16 bits)
- Data memory (RAM) : 222 words (222 x 4 bits)
- Stack level : 3 levels
- Instruction cycle : 2 μs (when operated at 5.0 V and 8 MHz)
- Interrupting function : (Internal: 3, and external: 2)
- 8-bit timer/counter : 2 CH (with modulo integrated)
- 8-bit serial interface
- 2-channel complete CMOS operational amplifier
(Two operation modes available: NORMAL and SAMPLE/HOLD)
- 4-channel input comparator with multiplexer
- 6-bit D/A converter
- Feasible to realize 4-channel, 6-bit A/D conversion function using the above-mentioned comparator and D/A converter
- LCD controller (14SEGMENT x 2COMMON, 13SEGMENT x 3COMMON, and 12SEGMENT x 4COMMON)
- Zero-cross detecting function
- Standby function (STOP/HALT)
- Data/memory low supply voltage holding function
- Oscillator circuit for system clock (ceramic and crystal)
- Single power unit (3.0 to 6.0 V, but 4.5 to 6.0 V when the operational amplifier is used)

PIN CONFIGURATION (Top View)



BLOCK DIAGRAM



1. OUTLINE

The μPD17102 is a 4-bit single chip microcontroller which integrates all the following circuits on one chip: 4-bit ALU, program memory (ROM), data memory (RAM), I/O ports, timer/event counter, serial interface, vector interrupt circuit.

This chip using the μPD17000 Series architecture has various built-in peripheral circuits including analog circuits, allowing the user to incorporate it into electrical appliances and intelligent units in a distributed system for home automation.

For program development, NEC supports the in-circuit emulator (IE-17K), so that the user can debug programs easily by using the emulator together with the SE board for each product.

2. PIN FUNCTIONS

2.1 Input/Output Ports

2.1.1 P0A₀ to P0A₃ (Port 0A): Bi-directional input/output ports

Port 0A is a 4-bit input port (pins from P0A₀ to P0A₃) with output latch circuits.

This port is mapped to 70H at bank 0 in the data memory space and accessed with normal data memory operation instructions. The direction of input/output is switched for all four bits by the P0AGIO value. Setting P0AGIO to "1" outputs the value stored at 70H of bank 0 to the pin and setting to "0" disables output and sets input mode.

Regardless of the P0AGIO value, the pin status can be read with a data memory reference instruction. The contents of the output latch remain unchanged unless the data at 70H of bank 0 is rewritten.

P0A₀ is shared by the timer 1 output pin TMOUT. It operates as TMOUT when PTOUTON in the register file is "0" and in normal input/output mode.

When TMOUT is selected, this pin outputs "1" at time 1 reset and reverses the output each time the timer 1 value matches the contents of the modulo register. At this time, this pin is set in output mode regardless of the P0AGIO value. The pin status at this time can also be read with a data memory reference instruction. The output latch as P0A₀ is independent of TMOUT, and therefore data can be written to 70H of bank 0 even if the pin operates as TMOUT and the data is output when PTOUTON is set to "0" while P0AGIO is "1."

P0A₁ to P0A₃ are shared by SCK, SO, and SI of the serial interface. The PA0 pin is set in normal input/output mode when the SIOON value in the register file is "0" and used as the SIO pin when it is "1."

In the port 0A input/output format, either of the Nch open/drain input/output or Nch open/drain input/output with a built-in pull-up resistor is selectable by the mask option. In Nch open/drain input/output mode, the port has a 9 V withstanding voltage and is suitable for an interface with a circuit using a different supply voltage. By using the Nch open/drain input/output structure, a 2-wire serial interface can also be used.

When SIOON is "1," data cannot be output to the SCK and SO pins as a port. Even if data is transferred to address 70H of bank 0, this data cannot be input to P0A₁ to P0A₃. At this time, only P0A₃ is available.

When the SCK pin is in input mode, however, data can be written to the P0A₁ output latch.

Table 2-1 Port 0A functions

PTOUTON	SIOON	POAGIO	Write to bank 0, 70H	Read from bank 0, 70H	Pin function			
					POA ₀	POA ₁	POA ₂	POA ₃
0	0	0	All four bits are valid.	Enable. (Pin status)	POA ₀ IN	POA ₁ IN	POA ₂ IN	POA ₃ IN
		1	All four bits are valid.		POA ₀ OUT	POA ₁ OUT	POA ₂ OUT	POA ₃ OUT
	1	0	Only POA ₀ is valid.		POA ₀ IN	SCK	SO	SI
		1	Only POA ₀ is valid.		POA ₀ OUT			
1	0	0	All four bits are valid.		TMOUT	POA ₁ IN	POA ₂ IN	POA ₃ IN
		1	All four bits are valid.			POA ₁ OUT	POA ₂ OUT	POA ₃ OUT
	1	0	Only POA ₀ is valid.			SCK	SO	SI
		1	Only POA ₀ is valid.					

Note: If data is written to 70H of bank 0 when SIOON is "1," this data can be written to POA₁ only when the SCK pin is in input mode.

2.1.2 POB₀ to POB₃ (port 0B), POC₀ to POC₃ (port 0C): Bi-directional input/output

Ports 0B and 0C are 4-bit input/output pins with output latch circuits: From POB₀ to POB₃ and from POC₀ to POC₃. These ports are mapped to 71H and 72H of bank 0 in the data memory space, respectively and are accessed with normal data memory operation instructions like port 0A. The direction of input/output is switched for all 4-bits by the POBGIO or POCGIO value in the register file. Setting the value to "1" outputs the data at 71H or 72H of bank 0 to the corresponding pin and "0" disables the output and sets the input mode. Regardless of the POBGIO and POCGIO values, the pin status is read when a data memory reference instruction is executed. At this time, the contents of the output latch remain unchanged.

The input/output format of ports 0B and 0C is the CMOS (push/pull) type.

Table 2-2 Functions of ports 0B and 0C

POBGIO POCGIO	Input/output direction of pin	Write to bank 0, 71H or 72H	Read from bank 0, 71H or 72H
0	Input (output disable)	Available	Available (pin status input)
1	Output		

2.1.3 P0D₀ to P0D₃ (port D): Bi-directional input/output

Port 0D comprises 4-bit input/output pins with output latch circuits. It is mapped to 73H of bank 0 in the data memory space. The input/output direction is switched by the P0DGIO value in the register file.

P0D₀ is shared with the AMP1 output pin AMP1OUT, and P0D₁ is shared with the AMP2 output pin AMP2OUT. These bits are used in normal input/output mode when the AMP1EN or AMP2EN values in the register file are "0" and as AMP1OUT and AMP2OUT respectively when the values are "1."

When AMP1OUT and AMP2OUT are selected, the pins are used as the AMP1OUT and AMP2OUT output pins, regardless of the P0DGIO value. A data memory reference instruction reads the pin status regardless of the function selected for the pin. At this time, the pin potential is intermediate, the read value is undefined. The μPD17102 reads only at the moment the instruction is executed and disables other input circuits. Therefore, the through current does not flow through the input circuit.

The P0D₀ and P0D₁ output latch circuits are independent of AMP1OUT and AMP2OUT. Therefore, data can be written to bank 0, 73H by setting AMP1EN and AMP2EN to "1" even if the pins operate as AMP1OUT and AMP2OUT. When P0DGIO is "1," the pins output data as a port by setting AMP1EN and AMP2EN to "0."

The port 0D input/output format is CMOS (push/pull) input/output.

Table 2-3 Port 0D functions

AP1EN AP2EN	P0DGIO	Write to bank 0, 73H	Read from bank 0, 73H	Pin function			
				P0D ₀	P0D ₁	P0D ₂	P0D ₃
0	0	All four bits are valid.	Enable. Pin status.	P0D ₀ IN	P0D ₁ IN	P0D ₂ IN	P0D ₃ IN
	1			P0D ₀ OUT	P0D ₁ OUT	P0D ₂ OUT	P0D ₃ OUT
1	0			AMP1OUT	AMP2OUT	P0D ₂ IN	P0D ₃ IN
	1					P0D ₂ OUT	P0D ₃ OUT

Note: The AMP output control is selectable for AMP1/2 separately.

2.1.4 P1A₀ to P1A₃ (port 1A): Input

Port 1A comprises 4-bit input pins.

It is mapped to 70H of bank 1 in the data memory space.

P1A₀ and P1A₁ are shared with AMP1 non-reverse input (AMP1IN+) and reverse input (AMP1IN-), P1A₂ and P1A₃ are shared with AMP2 non-reverse input (AMP2IN+) and reverse input (AMP2IN-). These pins are not switched and are always connected to both input circuits of the operator amplifier (analog input) and port (digital input).

When used as analog input pins, apply an intermediate potential or AC voltage. If a data memory reference instruction is executed at this time, an undefined value is read. Similar to port 0D, the through current does not flow through the input circuit.

Port 1A has three mask options: With pull-up resistor, with pull-down resistor, and with no built-in resistor. When the pins are used as analog input pins, select the mask option for no built-in resistor. Otherwise, the pins may not operate normally.

Output instructions to the port (data write to 70H in bank 1) are invalid.

Table 2-4 Port 1A function

Read from bank 1, 70H (logical input)	Write to bank 1, 70H	Analog input
Enable (Pin status input) (Undefined at intermediate potential)	Disable	Always connected to AMP input.

2

2.1.5 P1B₀ to P1B₃ (port 1B): Input

Port 1B comprises 4-bit input pins.

It is mapped to 71H of bank 1 in the data memory space.

Only one of these pins can be set as the input pin of the non-reserve input from the comparator by ADCCH0 and ADCCH1. For more information, see Section 3.12. Similar to ports 0D and 1A, the pin status of port 1B is read with the data memory reference instruction, regardless of the selected pin function, and the through current does not flow through the input circuit even if the intermediate potential is applied.

Port 1B also has three mask options: With pull-up resistor, with pull-down resistor, and with no built-in resistor. When the pins are used as analog input pins, select the mask option for no built-in resistor. Otherwise, the pins may not operate normally.

Output instructions to port 1B (data write to 71H in bank 1) are invalid.

Table 2-5 Port 1B function

Read from bank 1, 71H (logical input)	Write to bank 1, 71H	Analog input
Enable (Pin status input) (Undefined at intermediate potential)	Disable	Either pin is connected to the comparator input (by ADCCH0 and ADCCH1).

2.2 INT₀, INT₁

INT₀ and INT₁ are interrupt request input pins for which the active rising or falling edge is selectable by IEG₀ and IEG₁. At the rising or falling edge of the INT₀ or INT₁ signal selected by IEG₀ and IEG₁, the interrupt request flag (IRQ0, IRQ1) is set.

To prevent malfunctions from noise, the pins have a built-in noise remover. The status of the pin for which noise is eliminated by the noise remover is read by referencing INT₀ and INT₁ in the register file with the PEEK instruction, so that the pins are simply used as input pins.

In addition, INT₀/INT₁ are the count clock input pins of timer 1/2, respectively, and are used when external clocks are selected as timer count clock sources. When sharing the timer input and INT₀/INT₁ interrupt request input, note that the INT₀/INT₁ interrupt request flag is also set by the clock.

The INT₁ pin is also used to detect zero-cross when ZCROSS in the register file is set to "1."

2.3 CMPIN/DAC, VDD2, GND2

VDD2 and GND2 are pins used to apply the reference voltage of the built-in 6-bit D/A converter. Apply the VDD potential to VDD2 and the GND potential to GND2. These two pins are separated from VDD and GND and can have separated digital and analog power sources. The applied voltage between the pins is divided into 2⁶ steps (64 steps). The analog value corresponding to digital data stored in four bits of 72H and high-order two bits of 73H of bank 1 in the data memory space is the D/A converter output.

To output the D/A converter data from the CMPIN/DAC pin, set DACEN to "1" and CMPEN to "0" in the register file.

To use a comparator, set DACEN to "0" and CMPEN to "1" in the register file. At this time, the CMPIN/DAC pin operates as the reverse input pin of the comparator (CMPIN). Apply a voltage with the same potential as V_{DD} to the V_{DD2} pin. Also apply the same potential to GND_2 pin to minimize the current flowing through the D/A converter which is not used.

When using the 6-bit D/A converter under program control, set DACEN to "1" and CMPEN to "1" in the register file. At this time, D/A converter data is not output externally, but is directly input to the comparator reverse input pin. Therefore, the CMPIN/DAC pin is not used.

Table 2-6 V_{DD2} , GND_2 , and CMPIN/DAC functions

DACEN	CMPEN	V_{DD2}	GND_2	CMPIN/DAC	Function
0	0	V_{DD} potential	V_{DD} potential	V_{DD} potential	D/A converter and comparator are not used.
		V_{DD2}	GND_2	High impedance	Initial state when the D/A converter is used (Note).
0	1	V_{DD} potential	V_{DD} potential	CMPIN	When the comparator is used.
1	0	V_{DD2}	GND_2	DAC	When the D/A converter is used.
1	1	V_{DD2}	GND_2	V_{DD} potential	Used as D/A converter

V_{DD} potential indicates that V_{DD} potential is applied externally.

Note: DACEN and CMPEN are set to "0" at reset.

2.4 V_{LCD}

V_{LCD} is a power supply pin for driving the liquid crystal display panel (LCD panel).

Depending on the bias method used, it generates the $1/2 V_{LCD}$, $1/3 V_{LCD}$, and $2/3 V_{LCD}$ voltages. When using LCD_0 to LCD_{13} as the output pins, apply the high voltage under the supply voltage (V_{DD}).

2.5 LCD_0 to LCD_{11} , COM_3/LCD_{12} , COM_2/LCD_{13} , COM_1 , COM_0

LCD_0 to LCD_{11} , COM_3 , LCD_{12} , COM_2/LCD_{13} , COM_1 , and COM_0 are LCD panel segment driver pins used to select drive method, such as 14-segment 2-common, 13-segment 3-common, 12-segment 4-common.

LCD_0 to LCD_{13} are used as output pins when LCDEN in the register file is "0." At this time, COM_1 and COM_0 are not used.

For more information on the LCD panel, see Section 3.10.

Table 2-7 LCD_0 to LCD_{11} , COM_3/LCD_{12} , COM_2/LCD_{13} , COM_1 , and COM_0 functions

LCDEN	LCD_0 to LCD_{11} , COM_3/LCD_{12} , COM_2/LCD_{13}	COM_1 , COM_0
0	All are output pins.	Not used
1	LCD drivers and common drivers	Common drivers

2.6 X_{IN} , X_{OUT}

X_{IN} and X_{OUT} are pins used to connect the oscillation vibrator in the system clock generator.

2.7 $\overline{RESET}$

$\overline{RESET}$ is a low-level active reset input pin. The reset has priority over all other operations. In addition to CPU initial start, this pin is also used to release standby mode.

2.8 V_{DD1}

V_{DD1} is a positive power supply pin.

2.9 GND₁, GND₂

GND₁ and GND₂ are GND potential pins. Wire them so that the same potential is used externally.

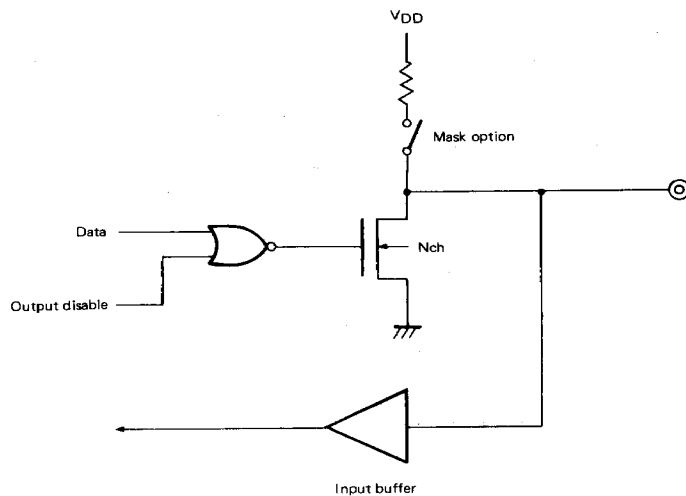
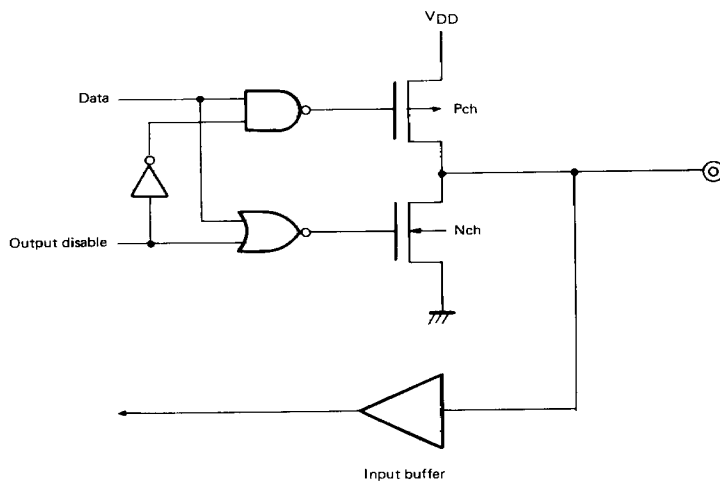
2.10 Pin Mask Options

The μPD17102 pins have the mask options listed below. These option can be selected bit according to purpose.

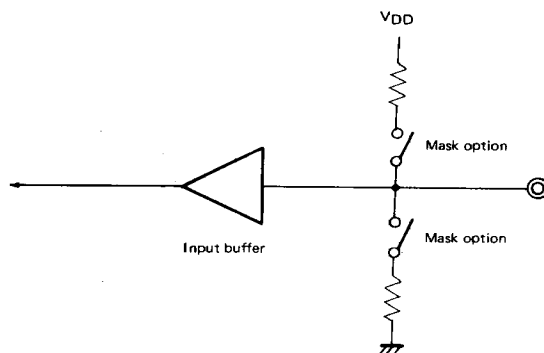
Pin name	Mask option
P0A ₀ to P0A ₃	(1) Nch open-drain input/output (2) Nch open-drain plus built-in pull-up resistor input/output
P1A ₀ to P1A ₃ P1B ₀ to P1B ₃	(1) No built-in resistor (2) Built-in pull-up resistor (3) Built-in pull-down resistor
INT ₀ INT ₁	(1) No built-in resistor (2) Built-in pull-up resistor (3) Built-in pull-down resistor
RESET	(1) No built-in resistor (2) Built-in pull-up resistor

2.11 Pin Input/Output Circuits

The Input/output circuit of each pin of the μ PD17102 is shown below in a partly simplified format:

(1) P0A₀ to P0A₃(2) P0B₀ to P0B₃, P0C₀ to P0C₃, P0D₀ to P0D₃

(3) P1A₀ to P1A₃, P1B₀ to P1B₃, INT₀, INT₁



(4) RESET

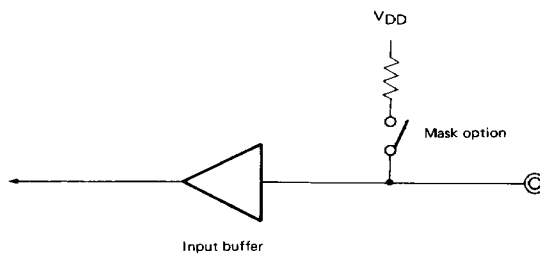


Table 2-8 Digital input/output port pin functions

PIN NAME	I/O	COMBINED USE	FUNCTION	WHEN RESET
POA ₀	Input/output	TMOUT	4-bit I/O port (port 0A)	High impedance (POAn input)
POA ₁		SCK		
POA ₂		SO		
POA ₃		SI		
POB ₀ to POB ₃	Input/output		4-bit I/O port (port 0B) Large current (15 mA)	High impedance (input)
POC ₀ to POC ₃	Input/output		4-bit I/O port (port 0C) Large current (15 mA)	High impedance (input)
POD ₀	Input/output	AMP1OUT	4-bit I/O port (port 0D) Middle current (10 mA)	High impedance (PODn input)
POD ₁		AMP2OUT		High impedance (input)
POD ₂ to POD ₃				
P1A ₀	Input	AMP1IN+	4-bit input port (port 1A)	Input
P1A ₁		AMP1IN-		
P1A ₂		AMP2IN+		
P1A ₃		AMP2IN-		
P1B ₀	Input	ADC ₀	4-bit input port (port 1B)	Input
P1B ₁		ADC ₁		
P1B ₂		ADC ₂		
P1B ₃		ADC ₃		

Table 2-9 Pins other than port pins

Pin name	Input/output	Shared	Function	At reset
INT ₀	Input		Used as both the timer 1 count clock input pin and the external interrupt input pin.	Input
INT ₁	Input		Used as the timer 2 count clock input pin and external interrupt input pin. Zero-cross detection function is selectable.	Input
TMOUT	Output	P0A ₀	Timer 1 output pin	P0A ₀ input
SCR	Input/output	P0A ₁	Serial clock input/output pin	P0A ₁ input
SO	Output	P0A ₂	Serial data output pin	P0A ₂ input
SI	Input	P0A ₃	Serial data input pin	P0A ₃ input
AMP1OUT	Output	P0D ₀	AMP1 output pin	P0D ₀ input
AMP2OUT		P0D ₁	AMP2 output pin	P0D ₁ input
AMP1IN+	Input	P1A ₀	AMP1 non-reversed input pin	Input
AMP1IN-		P1A ₁	AMP1 reversed input pin	
AMP2IN+		P1A ₂	AMP2 non-reversed input pin	
AMP2IN-		P1A ₃	AMP2 reversed input pin	
ADC ₀ to ADC ₃	Input	P1B ₀ to P1B ₃	Comparator input pin	Input
V _{DD2}	Input		D/A converter reference voltage input pin (high-potential side)	
GND ₂	Input		D/A converter reference voltage input pin (low-potential side)	
CMPIN	Input/output	DAC	Used as the D/A converter output pin and comparator input pin.	High impedance
LCD ₀ to LCD ₁₁	Output		LCD segment driver output pin. Also used as the output port.	Output
COM ₃	Output	LCD ₁₂	Used as the LCD common driver output and LCD segment driver pin. Also used as an output port.	Output
COM ₂		LCD ₁₃		
COM ₀ , COM ₁	Output		LCD common driver output pin	Output
V _{LCD}	Input		LCD driver split potential setting pin	Input
RESET	Input		System reset input pin	Input
V _{DD1}			Positive power supply pin	
GND ₁ , GND ₃			GND potential pin	
X _{IN} , X _{OUT}			System clock oscillator pin	

3. INTERNAL BLOCK

3.1 Program Counter (PC)

The program counter (PC) is an 11-bit binary counter that retains address data of the program memory (ROM).

Fig. 3-1 Program counter configuration

PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
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When the RESET signal goes to low, the PC is set to 0.

Usually, the counter is incremented by one each time an instruction is executed.

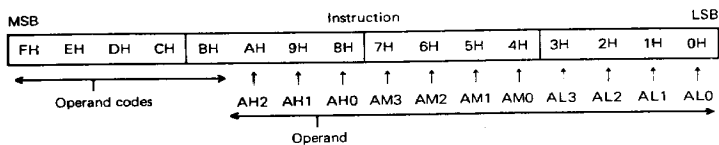
The CALL instruction saves the contents of the counter (return address) to the stack memory then loads the branch destination address to the counter. Return instructions (RET, RETSK, and RETI) load the contents of the stack memory (return address) to the counter. The branch instruction (BR) loads the branch destination address to the counter. The ROM data reference instruction (MOVT) temporarily loads the address at which the data to be referenced is stored to the counter. Take care with the level because the contents of the PC are saved to the stack memory immediately before the address is loaded.

In Fig. 3-2, AHn, AMn, and ALn are addresses indicated by the instruction operand. (See Fig. 3-3.) ARmm is bit n in the address register (ARm) which contains the address to be loaded to the program counter. SP is the stack pointer which points to the contents of the stack memory.

Fig. 3-2 Relationship between instructions and values to be loaded

	PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
RET, RETSK, RETI	(SP)	(SP)	(SP)	(SP)	(SP)	(SP)	(SP)	(SP)	(SP)	(SP)	(SP)
BR, CALL	AH2	AH1	AH0	AM3	AM2	AM1	AM0	AL3	AL2	AL1	AL0
BR@AR, CALL@AR, MOVT	1	1	1	AR13	AR12	AR11	AR10	AR03	AR02	AR01	AR00

Fig. 3-3 Instruction word configuration



7. ASSEMBLER RESERVED WORDS

7.1 Mask Option Pseudo Instructions

For coding μPD17102 programs, a mask option must be specified in Assembler source programs with the mask option pseudo instruction.

The following pins require the mask option:

- P0A₀, P0A₁, P0A₂, P0A₃
- P1A₀, P1A₁, P1A₂, P1A₃
- P1B₀, P1B₁, P1B₂, P1B₃
- INT₀, INT₁
- RESET

7.1.1 OPTION and ENDOP pseudo instructions

From the OPTION pseudo instruction to the ENDOP pseudo instruction is referred to as the mask option definition block. The format of this block is shown below.

Only the six pseudo instructions explained in Section 7.1.2 can be input to the mask option definition block.

Format:

Symbol field	Mnemonic field	Operand field	Comment field
[level:]	OPTION		[comment:]
	⋮		
	ENDPOP		

7.1.2 Mask option definition pseudo instructions

Table 7-1 lists the pseudo instruction that are allowed in the mask option definition block.

An example for defining the mask option is shown below.

Format:

Symbol field	Mnemonic field	Operand field
[level:]	OPTP1A	P1APLUP, P1APLDW, OPEN, OPEN
		→ P1A₃ is pull-up. → P1A₁ and P1A₀ are open.
		→ P1A ₂ is pull-down.

Table 7-1 Mask option definition pseudo instructions

Pin name	Mask option pseudo instruction	Number of parameters	Parameter name
P0A ₀ to P0A ₃	OPTP0A	4	P0APLUP : Pull up OPEN : Open
P1A ₀ to P1A ₃	OPTP1A	4	P1APLUP : Pull up P1APLDW : Pull down OPEN : Open
P1B ₀ to P1B ₃	OPTP1B	4	P1BPLUP : Pull up P1BPLDW : Pull down OPEN : Open
INT ₀	OPTINT0	1	INT0PLUP : Pull up INT0PLDW : Pull down OPEN : Open
INT ₁	OPTINT1	1	INT1PLUP : Pull up INT1PLDW : Pull down OPEN : Open
RESET	OPTRES	1	RESPLUP : Pull up OPEN : Open

7.2 Reserved Symbols

Table 7-2 lists the symbols defined in the μPD17102 device file. These defined symbols include the control register names, port names, and peripheral device names.

(1) Control registers in register file

The names of the control register assigned to data memory addresses 80H to BFH in bank 0 are defined. These registers are accessible through the window register (WR) with the PEEK and POKE instructions.

(2) Registers and ports in data memory

Registers assigned to data memory addresses 00H to 7FH, and ports and system registers assigned to 70H and after are defined.

(3) Peripheral circuits

Peripheral circuits accessible with the GET and PUT D/A converters are defined.

Table 7-2 List of reserved symbols (1/4)

NAME	ATTRIBUTE	VALUE	R/W	DESCRIPTION
DBF3	MEM	0.0CH	R/W	Bit 15 to bit 12 of data buffer
DBF2	MEM	0.0DH	R/W	Bit 11 to bit 8 of data buffer
DBF1	MEM	0.0EH	R/W	Bit 7 to bit 4 of data buffer
DBF0	MEM	0.0FH	R/W	Bit 3 to bit 0 of data buffer
AR3	MEM	0.74H	R	Bit 15 to bit 12 of address register
AR2	MEM	0.75H	R	Bit 11 to bit 8 of address register
AR1	MEM	0.76H	R/W	Bit 7 to bit 4 of address register
AR0	MEM	0.77H	R/W	Bit 3 to bit 0 of address register
WR	MEM	0.78H	R/W	Window register
BANK	MEM	0.79H	R/W	Bank register
IXH	MEM	0.7AH	R/W	Bit 11 to bit 8 of index register
MPH	MEM	0.7AH	R/W	Bit 7 to bit 4 of memory pointer
MPE	FLG	0.7AH.3	R/W	Memory pointer enable flag
IXM	MEM	0.7BH	R/W	Bit 7 to bit 4 of index register
MPL	MEM	0.7BH	R/W	Bit 3 to bit 0 of memory pointer
IXL	MEM	0.7CH	R/W	Bit 3 to bit 0 of index register
RPH	MEM	0.7DH	R/W	Bit 7 to bit 4 of register pointer
RPL	MEM	0.7EH	R/W	Bit 3 to bit 0 of register pointer
PSW	MEM	0.7FH	R/W	Program status word
BCD	FLG	0.7EH.0	R/W	BCD operation flag
CMP	FLG	0.7FH.3	R/W	Compare flag
CY	FLG	0.7FH.2	R/W	Carry flag
Z	FLG	0.7FH.1	R/W	Zero flag
IXE	FLG	0.7FH.0	R/W	Index register enable flag
LCDD0	MEM	0.60H	R/W	LCD segment 0
LCDD1	MEM	0.61H	R/W	LCD segment 1
LCDD2	MEM	0.62H	R/W	LCD segment 2
LCDD3	MEM	0.63H	R/W	LCD segment 3
LCDD4	MEM	0.64H	R/W	LCD segment 4
LCDD5	MEM	0.65H	R/W	LCD segment 5
LCDD6	MEM	0.66H	R/W	LCD segment 6

Table 7-2 List of reserved symbols (2/4)

NAME	ATTRIBUTE	VALUE	R/W	DESCRIPTION
LCDD7	MEM	0.67H	R/W	LCD segment 7
LCDD8	MEM	0.68H	R/W	LCD segment 8
LCDD9	MEM	0.69H	R/W	LCD segment 9
LCDD10	MEM	0.6AH	R/W	LCD segment 10
LCDD11	MEM	0.6BH	R/W	LCD segment 11
LCDD12	MEM	0.6CH	R/W	LCD segment 12
LCDD13	MEM	0.6DH	R/W	LCD segment 13
P0A0	FLG	0.70H.0	R/W	Port 0A bit 0
P0A1	FLG	0.70H.1	R/W	Port 0A bit 1
P0A2	FLG	0.70H.2	R/W	Port 0A bit 2
P0A3	FLG	0.70H.3	R/W	Port 0A bit 3
P0B0	FLG	0.70H.0	R/W	Port 0B bit 0
P0B1	FLG	0.71H.1	R/W	Port 0B bit 1
P0B2	FLG	0.71H.2	R/W	Port 0B bit 2
P0B3	FLG	0.71H.3	R/W	Port 0B bit 3
P0C0	FLG	0.71H.0	R/W	Port 0C bit 0
P0C1	FLG	0.72H.1	R/W	Port 0C bit 1
P0C2	FLG	0.72H.2	R/W	Port 0C bit 2
P0C3	FLG	0.72H.3	R/W	Port 0C bit 3
P0D0	FLG	0.73H.0	R/W	Port 0D bit 0
P0D1	FLG	0.73H.1	R/W	Port 0D bit 1
P0D2	FLG	0.73H.2	R/W	Port 0D bit 2
P0D3	FLG	0.73H.3	R/W	Port 0D bit 3
P1A0	FLG	1.70H.0	R	Port 1A bit 0
P1A1	FLG	1.70H.1	R	Port 1A bit 1
P1A2	FLG	1.70H.2	R	Port 1A bit 2
P1A3	FLG	1.70H.3	R	Port 1A bit 3
P1B0	FLG	1.71H.0	R	Port 1B bit 0
P1B1	FLG	1.71H.1	R	Port 1B bit 1
P1B2	FLG	1.71H.2	R	Port 1B bit 2
P1B3	FLG	1.71H.3	R	Port 1B bit 3
DARH	MEM	1.72H	R/W	D/A conversion data bit 4 and bit 5

Table 7-2 List of reserved symbols (3/4)

NAME	ATTRIBUTE	VALUE	R/W	DESCRIPTION
DARL	MEM	1.73H	R/W	D/A conversion data bit 3 to bit 0
DACCMP	FLG	1.73H.0	R	Result of comparison
SP	MEM	0.81H	R/W	Stack pointer
SIOTS	FLG	0.82H.3	R/W	SIO operating status
SIOHIZ	FLG	0.82H.2	R/W	Status of SO pin
SIOCK1	FLG	0.82H.1	R/W	Selection of serial clock
SIOCK0	FLG	0.82H.0	R/W	Selection of serial clock
INT1	FLG	0.8FH.2	R	Status of INT ₁ pin
INT0	FLG	0.8FH.1	R	Status of INT ₀ pin
ZCROSS	FLG	0.8FH.0	R/W	Status of zero-cross detection circuit
TM1EN	FLG	0.91H.3	R/W	Timer 1 permit
TM1RES	FLG	0.91H.2	R/W	Timer 1 reset
TM1CK1	FLG	0.91H.1	R/W	Timer 1 clock selection
TM1CK0	FLG	0.91H.0	R/W	Timer 1 clock selection
TM2EN	FLG	0.92H.3	R/W	Timer 2 permit
TM2RES	FLG	0.92H.2	R/W	Timer 2 reset
TM2CK1	FLG	0.92H.1	R/W	Timer 2 clock selection
TM2CK0	FLG	0.92H.0	R/W	Timer 2 clock selection
IEG1	FLG	0.9FH.2	R/W	INT1 edge selection
IEG0	FLG	0.9FH.1	R/W	INT0 edge selection
AMP1EN	FLG	0.A1H.3	R/W	AMP1 permit
AMP1MD2	FLG	0.A1H.2	R/W	Mode selection
AMP2MD1	FLG	0.A2H.1	R/W	Be sure to write "0"
AMP2MD0	FLG	0.A2H.0	R/W	SAMPLE-HOLD selection
CMPEN	FLG	0.A3H.3	R/W	Comparator permit
DACEN	FLG	0.A3H.2	R/W	D/A converter permit
ADCCH1	FLG	0.A3H.1	R/W	Comparator input selection
ADCCH0	FLG	0.A3H.0	R/W	Comparator input selection
P0DGIO	FLG	0.A7H.3	R/W	Port 0D I/O selection
P0BGIO	FLG	0.A7H.2	R/W	Port 0C I/O selection
P0BGIO	FLG	0.A7H.1	R/W	Port 0B I/O selection
P0AGIO	FLG	0.A7H.0	R/W	Port 0A I/O selection

Table 7-2 List of reserved symbols (4/4)

NAME	ATTRIBUTE	VALUE	R/W	DESCRIPTION
IPTM2	FLG	0.AEH.1	R/W	INTTM2 permit flag
IP1	FLG	0.AEH.0	R/W	INT1 permit flag
IPSIO	FLG	0.AFH.3	R/W	INTSIO permit flag
IPO	FLG	0.AFH.2	R/W	INT0 permit flag
IPTM1	FLG	0.AFH.1	R/W	INTTM1 permit flag
LCDOFF	FLG	0.B1H.3	R/W	LCD segment/port selection
LCDMD2	FLG	0.B1H.2	R/W	LCD mode selection
LCDMD1	FLG	0.B1H.1	R/W	LCD mode selection
LCDMD0	FLG	0.B1H.0	R/W	LCD mode selection
LCDEN	FLG	0.B2H.3	R/W	ICD segment output permit
PTOUTON	FLG	0.B7H.0	R/W	PTOUT output permit
SIOON	FLG	0.B7H.1	R/W	SIO output permit
IRQTM2	FLG	0.BEH.1	R/W	INTTM2 interrupt request
IRQ1	FLG	0.BEH.0	R/W	INT1 interrupt request
IRQSIO	FLG	0.BFG.3	R/W	INTSIO interrupt request
IRQ0	FLG	0.BFH.2	R/W	INT0 interrupt request
IRQTM1	FLG	0.BFG.1	R/W	INTTM1 interrupt request
DBF	DAT	0FH	R/W	GET/PUT instruction operand
IX	DAT	01H	R/W	Index register
AR	DAT	00H	R/W	Address register
SIOSFR	DAT	01H	R/W	SIO register
TM1M	DAT	02H	W	Timer 1 modulo register
TM2M	DAT	03H	W	Timer 2 modulo register
TMC	DAT	41H	R	Timer count register

Note: "W. XYH. Z" in the value field indicates

W Bank
X Row address
Y Column address
Z Bit

8. INSTRUCTION SET

Table 8-1 List of instruction sets

b14 to b11		b15		0	1
BIN	HEX				
0000	0	ADD	r, m	ADD	m, #i
0001	1	SUB	r, m	SUB	m, #i
0010	2	ADDC	r, m	ADDC	m, #i
0011	3	SUBC	r, m	SUBC	m, #i
0100	4	AND	r, m	AND	m, #i
0101	5	XOR	r, m	XOR	m, #i
0110	6	OR	r, m	OR	m, #i
0111	7	INC	AR		
		INC	IX		
		MOVT	DBF, @AR		
		BR	@AR		
		CALL	@AR		
		RET			
		RETSK			
		EI			
		DI			
		RETI			
		PUSH	AR		
		POP	AR		
		GET	DBF		
		PUT	p, DBF		
		PEEK	WR, RA		
		POKE	RA, WR		
		RORC	r		
		STOP	s		
		HALT	h		
		NOP			
1000	8	LD	r, m	ST	m, r
1001	9	SKE	m, #i	SKGE	m, #i
1010	A	MOV	@r, m	MOV	m, @r
1011	B	SKNE	m, #i	SKLT	m, #i
1100	C	BR	addr	CALL	addr
1101	D			MOV	m, #i
1110	E			SKT	m, #n
1111	F			SKF	m, #n

Table 8-2 List of INSTRUCTIONS

Legends

M	: One of data memory specified by [(BANK), m]	PC	: Program counter
m	: Data memory address specified by [mH, mL] of each bank	SP	: Stack pointer
m _H	: Data memory address high (row address) : 3 bits	STACK	: Stack specified by (SP)
m _L	: Data memory address low (column address) : 4 bits	BANK	: Bank register
R	: One of general register specified by [(RP), r]	(AR) rom	: One of program memory data specified by (AR)
r	: General register address low (column address) : 4 bits	INTEF	: Interrupt enable flag
RP	: General register pointer	i	: Immediate data : 4 bits
RF	: One of register file specified by rf	n	: Bit position : 4 bits
rf	: Register file address specified by [rfH, rfL]	addr	: One of program memory address : 11 bits
rf _H	: Register file address high (row address) : 3 bits	a _H	: Program memory address high : 3 bits
rf _L	: Register file address low (column address) : 4 bits	a _M	: Program memory address middle : 4 bits
AR	: Address register	a _L	: Program memory address low : 4 bits
IX	: Index register	CY	: Carry flag
IXE	: Index register enable flag	CMP	: Compare flag
DBF	: Data buffer	s	: Stop release condition
WR	: Window register	h	: Halt release condition
MP	: Memory pointer	[]	: Address of M, R, RF
MPE	: Memory pointer enable flag	i	: Contents of M, R, RF, AR, IX, DBF, WR, PE
PE	: Peripheral		
p	: Peripheral address		
p _H	: Peripheral address high (row address) : 3 bits		
p _L	: Peripheral address low (column address) : 4 bits		

Instruction group	Mnemonic	Operand	Function	Operation	Machine code			
					Operation code	3bits	4bits	4bits
Addition	ADD	r, m	Add memory to register	$R: CY \leftarrow (R) + (M)$	0000	m_H	m_L	r
		m, #i	Add immediate data to memory	$M: CY \leftarrow (M) + i$	1000	m_H	m_L	i
	ADDC	r, m	Add memory to register with carry	$R: CY \leftarrow (R) + (M) + (CY)$	0001	m_H	m_L	r
		m, #i	Add immediate data to memory with carry	$R: CY \leftarrow (M) + i + (CY)$	1001	m_H	m_L	i
	INC	AR	Increment address register	$AR \leftarrow AR + 1$	0011	000	1001	0000
		IX	Increment index register	$IX \leftarrow IX + 1$	0011	000	1000	0000
Subtraction	SUB	r, m	Subtract memory from register	$R: CY \leftarrow (R) - (M)$	0001	m_H	m_L	r
		m, #i	Subtract immediate data from memory	$M: CY \leftarrow (M) - i$	1001	m_H	m_L	i
	SUBC	r, m	Subtract memory from register with borrow	$R: CY \leftarrow (R) - (M) - (CY)$	0011	m_H	m_L	r
		m, #i	Subtract immediate data from memory with borrow	$M: CY \leftarrow (M) - i - (CY)$	1011	m_H	m_L	i
Comparison	SKE	m, #i	Skip if memory equal to immediate data	$M - i$, skip if zero	0100	m_H	m_L	i
	SKGE	m, #i	Skip if memory greater than or equal to immediate data	$M - i$, skip if not borrow	1100	m_H	m_L	i
	SKLT	m, #i	Skip if memory less than immediate data	$M - i$, skip if borrow	1101	m_H	m_L	i
	SKNE	m, #i	Skip if memory not equal to immediate data	$M - i$, skip if not zero	0101	m_H	m_L	i
	Logical operation	AND	m, #i	Logical AND of memory and immediate data	$M \leftarrow (M) \text{ AND } i$	1010	m_H	m_L
r, m			Logical AND of register and memory	$R \leftarrow (R) \text{ AND } (M)$	0010	m_H	m_L	r
OR		m, #i	Logical OR of memory and immediate data	$M \leftarrow (M) \text{ OR } i$	1011	m_H	m_L	i
		r, m	Logical OR of register and memory	$R \leftarrow (R) \text{ OR } (M)$	0011	m_H	m_L	r
XOR		m, #i	Logical XOR of memory and immediate data	$M \leftarrow (M) \text{ XOR } i$	1001	m_H	m_L	i
		r, m	Logical XOR of register and memory	$R \leftarrow (R) \text{ XOR } (M)$	0010	m_H	m_L	r
Transfer	LD	r, m	Load memory to register	$R \leftarrow (M)$	0100	m_H	m_L	r
	ST	m, r	Store register to memory	$(M) \leftarrow R$	1100	m_H	m_L	r
	MOV	@r, m	Move memory to destination memory referring to register	if MPE = 1, $[(MP), (R)] \leftarrow (M)$ if MPE = 0, $(m_H), (R)] \leftarrow (M)$	0101	m_H	m_L	r
		m, @r	Move source memory referring to register to memory	if MPE = 1, $M \leftarrow [(MP), (R)]$ if MPE = 0, $M \leftarrow [(m_H), (R)]$	1101	m_H	m_L	r
		m, #i	Move immediate data to memory	$M \leftarrow i$	1110	m_H	m_L	i
	MOVT	DBF, @AR	Move ROM data from the address specified in AR to DBF	$sp \leftarrow (sp) - 1, \text{STACK} \leftarrow PC$ $DBF \leftarrow (AR) \text{ rom},$ $PC \leftarrow \text{STACK}, sp \leftarrow (sp) + 1$	0011	000	0001	0000
	PUSH	AR	Decrement SP, then move AR to stack top	$SP \leftarrow (SP) - 1, \text{STACK} \leftarrow AR$	0011	000	1101	0000
	POP	AR	Move stack top to AR, then increment SP	$AR \leftarrow \text{STACK}, SP \leftarrow SP + 1$	0011	000	1100	0000
PEEK	WR, RA	Get RA from RF through WR	$WR \leftarrow (RF)$	0011	rf_H	0011	rf_L	

Instruction category	Mnemonic	Operand	Function	Operation	Machine code			
					Operation code	3bits	4bits	4bits
Transfer	POKE	RA,WR	Put data on WR into RA of RF	(RF) ← WR	00111	rf _H	0010	rf _L
	GET	DBF,p	Get peripheral data to DBF	DBF ← p	00111	p _H	1011	p _L
	PUT	p,DBF	Put data in DBF to peripheral	p ← DBF	00111	p _H	1010	p _L
Decision	SKT	m, #n	Test memory bits, then skip if all bits specified are true	CMP ← 0 skip if M(N) = all "1"	11110	m _H	m _L	n
	SKF	m, #n	Test memory bits, then skip if all bits specified are false	CMP ← 0 skip if M(N) = all "0"	11111	m _H	m _L	n
Branch	BR	addr	Jump to the address	PC ← ADDR	01100	a _H	a _M	a _L
		@AR	Jump to the address specified in AR	PC ← AR	00111	000	0100	0000
Shift	RORC	r	Rotate register right with carry	(CY) → (R) → CY	00111	000	0111	r
Subroutine	CALL	addr	Call subroutine	SP ← (SP) - 1 STACK ← ((PC) + 1), PC ← ADDR	11100	a _H	a _M	a _L
		@AR	Call subroutine specified in AR	SP ← (SP) - 1, STACK ← ((PC) + 1), PC ← (AR)	00111	000	0101	0000
	RET		Return to main routine from subroutine	PC ← (STACK), SP ← (SP) + 1	00111	000	1110	0000
	RETSK		Return to main routine from subroutine, then skip unconditionary	PC ← (STACK), SP ← (SP) + 1 and skip	00111	001	1110	0000
	RETI		return to main routine from interrupt service routine	PC ← (STACK), SP ← (SP) + 1 BANK ← (interrupt stack)	00111	100	1110	0000
Interrupt	EI		Enable interrupt	INTE flag ← 1	00111	000	1111	0000
	DI		Disable interrupt	INTE flag ← 0	00111	001	1111	0000
Others	STOP	s	Stop clock	STOP	00111	010	1111	s
	HALT	h	Halt the CPU, restart by condition H	HALT	00111	011	1111	h
	NOP		No operation	No operation	00111	100	1111	0000

9. ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings ($T_a = 25^\circ\text{C}$)

Supply Voltage	V_{DD}	-0.3 to +7.0	V		
Input Voltage	V_I	-0.3 to $V_{DD} + 0.3$	V	P0A	(1)
		-0.3 to +11	V		(2)
Output Voltage	V_O	-0.3 to $V_{DD} + 0.3$	V	All pins other than P0A	
		-0.3 to $V_{DD} + 0.3$	V	P0A	(1)
		-0.3 to +11	V		(2)
		-0.3 to $V_{LCD} + 0.3$	V	Segment/common pins	
		-0.3 to $V_{DD} + 0.3$	V	Pins other than above	
High-Level Output Current	I_{OH}	-5	mA	1 pin	
		-20	mA	Total of all pins	
Low-Level Output Current	I_{OL}	15	mA	1 pin	P0A, P0D
		30	mA		P0B, P0C
		100	mA	Total of all pins	
Operating Temperature	T_{opt}	-40 to +85	$^\circ\text{C}$		
Storage Temperature	T_{stg}	-65 to +150	$^\circ\text{C}$		
Power Consumption	P_d	190	mW	$T_a = 85^\circ\text{C}$	

Remarks: 1. N-ch open/drain output plus built-in pull-up resistor output
2. N-ch open/drain input/output

CAPACITY ($T_a = 25^\circ\text{C}$, $V_{DD} = 0\text{ V}$)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Input Capacity	C_{IN}			15	pF	$f = 1\text{ MHz}$ Pins other than those measured: 0 V
Output Capacity	C_{OUT}			15	pF	
Input/Output Capacity	C_{IO}			15	pF	

DC CHARACTERISTICS (T_a = -40 to +85 °C, V_{DD} = 3.0 to 6.0 V)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION	
High-Level Input Voltage	V _{IH1}	0.8 V _{DD}		9	V	At SI or $\overline{\text{SCK}}$ input	
	V _{IH2}	0.7 V _{DD}		9	V	At POA input	
	V _{IH3}	0.8 V _{DD}		V _{DD}	V	INT ₁ , INT ₁ , RESET	
	V _{IH4}	0.7 V _{DD}		V _{DD}	V	Pins other than above	
Low-Level Input Voltage	V _{IL1}	0		0.2 V _{DD}	V	SI, $\overline{\text{SCK}}$, INT ₀ , INT ₁ , RESET	
	V _{IL2}	0		0.3 V _{DD}	V	Pins other than above	
High-Level Output Voltage	V _{OH}	V _{DD} −2.0	V _{DD} −0.4		V		V _{DD} = 4.5 to 6.0 V I _{OH} = −1 mA
		V _{DD} −1.0	V _{DD} −0.04		V		I _{OH} = −100 μA
Low-Level Output Voltage	V _{OL}		0.85	2.0	V	POB, POC	V _{DD} = 4.5 to 6.0 V I _{OL} = 15 mA
			0.06	0.5	V		I _{OL} = 600 μA
			0.85	2.0	V	POA, POD	V _{DD} = 4.5 to 6.0 V I _{OL} = 10 mA
			0.15	0.4	V		V _{DD} = 4.5 to 6.0 V I _{OL} = 1.6 mA
			0.04	0.5	V		I _{OL} = 400 μA
High-Level Input Leak Current	I _{LIH1}			3	μA	Other than X1 and XO	V _{IN} = V _{DD}
	I _{LIH2}			10	μA	X1, XO	V _{IN} = V _{DD}
	I _{LIH3}			10	μA	POA (3)	V _{IN} = 9 V
Low-Level Input Leak Current	I _{LIL}			−3	μA	Other than X1 and XO	V _{IN} = 0 V
				−10	μA	X1, XO	V _{IN} = 0 V
High-Level Output Leak Current	I _{LOH1}			3	μA		V _{OUT} = V _{DD}
	I _{LOH2}			10	μA	POA (3)	V _{OUT} = 9 V
Low-Level Output Leak Current	I _{LOL}			−3	μA		V _{OUT} = 0 V
Input pin with built-in resistor (pull up/pull down)		35	65	110	kΩ	INT0, INT1, P1A, P1B	
Input pin with built-in resistor (pull up)		35	65	110	kΩ	RESET	
Input pin with built-in resistor (pull down)		7	15	26.5	kΩ	POA	
Supply Current (4)	I _{DD1}		1500	4500	μA	Operation mode	V _{DD} = 5 V ± 10 % f _{CC} = 8 MHz
			250	750	μA		V _{DD} = 3 V ± 10 % f _{CC} = 2 MHz
	I _{DD2}		550	1600	μA	Halt mode	V _{DD} = 5 V ± 10 % f _{CC} = 8 MHz
			110	330	μA		V _{DD} = 3 V ± 10 % f _{CC} = 2 MHz
	I _{DD3}		0.1	10	μA	Stop mode	V _{DD} = 5 V ± 10 %
			0.1	5	μA		V _{DD} = 3 V ± 10 %

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
V _{LCD} Voltage Range	V _{LCD}	3.0		V _{DD}	V	
Common Output Impedance (5)	R _{COM}		40		k Ω	V _{DD} = 4.5 to 6.0 V
Segment Output Impedance (5)	R _{SEG1}		40		k Ω	At LCD drive V _{DD} = 4.5 to 6.0 V
	R _{SEG2}		5		k Ω	At port operation Total output of all segment pins Current 2 mA or less V _{DD} = V _{LCD} = 4.5 to 6.0 V
Resistance Between V _{LCD} and GND	R _{VLC}		100		k Ω	When normal
			3.0		k Ω	When switching

Remarks: 3. When N-ch open/drain input/output is selected

4. The current that flows through the built-in pull-up or pull-down resistor is excluded

5. 3.5 k Ω (typ.) when switching between the common and segment output.

AMPLIFIER CHARACTERISTICS ($T_a = -40 = +85^\circ\text{C}$, $V_{DD} = 4.5$ to 6.0 V)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Input Offset Voltage	V _{OS}		± 6	± 18	mV	Normal amplifier mode
In-phase Input Voltage	V _{ICM}	0.0		3.6	V	V _{DD} = 5.0 V
Output Voltage Range	V _{OUT}	0.12		4.8	V	V _{DD} = 5.0 V, I _{OUT} = 0 μ A
Unity Gain Frequency	f _O		1.5		MHz	
Large Amplitude Gain	A _V		85		dB	V _{DD} = 5.0 V
Output Current	I _{OUT}	-50		100	μ A	V _{DD} = 5.0 V
CMRR			75		dB	
SVRR			-60		dB	
Through Rate		1.0			V/ μ s	
Hold Time	t _{SAMP}		0.05		ms	Sample/hold amplifier mode
Input/Output Voltage Error	V _{DIF}		± 6	± 18	mV	Sample/hold amplifier mode
Input Voltage Range	V _{IN}		0.12	2.5	V	Sample/hold amplifier mode
Supply Current	I _{AMP}		230	500	μ A	

COMPARATOR CHARACTERISTICS ($T_a = -40$ to $+85^\circ\text{C}$, $V_{DD} = 4.5$ to 6.0 V)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Input Voltage Range	V _{IN}	V _{SS}		V _{DD}	V	
Response Speed (6)	t _{COMP}	2			IC	
Power Consumption	V _{COMP}		100		μ A	V _{DD} = 5.0 V
Absolute Accuracy	V _{IT}		± 8.0	± 15.0	mV	
Input Resolution	V _{RE}		3.0		mV	

D/A CONVERTER CHARACTERISTICS ($T_a = -40$ to $+85$ °C, $V_{DD} = 4.5$ to 6.0 V, $V_{REFH} = V_{DD}$, $V_{REFL} = 0$ V)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Resolution		6	6	6	Bit	
Linearity				±0.5	LSB	
D/A Conversion Time (6)	t_{CONV}	2			IC	At no output load
DAC Current	I_{DAC}		220	390	μA	
A/D Conversion Time (6)		4			IC	

Remarks 6: IC indicates "instruction cycle".

ZERO-CROSS CHARACTERISTICS ($T_a = -40$ to $+85$ °C, $V_{DD} = 4.5$ to 6.0 V)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Detection Input Level	V_{ZX}	0.8	3.0		V _{p.p}	Input AC
Accuracy	A_{ZX}		±120		mV	50/60 Hz
Detection Input Frequency	f_{ZX}	0.04	1		kHz	

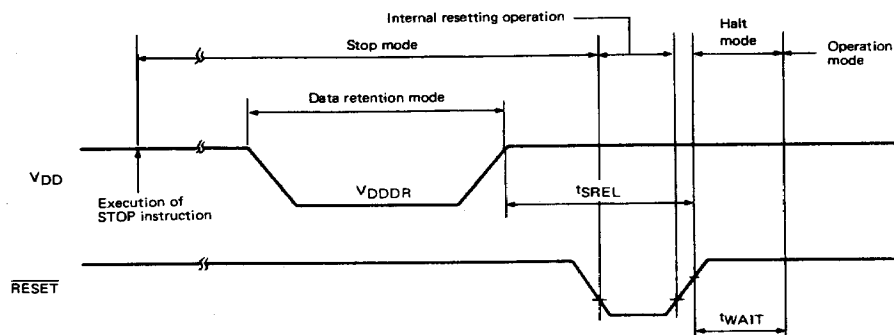
DATA MEMORY DATA RETENTION CHARACTERISTICS AT LOW SUPPLY VOLTAGE IN STOP MODE ($T_a = -40$ to $+85$ °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Data Retention Supply Voltage	V_{DDDR}	2.0		6.0	V	
Data Retention Supply Current	I_{DDDR}		0.1	5.0	μA	$V_{DDDR} = 2.0$ V
Release Signal Set Time	t_{SREL}	0			μs	
Wait Time for Stable Oscillation	t_{WAIT}		$2^{19}/f_x$		ms	Release by RESET (7)
			(8)		ms	Release by interrupt request

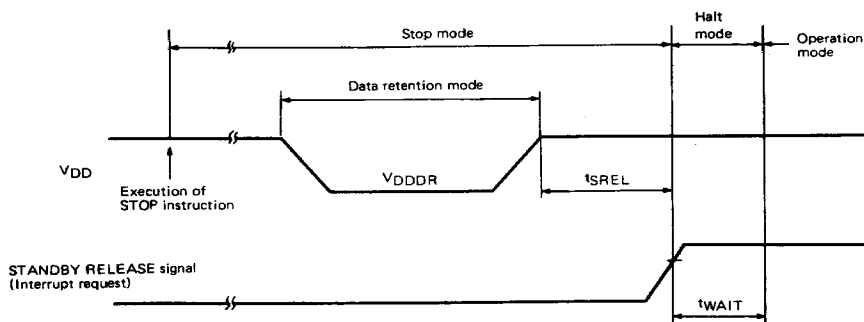
Remarks: 7. f_x indicates the oscillator frequency.

8. According to the timer 2 value.

Data Retention Timing (Stop Mode Release by Reset)



Data Retention Timing (Stand-by Release Signal: Stop Mode Release)

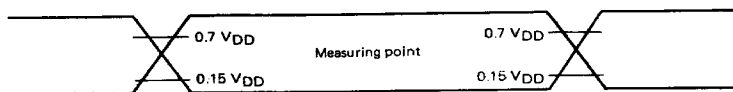


AC CHARACTERISTICS (T_a = -40 to +85 °C, V_{DD} = 3.0 to 6.0 V)

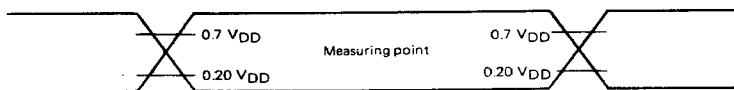
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION	
Internal Clock Cycle Time	t _{CY}	2		30	μs	V _{DD} = 4.5 to 6.0 V	
		8		30	μs		
Event Input Frequency	f _{PO}	0		1000	kHz	duty = 50 %	V _{DD} = 4.5 to 6.0 V
		0		350	kHz		
Event Input Rising/Falling Time	t _{POR} t _{POF}			0.1	μs	Excluding zero-cross mode	
Event Input High/Low Level Width	t _{POH}	0.5			μs	V _{DD} = 4.5 to 6.0 V	
	t _{POL}	1.45			μs		
$\overline{\text{SCK}}$ Input Cycle Time (9)	t _{KCY}	2.0			μs	At data input	V _{DD} = 4.5 to 6.0 V
		10.0			μs	At data output	
		5.0			μs	At data input	
		13.0			μs	At data output	
$\overline{\text{SCK}}$ Input High/Low Level Width (9)	t _{KH} t _{KL}	1.0			μs	At data input	V _{DD} = 4.5 to 6.0 V
		5.0			μs	At data Output	
		2.5			μs	At data input	
		6.5			μs	At data Output	
SI Setup Time (to $\overline{\text{SCK}}\uparrow$)	t _{SIK}	100			μs		
SI Hold Time (to $\overline{\text{SCK}}\uparrow$)	t _{KSI}	100			μs		
$\overline{\text{SCK}}\downarrow \rightarrow$ SO output delay time (9)	t _{KSO}			4.5	μs	C _p = 100 pF	
INT high/low level width	t _{IOH} t _{IOL}	10			μs		
$\overline{\text{RESET}}$ low level width	t _{RSL}	10			μs		

Remarks 9: For SI, SO and $\overline{\text{SCK}}$ pins, the N-ch open/drain output plus built-in pull-up resistor input/output.

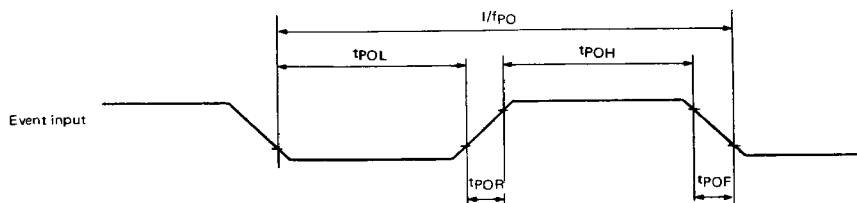
AC Timing Measuring Point (INT₀, INT₁, SI, $\overline{\text{SCK}}$ and SO Pins)



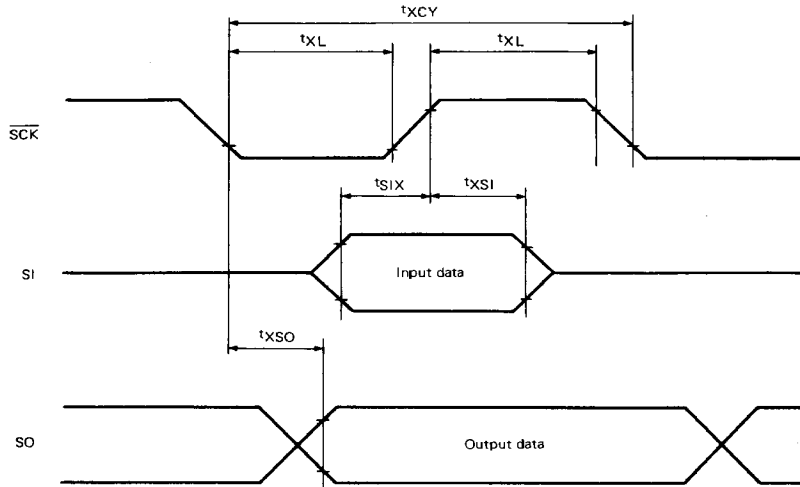
AC Timing Measuring Point (Pins other than INT₀, INT₁, SI, $\overline{\text{SCK}}$ SO)



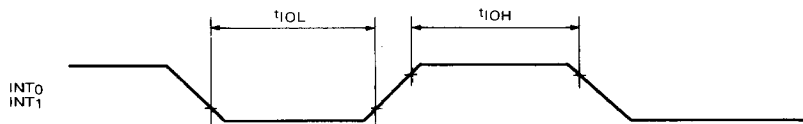
Event Input Timing



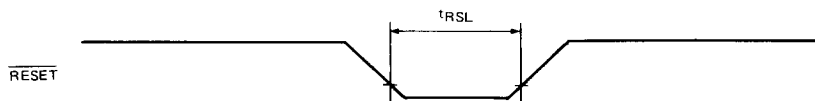
Serial Transfer Timing



INT Input Timing



RESET Input Timing



10. RECOMMENDED SOLDERING CONDITIONS

The following conditions (see table below) must be met when soldering this product.

Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

TYPES OF SURFACE MOUNT DEVICE

For more details, refer to our document "SMT MANUAL" (IEI-1207).

μPD17102G

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak package's surface temperature : 230 °C or below, Reflow time : 30 seconds or below (210 °C or higher), Number of reflow process : 1, Exposure limit* : None	IR30-00
VPS	Peak package's surface temperature : 215 °C or below, Reflow time : 40 seconds or below (200 °C or higher), Number of reflow process : 1, Exposure limit* : None	VP15-00
Wave soldering	Solder temperature : 260 °C or below, Flow time : 10 seconds or below, Number of flow process : 1, Exposure limit* : None	WS60-00
Partial heating method	Terminal temperature : 300 °C or below, Flow time : 10 seconds or below, Exposure limit* : None	

*: Exposure limit before soldering after dry-pack package is opened.

Storage conditions: 25 °C and relative humidity at 65 % or less.

Note: Do not apply more than a single process at once, except for "Partial heating method".

11. DEVELOPMENT SUPPORT TOOLS

The following tools are supported for developing systems using the μPD17102 chip.

Hard-ware	IE-17K	IE-17K is an in-circuit emulator available for all the μPD17000 Series chips. For the μPD17102 chip, use IE-17K and the optional SE-17102 together. When connected to a personal computer, IE-17K adds and modifies programs in real time. A PC-9801 personal computer runs the support software SIMPLEHOST, providing a more advanced development environment.		
	SE-17102	SE-17102 is an emulation board (SE board) used to evaluate the system by mounting the program developed by IE-17K and loading the board instead of the μPD17102 to the system.		
	EP-17102G	Probe used to connect the target system.		
Soft-ware	μPD17000 Series Assembler AS17K	Host machine	OS	Order name (product name)
		PC-9800 Series (excluding PC-98LT)	MS-DOS™ (Ver 2.11 or later)	μS5A1AS17K (8" 2D) μS5A10AS17K (5" 2HD)
	Device file	Used together with the μPD17000 Series Assembler AS17K (for μPD17102 only).		μS5A1AS17102 (8" 2D) μS5A10AS17102 (5" 2HD)
	SIMPLEHOST*	Program to support man-machine interface when connecting PC-9801 to IE-17K. MS-WINDOWS™ is required.		μS5A11E17K (8" 2D) μS5A10E17K (5" 2HD)

*: Under development

MS-DOS™ and MS-WINDOW™ are the trademark of Microsoft Co., Ltd.