SHARP

NEW PRODUCT INFORMATION
PRELIMINARY

LZ9C Series

Channel-free Gate Array (Sea-of-gates) With Built-in CPU Core

Description

The LZ9C series is a channel-free gate array with a built-in Z80 CPU core.

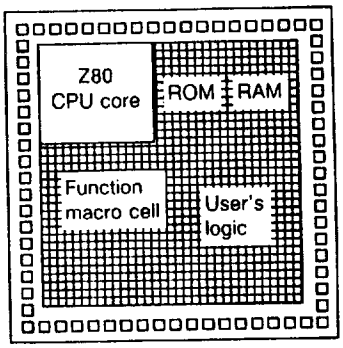
In general, there are two logic unit systems for a system integration chip. One is standard cell logic and the other is gate array logic.

Development of the standard cell logic chip requires longer TAT of approx. 6 months.

However, a gate array logic chip of the LZ9C series, requires very short TAT of approx. 2 months for designing user's own system chip.

Furthermore, the LZ9C series is compatible with the LZ98 series and its library, which allow the LZ9C series to be developed with same development procedure and environment as those of the LZ98 series of gate arrays.

Block Diagram



Features

1. CMOS process
2. Sea-of-gate structure
3. On-chip CMOS Z80 CPU core
4. Total gate count and I/O buffers

LZ9C series	Total gate count *	I/O buffers
LZ9C3500	3500	96
LZ9C10000	10000	116
LZ9C16000	16000	134
LZ9C26000	26000	162
LZ9C32000	32000	178

* Usable gate count should be 60 percent of total gates.

5. Delay time: 0.6ns/gate (F.O. = 3, ℓ = 1mm)
6. Output current: 12mA
7. Supply voltage: 5V ± 10%
8. Short turn around time delivery
9. Compatible with Sharp's LZ98 series of gate arrays and its library
10. CPU peripheral macro cells available

I C

LZ9C Series Lineup

Model No.		LZ9C3500	LZ9C10000	LZ9C16000	LZ9C26000	LZ9C32000
Total gate count		3500	10000	16000	26000	32000
Usable gate count		2100	6000	9600	15600	19200
I/O buffers		96	116	134	162	178
Process		1μm CMOS, double metal				
Delay time	Internal gate	0.6ns				
	Input buffer	2.2ns				
	Output buffer	2.7ns				
I/O level		TTL/CMOS				
Supply voltage		5V ± 5% (TTL interface) 5V ± 10% (CMOS interface)				

LZ9C Series

Channel-free Gate Array
(Sea-of-gates) With Built-in CPU Core

Electrical Characteristics

Parameter	Symbol	Conditions	TTL level			CMOS level			Unit
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input LOW voltage	V_{IL}				0.8			1.5	V
Input HIGH voltage	V_{IH}		2.0			3.5			V
Input HIGH threshold voltage	V_T^+	Schmitt input buffer			2.2			3.7	V
Input LOW threshold voltage	V_T^-	Schmitt input buffer	0.5			1.0			V
Hysteresis voltage	$V_T^+ - V_T^-$	Schmitt input buffer	0.2			0.4			V
Output LOW voltage	V_{OL}	I_{OL} = 1, 2, 4, 6, 8, 12mA			0.4			0.4	V
Output HIGH voltage	V_{OH}	I_{OH} = −0.5, −1, −2, −3, −4, −6mA	4.0			4.0			V
Input leakage current	I_i	V_I = 0V, V_{CC}	−1.0		1.0	−1.0		1.0	μA
Output leakage current	I_{OZ}	Output high impedance	−1.0		1.0	−1.0		1.0	μA
Input LOW current	$\lvert I_{OL} \rvert$	V_I = 0V	8	20	60	8	20	60	μA
Input HIGH current	I_{OH}	V_I = V_{CC}	8	20	60	8	20	60	μA

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC}	−0.3 to 6.0	V
Input voltage	V_I	−0.3 to V_{CC} + 0.3	V
Output voltage	V_O	−0.3 to V_{CC} + 0.3	V
Operating temperature	Topr	−40 to +85	°C
Storage temperature	Tstg	−55 to +150	°C

Recommended Operating Conditions

Parameter	Symbol	TTL level			CMOS level			Unit
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply voltage	V_{CC}	4.75	5	5.25	4.5	5	5.5	V
Operating temperature	Topr	−40		+85	−40		+85	°C

Macro Cells

(1) Internal standard macro cells

Name	Function	Gate count
Inverters, non-Inverters		
INV1	Single drive inverter	1
INV2	Double drive inverter	1
INV3	Tripple drive inverter	2
INV4	Quad drive inverter	2
INV6	6 times drive inverter	3
INV1P	Single drive inverter Pch Tr. PARA.	1
INV2P	Double drive inverter Pch Tr. PARA.	2
INV4P	Quad drive inverter Pch Tr. PARA.	4
NIN1	Single drive non-inverter	1
NIN2	Double drive non-inverter	2
NIN3	Triple drive non-inverter	2
NIN4	Quad drive non-inverter	3
Internal bus buffers, delay elements		
CINV	Active high clocked inverter (Half drive internal bus buffer)	2
CXINV	Active low clocked inverter (Half drive internal bus buffer)	2
INTB1	Single drive internal bus buffer	3
INTB2	Double drive internal bus buffer	4
INTB4	Quad drive internal bus buffer	5
DLY10	10nsec delay (App.)	12
DLY20	20nsec delay (App.)	24
DLY40	40nsec delay (App.)	48
NAND/NOR gates		
NA2	2-input NAND gate	1
NA3	3-input NAND gate	2
NA4	4-input NAND gate	2
NA5	5-input NAND gate	4
NA6	6-input NAND gate	5
NA7	7-input NAND gate	5
NA8	8-input NAND gate	6
NA2P	2-input POWER NAND gate	2
NA3P	3-input POWER NAND gate	3
NA4P	4-input POWER NAND gate	4
NO2	2-input NOR gate	1
NO3	3-input NOR gate	2
NO4	4-input NOR gate	2
NO5	5-input NOR gate	4
NO6	6-input NOR gate	5
NO7	7-input NOR gate	5
NO8	8-input NOR gate	6
NO2P	2-input POWER NOR gate	2
NO3P	3-input POWER NOR gate	3
NO4P	4-input POWER NOR gate	4
AND/OR/EX-NOR gates		
AN2	2-input AND gate	2
AN3	3-input AND gate	2
AN4	4-input AND gate	3
OR2	2-input OR gate	2
OR3	3-input OR gate	2
OR4	4-input OR gate	3

LZ9C Series

Channel-free Gate Array
(Sea-of-gates) With Built-in CPU Core

Name	Function	Gate count
AND/OR/EX-NOR gates		
EXO	2-input EXCLUSIVE OR	3
EXN	2-input EXCLUSIVE NOR	3
Combined logic circuits, combined gate circuits		
ON1	2,1 input OR-NAND gate	2
DN1	2,1 input AND-NOR gate	2
DN22	2×2 input AND-NOR gate	2
OA1	2,1 input OR-AND gate	2
OA22	2×2 input OR-AND gate	3
AO1	2,1 input AND-OR gate	2
AO22	2×2 input AND-OR gate	3
AO23	2×3 input AND-OR gate	4
AO24	2×4 input AND-OR gate	5
AO25	2×5 input AND-OR gate	6
AO26	2×6 input AND-OR gate	7
AO32	3×2 input AND-OR gate	4
AO33	3×3 input AND-OR gate	5
AO34	3×4 input AND-OR gate	7
AO42	4×2 input AND-OR gate	5
AO43	4×3 input AND-OR gate	7
AO52	5×2 input AND-OR gate	7
AON	2,1,1 input AND-OR-NAND gate	2
OAN	2,1,1 input OR-AND-NOR gate	2
DS	2 to 1 data selector	3
DSN	2 to 1 inverting data selector	3
ADDH	Half adder	4
ADDF	Full adder	7
Latch, flip-flop cells		
DLT	D latch	4
DLTR	D latch with reset	5
D	D flip-flop	6
DR	D flip-flop with reset	8
DRS	D flip-flop with reset & set	10
DRS4	D flip-flop with reset & set	8
DAL3	D flip-flop with asynchronous load	10
TR	T flip-flop with reset	10
JK	JK flip-flop	9
JKRS	JK flip-flop with reset & set	12
Flip-flop cells for ATPG		
SD	D flip-flop for ATPG	8
SDR	D flip-flop with reset for ATPG	9
SDRS	D flip-flop with reset & set for ATPG	11
SDRS4	D flip-flop with reset & set for ATPG	10
SDAL3	D flip-flop with asynchronous load for ATPG	12
STR	T flip-flop with reset for ATPG	11
SJK	JK flip-flop for ATPG	11
SJKRS	JK flip-flop with reset & set for ATPG	13

Name	Function	Gate count
CPU macro cells		
DMAC	Direct Memory Access Controller	5482 + α
UART	Universal Asynchronous Receiver and Transmitter	3015 + α
USART	Universal Synchronous/Asynchronous Receiver and Transmitter	2500 + α
PIT	Programmable Internal Timer	3516 + α
PIO	Parallel I/O	2056 + α
PIC	Programmable Interrrupt Controller	2209 + α
CG	Clock Generator	111 + α
BUSC	Bus Controller	572 + α

α: gates for test circuits

I/O Buffer Cells

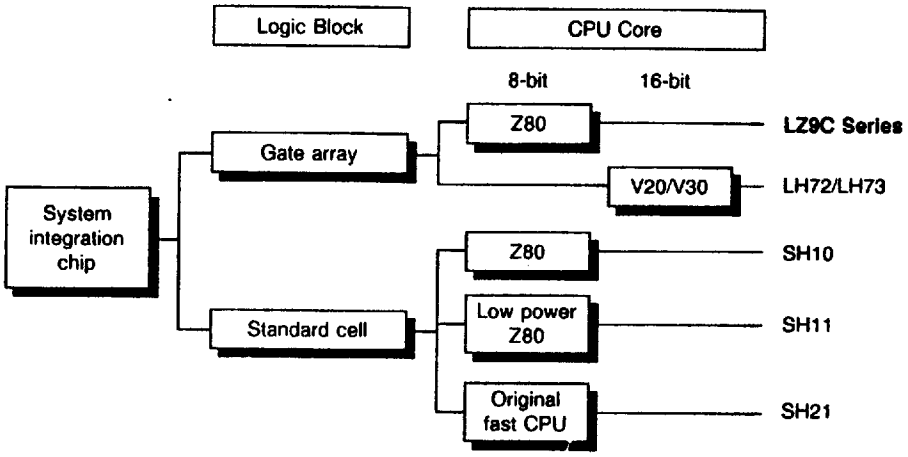
(1) Standard I/O cells (Cells with pull-up/pull-down resistors are also available.)

Name	Function	Gate count
Special input cells		
IBF	TTL level input buffer	1
IBFC	CMOS level input buffer	1
IBFS	TTL level schmitt-trigger input buffer	1
IBFCS	CMOS level schmitt-trigger input buffer	1
Special output cells		
OBF	Output buffer I_{OL} = 4mA (I_{OH} = – 2mA)	0
OBF1M	Output buffer I_{OL} = 1mA (I_{OH} = – 0.5mA)	0
OBF2M	Output buffer I_{OL} = 2mA (I_{OH} = – 1mA)	0
OBF6M	Output buffer I_{OL} = 6mA (I_{OH} = – 3mA)	0
OBF8M	Output buffer I_{OL} = 8mA (I_{OH} = – 4mA)	0
OBF12M	Output buffer I_{OL} = 12mA (I_{OH} = – 6mA)	0
TOBF (4mA)	Output buffer I_{OL} = 4mA (I_{OH} = – 2mA, 3-state output)	0
OBFN (4mA)	Output buffer I_{OL} = 4mA (Nch open drain output)	0
OBFP (2mA)	Output buffer I_{OH} = 2mA (Pch open drain output)	0
Common I/O cell		
IOBF (4mA)	TTL level input and I_{OL} = 4mA (I_{OH} = 2mA) output buffer	1
IOBFC (4mA)	CMOS level input and I_{OL} = 4mA (I_{OH} = 2mA) output buffer	1
Special I/O cells		
OSC	Oscillator with IBF0 (Drive factor 4)	1
OSC1M	Oscillator with IBF0 (Drive factor 1)	1
OSC2M	Oscillator with IBF0 (Drive factor 2)	1
OSCL	Low power oscillator (with IBF0)	1
ASW	Analog switch (with OBF0)	0
OBF0	Analog switch (with ASW)	0
IBF0	Oscillator with OSC, OSCIM, OSC2M, or OSCL	0
XIBFC5	5 times drive inverting input buffer	0
XOBF1M	3 PAD C-R oscillator with IBFCS and OSC	0
NABF	Amplifier NAND input buffer with OBFC0	0
IOBF0C	Amplifier with NABF	1
BINV5	5 times drive inverter ON I/O cell	0

LZ9C Series

Channel-free Gate Array (Sea-of-gates) With Built-in CPU Core

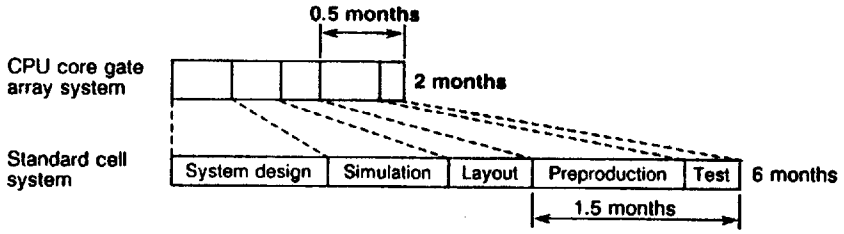
Sharp's Product Lineup



- Relative Reference Table

	System integration chip	
	Gate array system (LZ9C10000)	Standard cell
Turn around time	**2 months**	6 months
Preproduction time	**0.5 month**	1.5 months
Development cost ratio	1	3
Unit price ratio	1	0.8

- Turn Around Time Frame

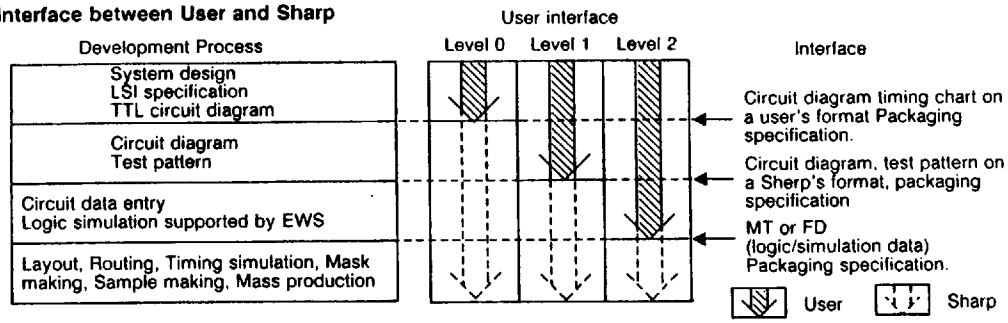


Packages

Model No.	DIP					SDIP		QFP											SOP	CPGA			QFJ
	24	28	32	40	48	42	64	44	48	60	64	80 □	80 ▢	96	100	128	160	208	28	120	144	180	44
LZ9C3500	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●				●				●
LZ9C10000	●	●		●	●		●	●		●	●	●	●	●	●	●							
LZ9C16000	●			●			●			●		●	●	●	●	●	●					●	
LZ9C26000			●	●			●						●	●		●	●	●		●	●	●	
LZ9C32000			●	●									●	●		●	●	●		●	●	●	

Support System

- **Interface between User and Sharp**



Support Tools

Support	System	Version
EWS	Mentor IDEA	Ver. 70

Support	System	Hardware
Personal computer	Sharp SF-CAD	PC8041 (MS-DOS 3.2)
	Workview (Ver. 3.0)	IBM PC-AT (MS-DOS 3.2)

CPU Peripherals macro Cell			Cell library compatible with LZ98
Peripherals		Gate scale	
82C37	DMAC	5482 + α	· Basic macro cell library
82C50	UART	3015 + α	
82C51	USART	2500 + α	· TTL 74 equivalent cells
82C54	PIT	3516 + α	
82C55	PIO	2056 + α	· ROM
82C59	PIC	2209 + α	
82C84	CG	111 + α	· RAM
82C88	BUSC	572 + α	

α: Additional gates for test circuits with approx. 10% of each gate count, which eliminate tests at user's side.