

# HM658128A Series

131072-word × 8-bit High Speed CMOS Pseudo Static RAM

The Hitachi HM658128A is a pseudo-static RAM organized as 131,072-word × 8-bit. HM658128A realizes low power consumption and high speed access time by employing 1.3 μm CMOS process technology.

The HM658128A supports 3 refresh functions: address refresh, auto refresh and self refresh. Low power version dissipates only 0.5 mW (typ) in self refresh mode and retains the data with battery. Self refresh mode is guaranteed only for L-version and LL-version.

The HM658128A is pin-compatible with 1-Mbit static RAM.

## Features

- Single 5 V (±10%)
- High speed
  - Access time  
CE Access time: 80/100/120 ns
  - Cycle time  
Random read/  
Write cycle time : 130/160/190 ns
- Low power: 300 mW typ (active)  
0.5 mW (standby)
- All inputs and outputs TTL compatible
- Non multiplexed address
- 512 refresh cycles (8 ms)
- Refresh functions
  - Address refresh
  - Automatic refresh
  - Self refresh (Only for L-version and LL-version)

## Ordering Information

Type No.	Access time	Package
HM658128ADP-8	80 ns	600-mil 32-pin plastic DIP (DP-32)
HM658128ADP-10	100 ns	
HM658128ADP-12	120 ns	
HM658128ALP-8	80 ns	
HM658128ALP-10	100 ns	
HM658128ALP-12	120 ns	
HM658128ALP-8L	80 ns	
HM658128ALP-10L	100 ns	
HM658128ALP-12L	120 ns	
HM658128ADFP-8	80 ns	32-pin plastic SOP (FP-32D)
HM658128ADFP-10	100 ns	
HM658128ADFP-12	120 ns	
HM658128ALFP-8	80 ns	
HM658128ALFP-10	100 ns	
HM658128ALFP-12	120 ns	
HM658128ALFP-8L	80 ns	
HM658128ALFP-10L	100 ns	
HM658128ALFP-12L	120 ns	
HM658128ALT-8	80 ns	8 mm × 20 mm 32-pin plastic TSOP (TFP-32D)
HM658128ALT-10	100 ns	
HM658128ALT-12	120 ns	
HM658128ALT-8L	80 ns	
HM658128ALT-10L	100 ns	
HM658128ALT-12L	120 ns	
HM658128ADT-8	80 ns	
HM658128ADT-10	100 ns	
HM658128ADT-12	120 ns	
HM658128ADR-8	80 ns	8 mm × 20 mm 32-pin plastic TSOP reverse type (TFP-32DR)
HM658128ADR-10	100 ns	
HM658128ADR-12	120 ns	
HM658128ALR-8	80 ns	
HM658128ALR-10	100 ns	
HM658128ALR-12	120 ns	
HM658128ALR-8L	80 ns	
HM658128ALR-10L	100 ns	
HM658128ALR-12L	120 ns	

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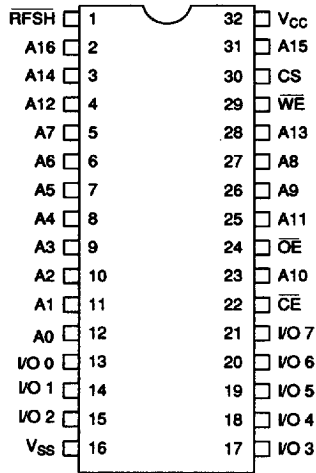
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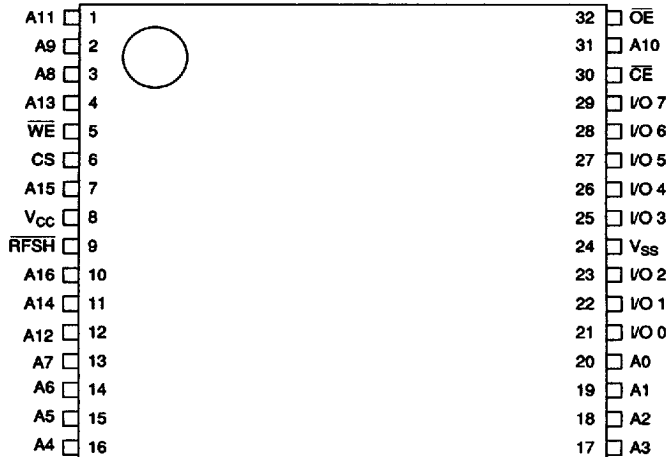
## Pin Arrangement

### HM658128AP/AFP Series



(Top View)

### HM658128AT Series



(Top View)

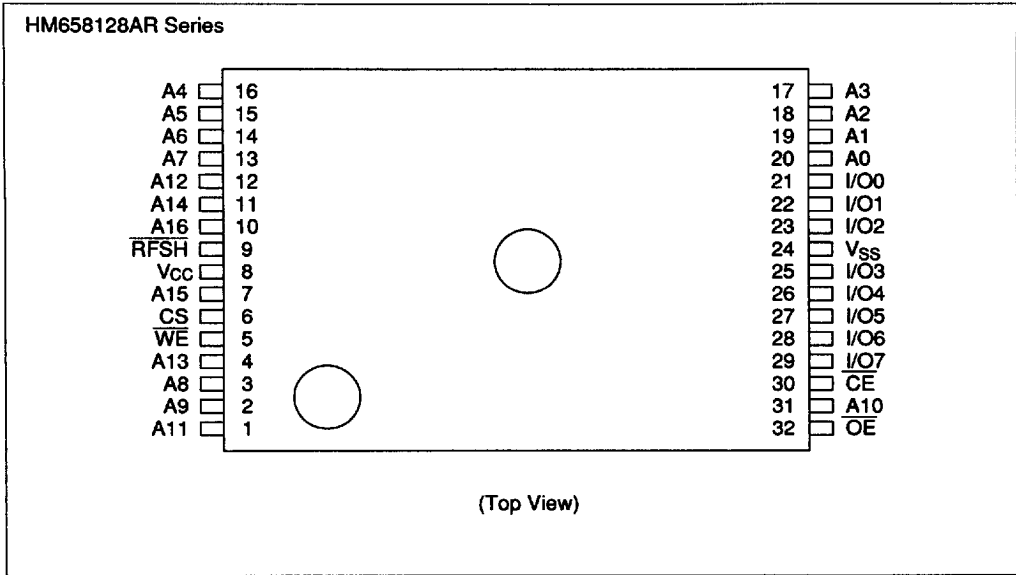
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Pin Arrangement (cont)



Pin Description

Symbol	Pin name
A0 – A16	Address inputs
I/O0 – I/O7	Data input/output
RFSH	Refresh
CE	Chip enable
OE	Output enable
WE	Write enable
CS	Chip select
V <sub>CC</sub>	Power supply
V <sub>SS</sub>	Ground

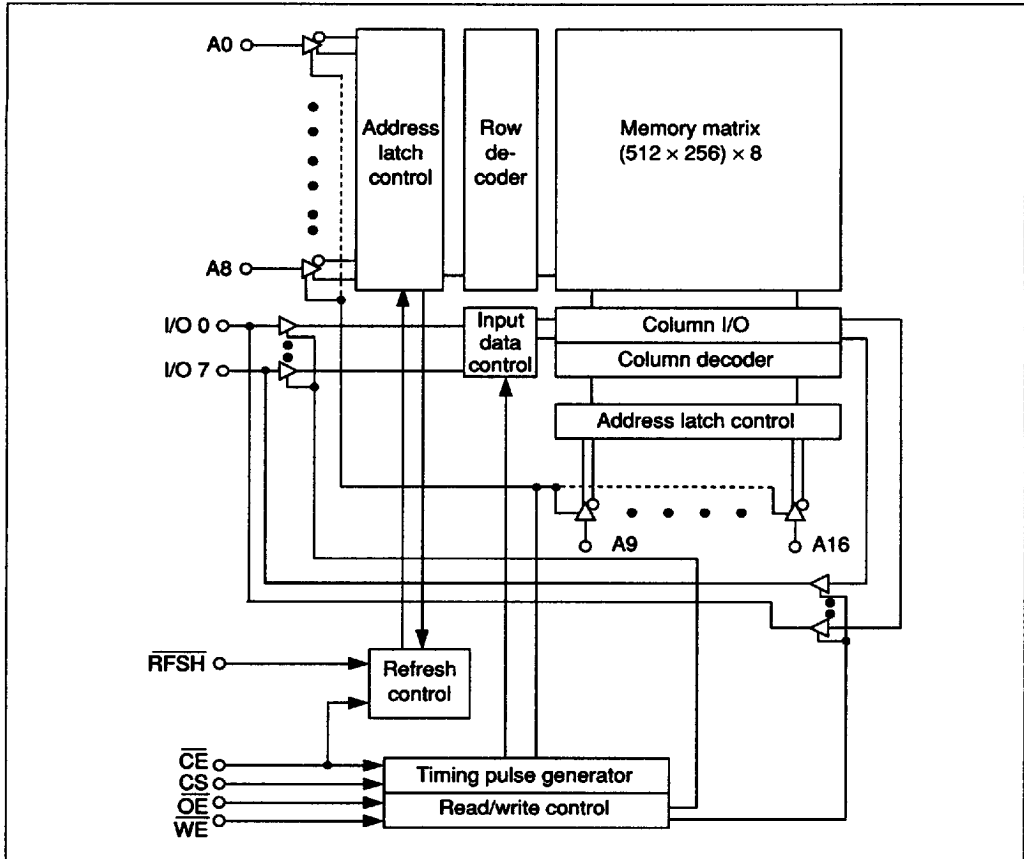
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## Block Diagram



## Truth Table

$\overline{CE}$	CS at $\overline{CE}$ going low	$\overline{RFSH}$	$\overline{OE}$	$\overline{WE}$	I/O pin	Mode
L	H	X	L	H	Low-Z	Read
L	H	X	X	L	High-Z	Write
L	H	X	H	H	High-Z	—
L	L	X	X	X	High-Z	CS Standby
H	X	L	X	X	High-Z	Refresh <sup>1</sup>
H	X	H	X	X	High-Z	Standby

Note: 1. Self refresh is guaranteed only for L-version and LL-version.

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**Absolute Maximum Ratings**

Parameter	Symbol	Rating	Unit
Terminal voltage with respect to $V_{SS}$	$V_T$	-1.0 to +7.0	V
Power dissipation	$P_T$	1.0	W
Operating temperature	$T_{opr}$	0 to +70	°C
Storage temperature	$T_{stg}$	-55 to +125	°C
Storage temperature under bias	$T_{bias}$	-10 to +85	°C

**Recommended DC Operating Conditions ( $T_a = 0$  to +70°C)**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{CC}$	4.5	5.0	5.5	V
	$V_{SS}$	0	0	0	V
Input voltage	$V_{IH}$	2.2	—	6.0	V
	$V_{IL}$	-0.5 <sup>1</sup>	—	0.8	V

Note: 1.  $V_{IL}$  min = -3.0 V for pulse width  $\leq$  10 ns.

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DC Characteristics (Ta = 0 to +70°C, V<sub>CC</sub> = 5 V ± 10%)

Parameter	Symbol	Min	Typ	Max	Unit	Test condition
Operating power supply current	I <sub>CC1</sub>	—	60	85	mA	I <sub>I/O</sub> = 0 mA t <sub>cy</sub> = min.
Standby power supply current	I <sub>SB1</sub>	—	1	2	mA	CE = V <sub>IH</sub> RFSH = V <sub>IH</sub> , Vin ≥ 0 V
Standby power supply current	I <sub>SB2</sub>	—	100 <sup>*1</sup>	200 <sup>*1</sup>	μA	CE ≥ V <sub>CC</sub> - 0.2 V RFSH ≥ V <sub>CC</sub> - 0.2 V, Vin ≥ 0 V
		—	70 <sup>*2</sup>	100 <sup>*2</sup>	μA	
Operating power supply current in self refresh mode	I <sub>CC2</sub>	—	1 <sup>*1, *2</sup>	2 <sup>*1, *2</sup>	mA	CE = V <sub>IH</sub> RFSH = V <sub>IL</sub> , Vin ≥ 0 V
		—	100 <sup>*1</sup>	200 <sup>*1</sup>	μA	
	—	70 <sup>*2</sup>	100 <sup>*2</sup>	μA		
Input leakage current	I <sub>LI</sub>	-10	—	10	μA	V <sub>CC</sub> = 5.5 V Vin = V <sub>SS</sub> to V <sub>CC</sub>
Output leakage current	I <sub>LO</sub>	-10	—	10	μA	OE = V <sub>IH</sub> V <sub>I/O</sub> = V <sub>SS</sub> to V <sub>CC</sub>
Output voltage	V <sub>OL</sub>	—	—	0.4	V	I <sub>OL</sub> = 2.1 mA
	V <sub>OH</sub>	2.4	—	—	V	I <sub>OH</sub> = -1 mA

- Notes: 1. This characteristics is guaranteed only for L-version.  
2. This characteristics is guaranteed only for LL-version.

Capacitance (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit	Test condition
Input capacitance	C <sub>in</sub>	—	8	pF	Vin = 0 V
Input/output capacitance	C <sub>I/O</sub>	—	10	pF	V <sub>I/O</sub> = 0 V

Note: This parameter is sampled and not 100% tested.

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## AC Characteristics (Ta = 0 to +70°C, VCC = 5 V ± 10%)

### Test Conditions

- Input pulse levels: 2.4 V, 0.4 V
- Input rise and fall times: 5 ns
- Timing measurement level: 2.2 V, 0.8 V
- Reference level: V<sub>OH</sub> = 2.0 V, V<sub>OL</sub> = 0.8 V
- Output load: 1 TTL and 100 pF (including scope and jig)

Parameter	Symbol	HM658128A-8		HM658128A-10		HM658128A-12		Unit
		Min	Max	Min	Max	Min	Max	
Random read or write cycle time	t <sub>RC</sub>	130	—	160	—	190	—	ns
Random read-modify-write cycle time	t <sub>RWC</sub>	190	—	220	—	260	—	ns
Chip enable access time	t <sub>CEA</sub>	—	80	—	100	—	120	ns
Output enable access time	t <sub>OEA</sub>	—	30	—	30	—	40	ns
Chip disable to output in high-Z	t <sub>CHZ</sub>	0	30	0	30	0	35	ns
Chip enable to output in low-Z	t <sub>CLZ</sub>	20	—	20	—	20	—	ns
Output disable to output in high-Z	t <sub>OHZ</sub>	—	25	—	25	—	30	ns
Output enable to output in low-Z	t <sub>OLZ</sub>	0	—	0	—	0	—	ns
Chip enable pulse width	t <sub>CE</sub>	80 ns	10 μs	100 ns	10 μs	120 ns	10 μs	
Chip enable precharge time	t <sub>p</sub>	40	—	50	—	60	—	ns
Address setup time	t <sub>AS</sub>	0	—	0	—	0	—	ns
Address hold time	t <sub>AH</sub>	30	—	30	—	35	—	ns
Read command setup time	t <sub>RCS</sub>	0	—	0	—	0	—	ns
Read command hold time	t <sub>RCH</sub>	0	—	0	—	0	—	ns
RFSH hold time	t <sub>RHC</sub>	15	—	15	—	15	—	ns
Chip select setup time	t <sub>CSS</sub>	0	—	0	—	0	—	ns
Chip select hold time	t <sub>CSH</sub>	30	—	30	—	35	—	ns
Write command pulse width	t <sub>WP</sub>	30	—	30	—	35	—	ns
Chip enable to end of write	t <sub>CW</sub>	80	—	100	—	120	—	ns
Data in to end of write	t <sub>DW</sub>	25	—	25	—	30	—	ns
Data in hold time for write	t <sub>DH</sub>	0	—	0	—	0	—	ns

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## HM658128A Series

AC Characteristics (Ta = 0 to +70°C, V<sub>CC</sub> = 5 V ± 10%) (cont)

Parameter	Symbol	HM658128A-8		HM658128A-10		HM658128A-12		Unit
		Min	Max	Min	Max	Min	Max	
Output active from end of write	t <sub>OW</sub>	5	—	5	—	5	—	ns
Write to output in high-Z	t <sub>WHZ</sub>	—	25	—	25	—	30	ns
Transition time (rise and fall)	t <sub>T</sub>	3	50	3	50	3	50	ns
Refresh command delay time	t <sub>RFD</sub>	40	—	50	—	60	—	ns
Refresh precharge time	t <sub>FP</sub>	40	—	40	—	40	—	ns
Refresh command pulse width	t <sub>RP</sub>	—	8	—	8	—	8	μs
Refresh command pulse width for automatic refresh	t <sub>FAP</sub>	80 ns	8 μs	80 ns	8 μs	80 ns	8 μs	
Automatic refresh cycle time	t <sub>FC</sub>	130	—	160	—	190	—	ns
Refresh command pulse width for self refresh	t <sub>FAS</sub> <sup>*9</sup>	8	—	8	—	8	—	μs
Refresh reset time for self refresh	t <sub>RFS</sub> <sup>*9</sup>	130	—	160	—	190	—	ns
Refresh period (512 cycles)	t <sub>REF</sub>	—	8	—	8	—	8	ms

- Notes:
1. t<sub>CHZ</sub>, t<sub>OHZ</sub> and t<sub>WHZ</sub> are defined as the time at which the output achieves the open circuit conditions.
  2. t<sub>CHZ</sub>, t<sub>CLZ</sub>, t<sub>OHZ</sub>, t<sub>OLZ</sub>, t<sub>WHZ</sub> and t<sub>OW</sub> are sampled under the condition of t<sub>T</sub> = 5 ns and not 100% tested.
  3. A write occurs during the overlap of a low  $\overline{CE}$  and a low  $\overline{WE}$ . Write ends at the earlier of  $\overline{WE}$  going high or  $\overline{CE}$  going high.
  4. If the  $\overline{CE}$  low transition occurs simultaneously with or latter from the  $\overline{WE}$  low transition, the output buffers remain in high impedance state.
  5. In write cycle,  $\overline{OE}$  or  $\overline{WE}$  must disable output buffers prior to applying data to the device and at the end of write cycle data inputs must be floated prior to  $\overline{OE}$  or  $\overline{WE}$  turning on output buffers.
  6. Transition time t<sub>T</sub> is measured between V<sub>IH</sub> min and V<sub>IL</sub> max.
  7. After power-up, pause more than 100 μs and execute at least 8 initialization cycles.
  8. 512 cycles of burst refresh or the first cycle of distributed automatic refresh must be executed within 15 μs after self refresh, in order to meet the refresh specification of 8 ms and 512 cycles.
  9. This characteristics is guaranteed only for L-version and LL-version.
  10. At the end of self refresh, refresh reset time (t<sub>RFS</sub>) is required to reset the internal self refresh operation of the RAM. During t<sub>RFS</sub>,  $\overline{CE}$  and  $\overline{RFSH}$  must be kept high. If auto refresh follows self refresh, low transition of  $\overline{RFSH}$  at the beginning of auto refresh must not occur during t<sub>RFS</sub> period.

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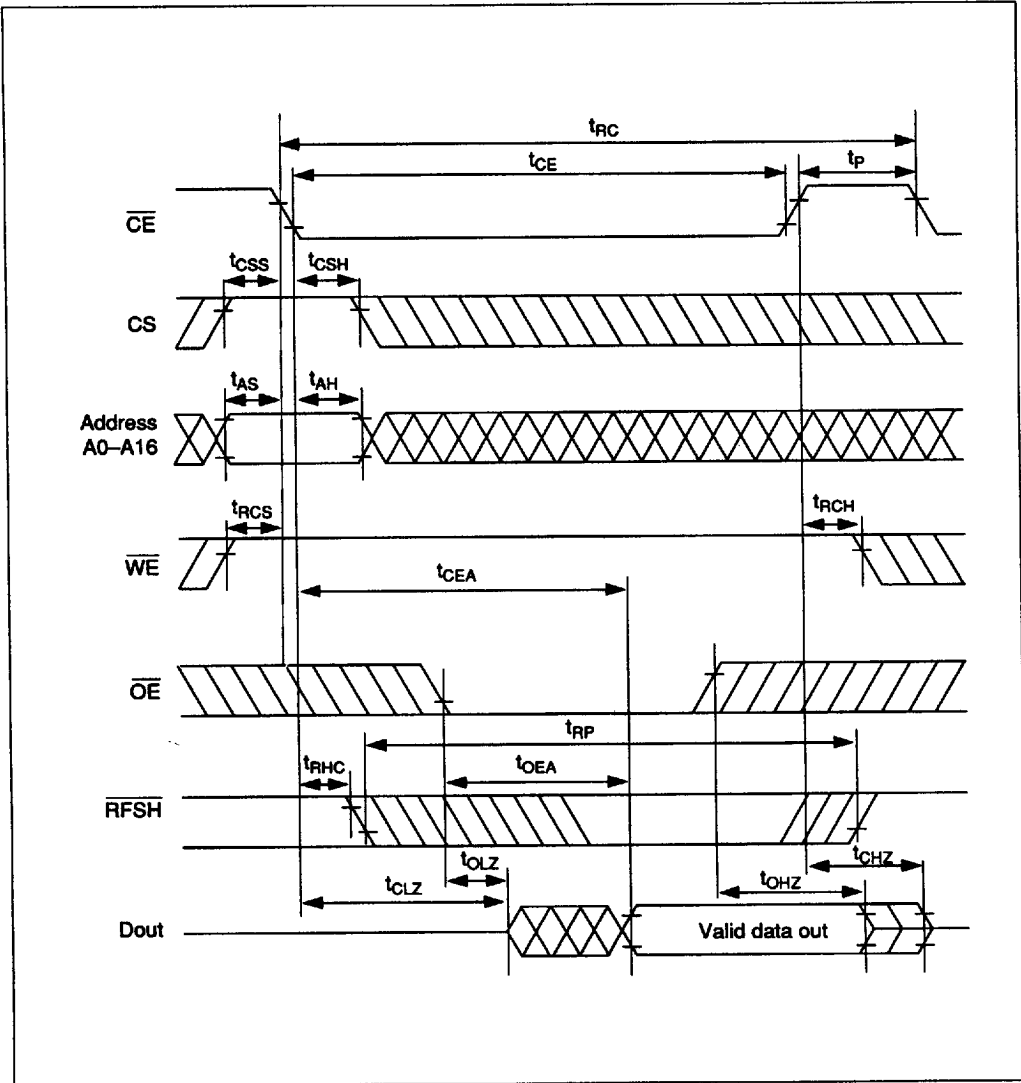
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Timing Waveforms

Read Cycle



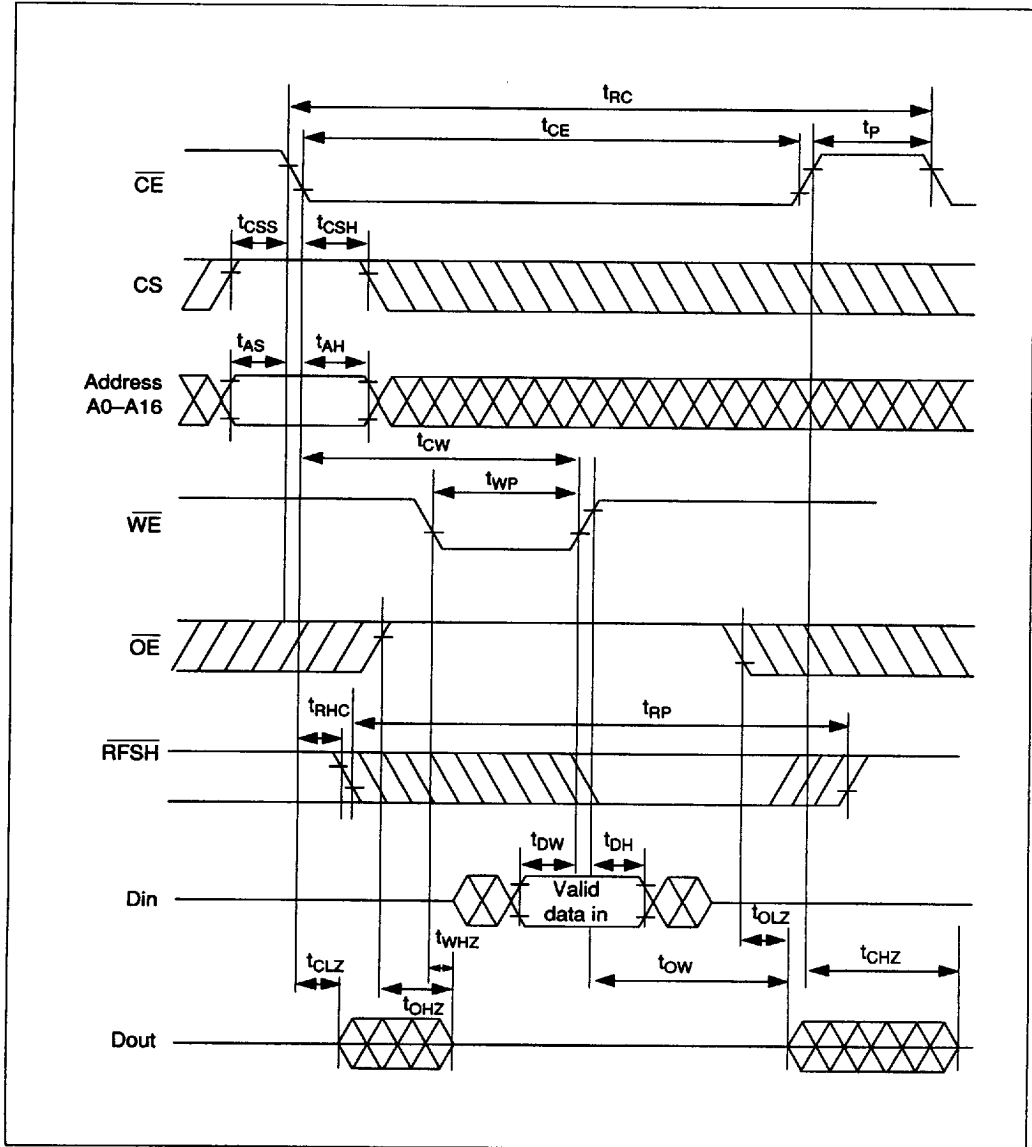
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## Write Cycle (OE clock)



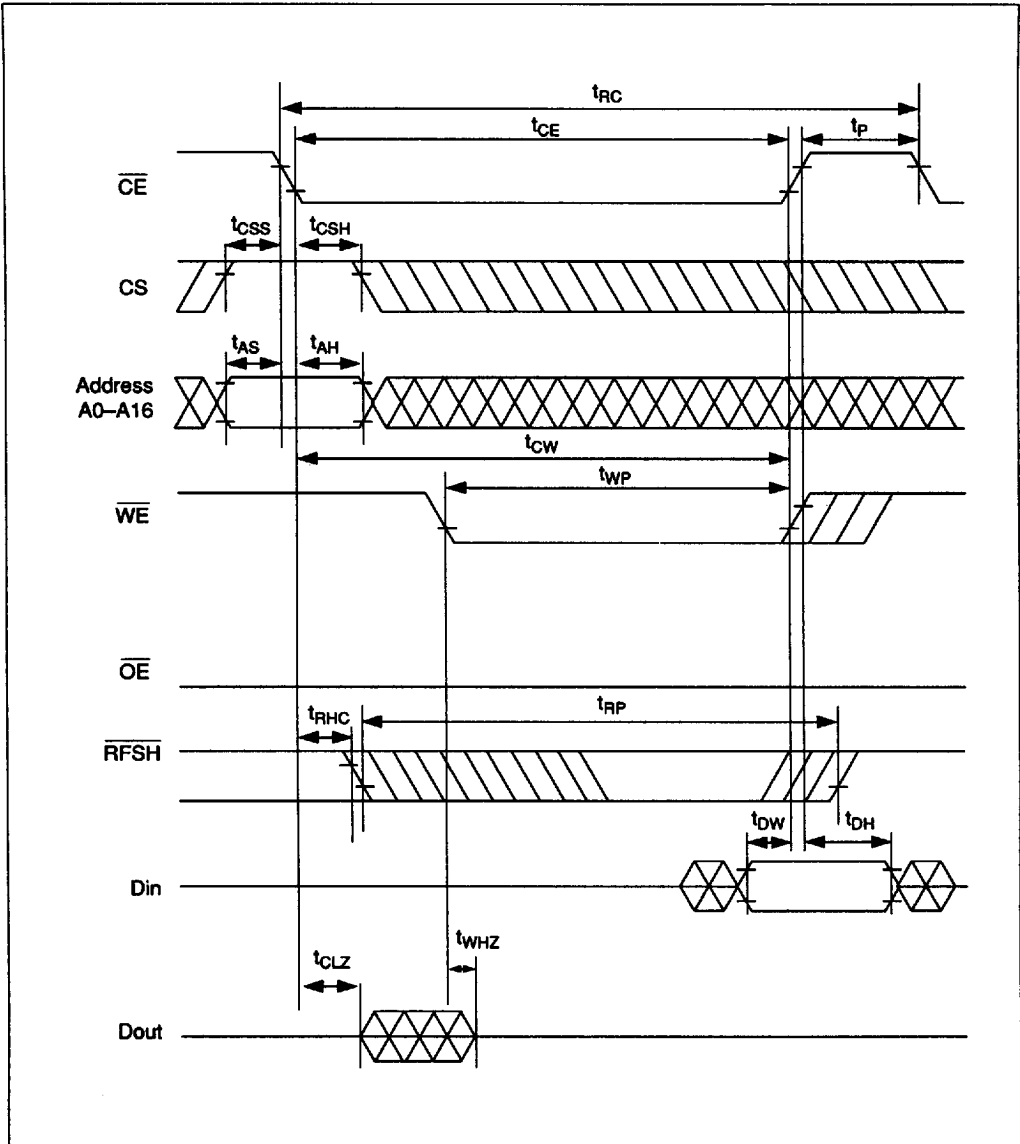
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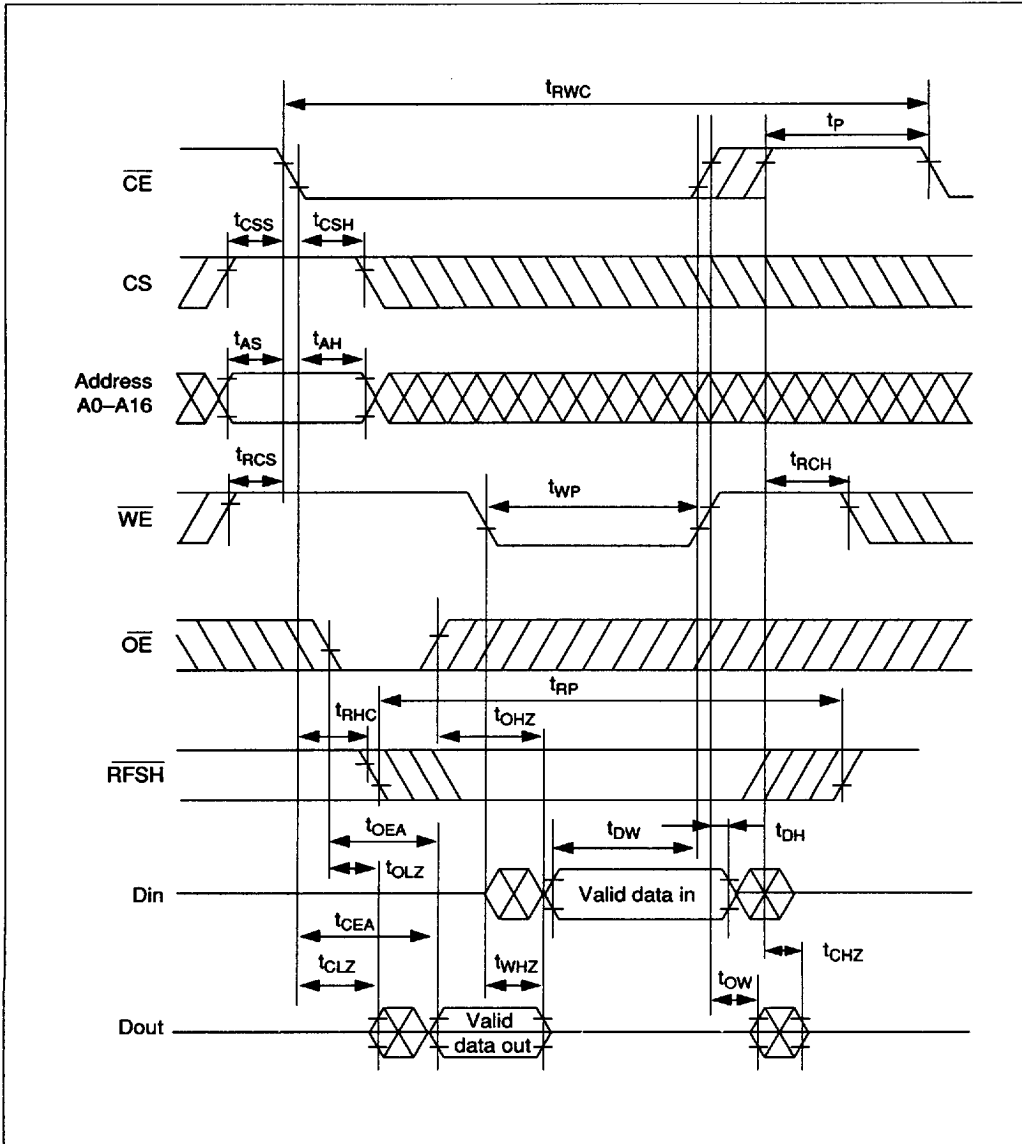
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Write Cycle ( $\overline{OE}$  Low Fix)



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## Read-Modify-Write Cycle



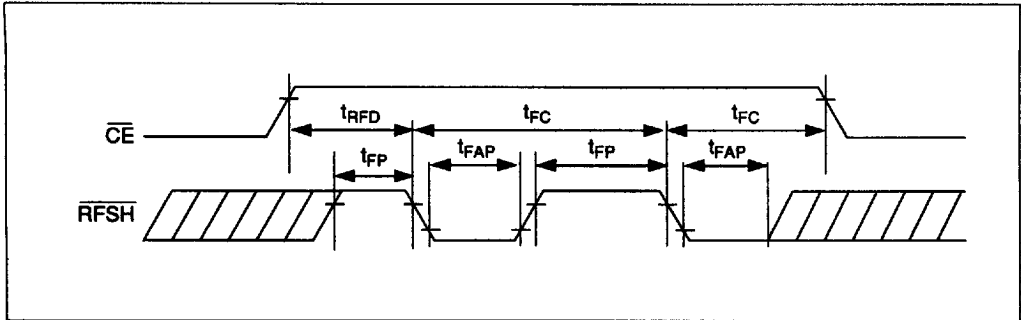
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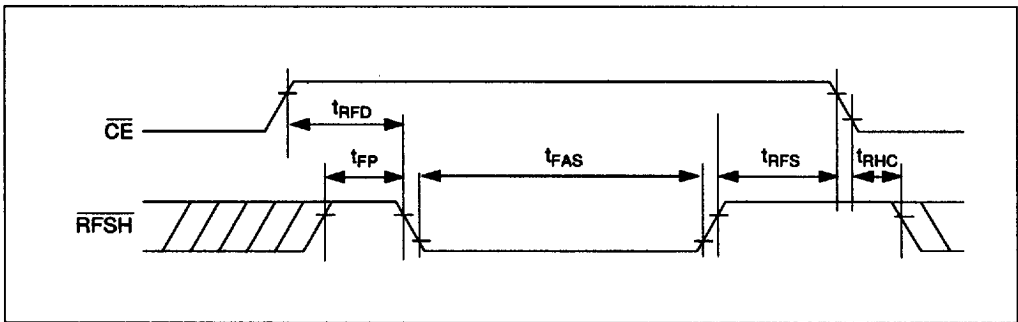
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Auto Refresh Cycle



Self Refresh Cycle



CS Standby Mode

