
HM51W4405BS Series

1,048,576-word $\times$ 4-bit Dynamic Random Access Memory

HITACHI

ADE-203-686A (Z)

Rev. 1.0

Nov. 29, 1996

Description

The Hitachi HM51W4405BS Series is a CMOS dynamic RAM organized 1,048,576-word $\times$ 4-bit. HM51W4405BS Series has realized higher density, higher performance and various functions by employing 0.8 μ m CMOS process technology and some new CMOS circuit design technologies. The HM51W4405BS Series offers Extended Data Out (EDO) Page Mode as a high speed access mode. It has the package variations of standard 26-pin plastic SOJ.

Features

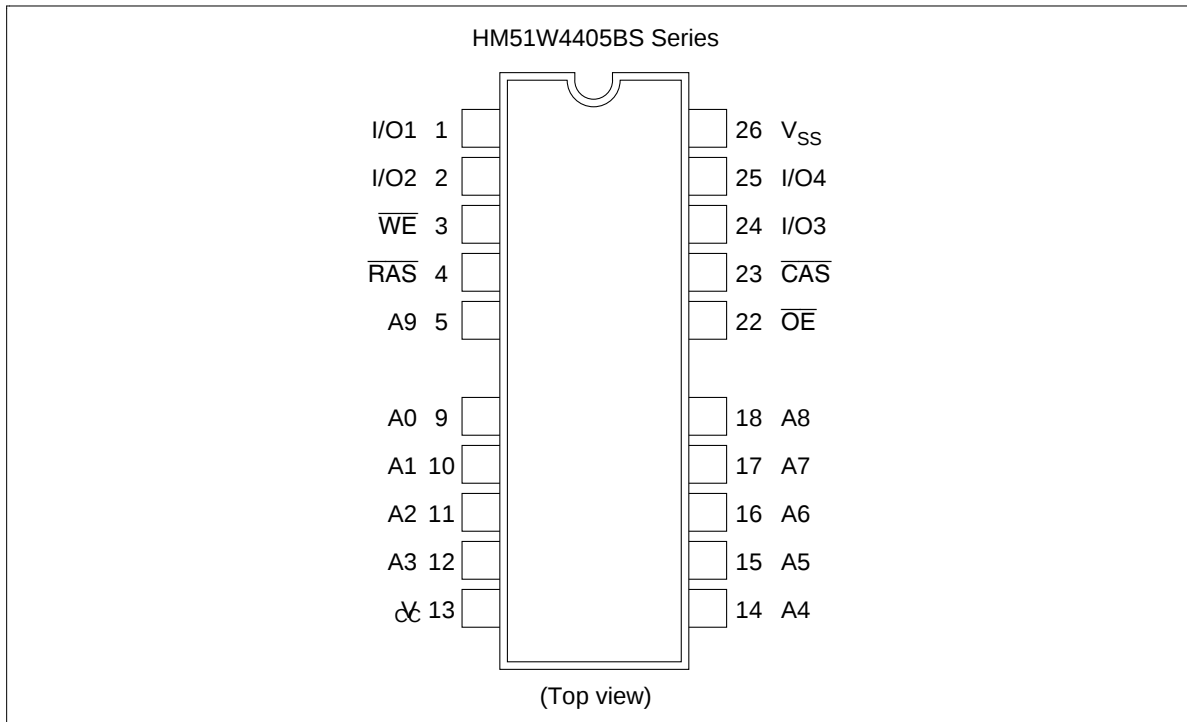
- Single 3.3 V (± 0.3 V) (HM51W4405BS-7)
- Single 3.3 V (+0.3 V/ -0.15 V) (HM51W4405BS-6R)
- High speed
 - Access time: 60/70 ns (max)
- Low power dissipation
 - Active mode: 288/252 mW (max)
 - Standby mode: 7.2 mW (max)
- EDO page mode capability
- 1024 refresh cycles : 16 ms
- 3 variations of refresh
 - $\overline{\text{RAS}}$ -only refresh
 - $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh
 - Hidden refresh

Ordering Information

Type No.	Access time	Package
HM51W4405BS-6R	60 ns	300-mil 26-pin plastic SOJ (CP-26/20D)
HM51W4405BS-7	70 ns	

HM51W4405BS Series

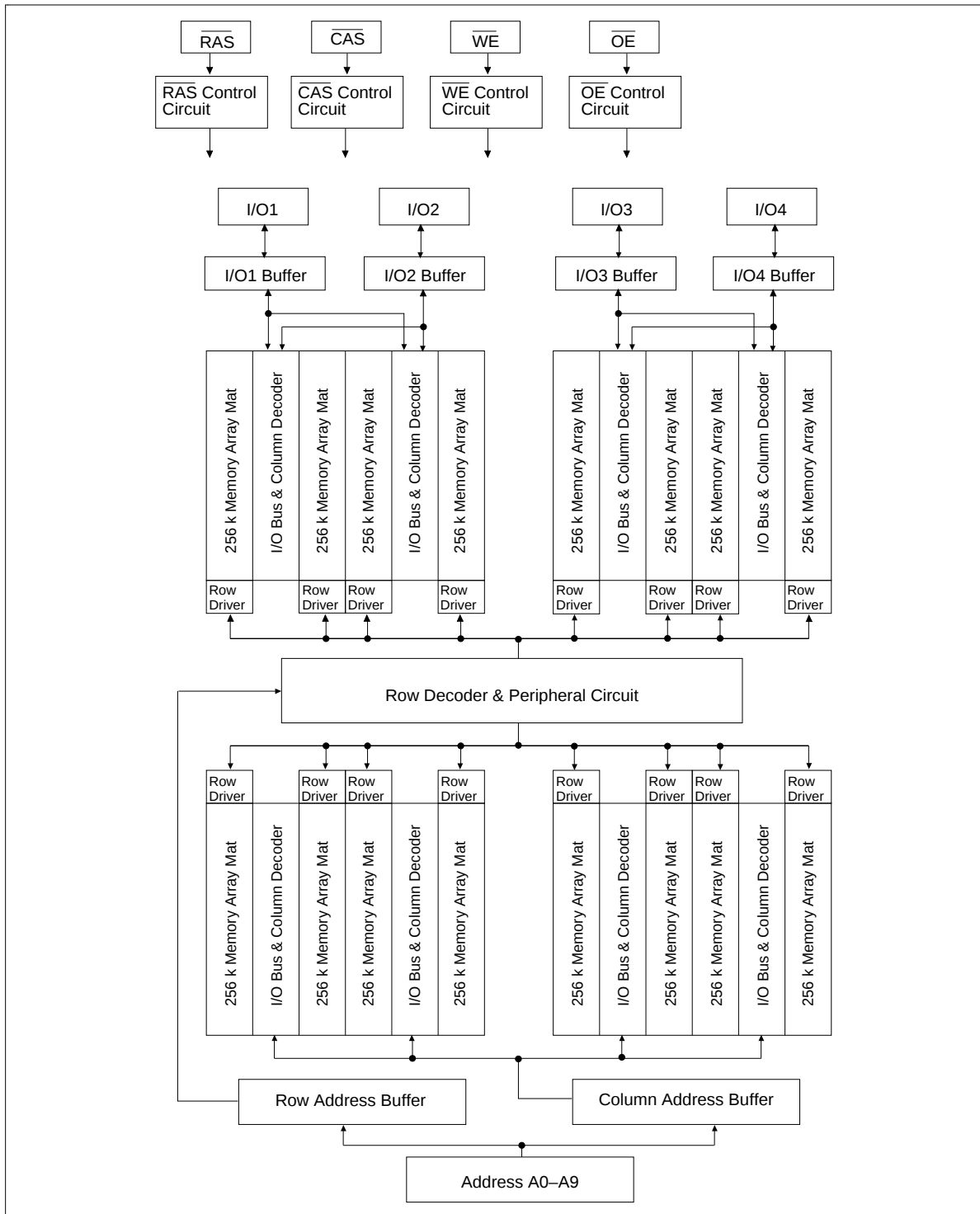
Pin Arrangement



Pin Description

Pin name	Function
A0 to A9	Address input - Row/Refresh: A0 to A9 - Column: A0 to A9
I/O1 to I/O4	Data-in/Data-out
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Read/Write enable
$\overline{OE}$	Output enable
V_{CC}	Power supply
V_{SS}	Ground

Block Diagram



HM51W4405BS Series

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	−0.5 to +4.6	V
Supply voltage relative to V_{SS}	V_{CC}	−0.5 to +4.6	V
Short circuit output current	I_{out}	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	−55 to +125	°C

Recommended DC Operating Conditions ($T_a = 0$ to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{SS}	0	0	0	V	
• (HM51W4405BS-6R)	V_{CC}	3.15	3.3	3.6	V	1
• (HM51W4405BS-7)	V_{CC}	3.0	3.3	3.6	V	1
Input high voltage	V_{IH}	2.0	—	$V_{CC} + 0.3$	V	1
Input low voltage	V_{IL}	−0.3	—	0.8	V	1

Note: 1. All voltage referred to V_{SS} .

HM51W4405BS Series

DC Characteristics

(Ta = 0 to +70°C, V_{CC} = 3.3 V +0.3 V/−0.15 V, V_{SS} = 0 V) (HM51W4405BS-6R)

(Ta = 0 to +70°C, V_{CC} = 3.3 V ±0.3 V, V_{SS} = 0 V) (HM51W4405BS-7)

HM51W4405B							
Parameter	Symbol	Min	Max	Min	Max	Unit	Test conditions
Operating current* ^{1, 2}	I _{CC1}	—	80	—	70	mA	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$ cycling, t _{RC} = min
Standby current	I _{CC2}	—	2	—	2	mA	TTL interface, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ = V _{IH} Dout = High-Z
Standby current	I _{CC2}	—	1	—	1	mA	CMOS interface $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ ≥ V _{CC} −0.2 V Dout = High-Z
$\overline{\text{RAS}}$ -only refresh current* ²	I _{CC3}	—	80	—	70	mA	t _{RC} = min
Standby current* ¹	I _{CC5}	—	4	—	4	mA	$\overline{\text{RAS}}$ = V _{IH} , $\overline{\text{CAS}}$ = V _{IL} Dout = enable
$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh current	I _{CC6}	—	80	—	70	mA	t _{RC} = min
EDO page mode current* ^{1, 3}	I _{CC4}	—	100	—	85	mA	t _{HPC} = min
Input leakage current	I _{LI}	−10	10	−10	10	μA	0 V ≤ Vin ≤ 4.6 V
Output leakage current	I _{LO}	−10	10	−10	10	μA	0 V ≤ Vout ≤ 4.6 V Dout = disable
Output high voltage	V _{OH}	2.4	V _{CC}	2.4	V _{CC}	V	High Iout = −2 mA
Output low voltage	V _{OL}	0	0.4	0	0.4	V	Low Iout = 2 mA

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.

2. Address can be changed twice or less while $\overline{\text{RAS}}$ = V_{IL}.

3. Address can be changed once or less while $\overline{\text{CAS}}$ = V_{IH}.

Capacitance

(Ta = 25°C, V_{CC} = 3.3 V +0.3 V/−0.15 V) (HM51W4405BS-6R)

(Ta = 25°C, V_{CC} = 3.3 V ±0.3 V) (HM51W4405BS-7)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C _{I1}	—	5	pF	1
Input capacitance (Clocks)	C _{I2}	—	7	pF	1
Output capacitance (Data-in, Data-out)	C _{I/O}	—	7	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.

2. $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ = V_{IH} to disable Dout.

HM51W4405BS Series

AC Characteristics

(Ta = 0 to +70°C, V_{CC} = 3.3 V +0.3 V/−0.15 V, V_{SS} = 0 V) (HM51W4405BS-6R)^{*1, *14, *15}

(Ta = 0 to +70°C, V_{CC} = 3.3 V ±0.3 V, V_{SS} = 0 V) (HM51W4405BS-7)^{*1, *14, *15}

Test Conditions

- Input rise and fall time : 2 ns
- Input level : V_{IL} = 0 V, V_{IH} = 3.0 V
- Input timing reference levels : 0.8 V, 2.0 V
- Output timing reference levels : 0.8 V, 2.0 V
- Output load: 1 TTL gate + C_L (100 pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

HM51W4405B							
Parameter	Symbol	-6R		-7		Unit	Notes
		Min	Max	Min	Max		
Random read or write cycle time	t _{RC}	104	—	124	—	ns	
$\overline{\text{RAS}}$ precharge time	t _{RP}	40	—	50	—	ns	
$\overline{\text{RAS}}$ pulse width	t _{RAS}	60	10000	70	10000	ns	17
$\overline{\text{CAS}}$ pulse width	t _{CAS}	10	10000	13	10000	ns	18
Row address setup time	t _{ASR}	0	—	0	—	ns	
Row address hold time	t _{RAH}	10	—	10	—	ns	
Column address setup time	t _{ASC}	0	—	0	—	ns	
Column address hold time	t _{CAH}	10	—	13	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	t _{RCD}	20	45	20	50	ns	8
$\overline{\text{RAS}}$ to column address delay time	t _{RAD}	15	30	15	35	ns	9
$\overline{\text{RAS}}$ hold time	t _{RSH}	15	—	18	—	ns	
$\overline{\text{CAS}}$ hold time	t _{CSH}	48	—	58	—	ns	21
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t _{CRP}	10	—	10	—	ns	
$\overline{\text{OE}}$ to Din delay time	t _{ODD}	15	—	18	—	ns	
$\overline{\text{OE}}$ delay time from Din	t _{DZO}	0	—	0	—	ns	
$\overline{\text{CAS}}$ setup time from Din	t _{DZC}	0	—	0	—	ns	
Transition time (rise and fall)	t _T	2	50	2	50	ns	7
Refresh period	t _{REF}	—	16	—	16	ms	

HM51W4405BS Series

Read Cycle

HM51W4405B							
Parameter	Symbol	Min	-6R	-7	Unit	Notes	
			Max	Min			Max
Access time from $\overline{\text{RAS}}$	t_{RAC}	—	60	—	70	ns	2, 3
Access time from $\overline{\text{CAS}}$	t_{CAC}	—	15	—	18	ns	3, 4, 13
Access time from address	t_{AA}	—	30	—	35	ns	3, 5, 13
Access time from $\overline{\text{OE}}$	t_{OAC}	—	15	—	18	ns	3
Read command setup time	t_{RCS}	0	—	0	—	ns	
Read command hold time to $\overline{\text{CAS}}$	t_{RCH}	0	—	0	—	ns	16
Read command hold time to $\overline{\text{RAS}}$	t_{RRH}	0	—	0	—	ns	16
Column address to $\overline{\text{RAS}}$ lead time	t_{RAL}	30	—	35	—	ns	
Column address to $\overline{\text{CAS}}$ lead time	t_{CAL}	18	—	23	—	ns	
Output buffer turn-off time	t_{OFF1}	—	15	—	15	ns	6,19
Output buffer turn-off time to $\overline{\text{OE}}$	t_{OFF2}	—	15	—	15	ns	6
$\overline{\text{CAS}}$ to Din delay time	t_{CDD}	15	—	18	—	ns	
$\overline{\text{RAS}}$ to Din delay time	t_{RDD}	15	—	18	—	ns	
$\overline{\text{WE}}$ to Din delay time	t_{WDD}	15	—	18	—	ns	
$\overline{\text{OE}}$ pulse width	t_{OEP}	15	—	18	—	ns	
Turn-off to $\overline{\text{RAS}}$	t_{OFR}	—	15	—	15	ns	6, 19
Turn-off to $\overline{\text{WE}}$	t_{WEZ}	—	15	—	15	ns	6
Output data hold time	t_{OH}	5	—	5	—	ns	
Output data hold time from $\overline{\text{RAS}}$	t_{OHR}	5	—	5	—	ns	
Read command hold time from $\overline{\text{RAS}}$	t_{RCHR}	60	—	70	—	ns	
Read command hold time from $\overline{\text{CAS}}$	t_{RCHC}	15	—	18	—	ns	
Read command hold time from column address	t_{RCHA}	30	—	35	—	ns	

HM51W4405BS Series

Write Cycle

HM51W4405B							
		-6R		-7			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Write command setup time	t_{WCS}	0	—	0	—	ns	10
Write command hold time	t_{WCH}	10	—	13	—	ns	
Write command pulse width	t_{WP}	10	—	10	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	10	—	13	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	10	—	13	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	ns	11
Data-in hold time	t_{DH}	10	—	13	—	ns	11

Read-Modify-Write Cycle

HM51W4405B							
		-6R		-7			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Read-modify-write cycle time	t_{RWC}	133	—	159	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	77	—	90	—	ns	10
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	32	—	38	—	ns	10
Column address to $\overline{WE}$ delay time	t_{AWD}	47	—	55	—	ns	10
$\overline{OE}$ hold time from $\overline{WE}$	t_{OEh}	15	—	18	—	ns	

Refresh Cycle

HM51W4405B							
		-6R		-7			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
$\overline{CAS}$ setup time (CBR refresh cycle)	t_{CSR}	10	—	10	—	ns	
$\overline{CAS}$ hold time (CBR refresh cycle)	t_{CHR}	10	—	10	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10	—	10	—	ns	
$\overline{CAS}$ precharge time in normal mode	t_{CPN}	10	—	13	—	ns	
CBR refresh cycle $\overline{WE}$ setup time	t_{WS}	0	—	0	—	ns	
CBR refresh cycle $\overline{WE}$ hold time	t_{WH}	10	—	10	—	ns	

HM51W4405BS Series

EDO Page Mode Cycle

HM51W4405B							
		-6R		-7			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
EDO page mode cycle time	t_{HPC}	25	—	30	—	ns	20
EDO page mode $\overline{CAS}$ precharge time	t_{CP}	10	—	13	—	ns	
EDO page mode $\overline{RAS}$ pulse width	t_{RASC}	—	100000	—	100000	ns	12
Access time from $\overline{CAS}$ precharge	t_{ACP}	—	35	—	40	ns	3, 13
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	35	—	40	—	ns	
Output data hold time from $\overline{CAS}$ low	t_{DOH}	3	—	3	—	ns	
$\overline{CAS}$ hold time referred $\overline{OE}$	t_{COL}	10	—	13	—	ns	
$\overline{CAS}$ to $\overline{OE}$ setup time	t_{COP}	5	—	5	—	ns	
Read command hold time from $\overline{CAS}$ precharge	t_{RCHP}	35	—	40	—	ns	

EDO Page Mode Read-Modify-Write Cycle

HM51W4405B							
		-6R		-7			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
EDO page mode read-modify-write cycle time	t_{HPCM}	66	—	77	—	ns	
EDO page mode read-modify-write cycle $\overline{CAS}$ precharge to $\overline{WE}$ delay time	t_{CPW}	52	—	60	—	ns	10

HM51W4405BS Series

Counter Test Cycle

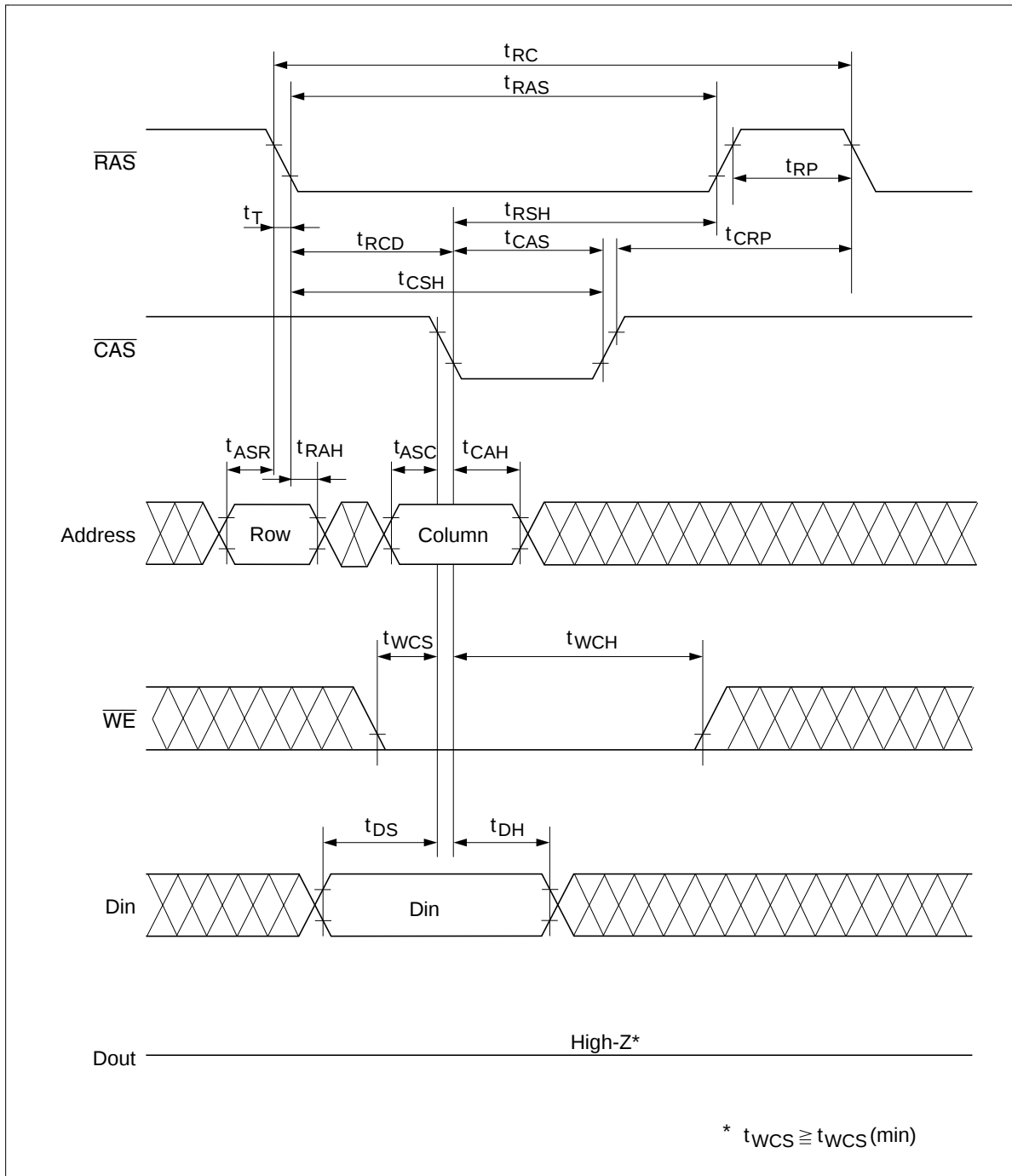
HM51W4405B							
		-6R		-7			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
CAS precharge time in counter test cycle	t _{CPT}	40	—	40	—	ns	

- Notes:
- AC measurements assume $t_T = 2$ ns.
 - Assumes that $t_{RCD} \leq t_{RCD}(\text{max})$ and $t_{RAD} \leq t_{RAD}(\text{max})$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
 - Measured with a load circuit equivalent to 1 TTL loads and 100 pF.
 - Assumes that $t_{RCD} \geq t_{RCD}(\text{max})$ and $t_{RAD} \leq t_{RAD}(\text{max})$.
 - Assumes that $t_{RCD} \leq t_{RCD}(\text{max})$ and $t_{RAD} \geq t_{RAD}(\text{max})$.
 - $t_{OFF1}(\text{max})$, $t_{OFF2}(\text{max})$, $t_{OFR}(\text{max})$ and $t_{WEZ}(\text{max})$ define the time at which the output achieves the open circuit condition and is not referred to output voltage levels.
 - $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
 - Operation with the $t_{RCD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met, $t_{RCD}(\text{max})$ is specified as a reference point only, if t_{RCD} is greater than the specified $t_{RCD}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
 - Operation with the $t_{RAD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met, $t_{RAD}(\text{max})$ is specified as a reference point only, if t_{RAD} is greater than the specified $t_{RAD}(\text{max})$ limit, then access time is controlled exclusively by t_{AA} .
 - t_{WCS} , t_{RWD} , t_{CWD} , t_{CPW} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}(\text{min})$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}(\text{min})$, $t_{CWD} \geq t_{CWD}(\text{min})$, $t_{CPW} \geq t_{CPW}(\text{min})$ and $t_{AWD} \geq t_{AWD}(\text{min})$, the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
 - These parameters are referred to $\overline{\text{CAS}}$ leading edge in an early write cycle and to $\overline{\text{WE}}$ leading edge in a delayed write or read-modify-write cycle.
 - t_{RASC} defines $\overline{\text{RAS}}$ pulse width in fast page mode cycles.
 - Access time is determined by the longest among t_{AA} , t_{CAC} and t_{ACP} .
 - An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles ($\overline{\text{RAS}}$ -only refresh cycle or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles is required.
 - In delayed write or read-modify-write cycles, $\overline{\text{OE}}$ must disable output buffer prior to applying data to the device.
 - Either t_{RCH} or t_{RRH} must be satisfied
 - $t_{RAS}(\text{min}) = t_{RWD}(\text{min}) + t_{RWL}(\text{min}) + t_T$ in read-modify-write cycle.
 - $t_{CAS}(\text{min}) = t_{CWD}(\text{min}) + t_{CWL}(\text{min}) + t_T$ in read-modify-write cycle.
 - Data output turns off and becomes high impedance from later rising edge of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$. Hold time and turn off time are specified by the timing specifications of later rising edge of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ between t_{OHR} and t_{OH} , and between t_{OFR} and t_{OFF} .
 - $t_{HPC}(\text{min})$ can be achieved during a series of EDO page mode early write cycles or EDO page mode read cycles. If both write and read operation are mixed in a EDO page mode $\overline{\text{RAS}}$ cycle (EDO page mode mix cycle (1), (2)), minimum value of $\overline{\text{CAS}}$ cycle t_{HPC} ($t_{CAS} + t_{CP} + 2t_T$) becomes greater than the specified $t_{HPC}(\text{min})$ value.
 - $t_{CSH}(\text{min})$ can be achieved when $t_{RCD} \leq t_{CSH}(\text{min}) - t_{CAS}(\text{min})$.
 - XXX: H or L (H: $V_{IH}(\text{min}) \leq V_{IN} \leq V_{IH}(\text{max})$, L: $V_{IL}(\text{min}) \leq V_{IN} \leq V_{IL}(\text{max})$)

//////: Invalid Dout

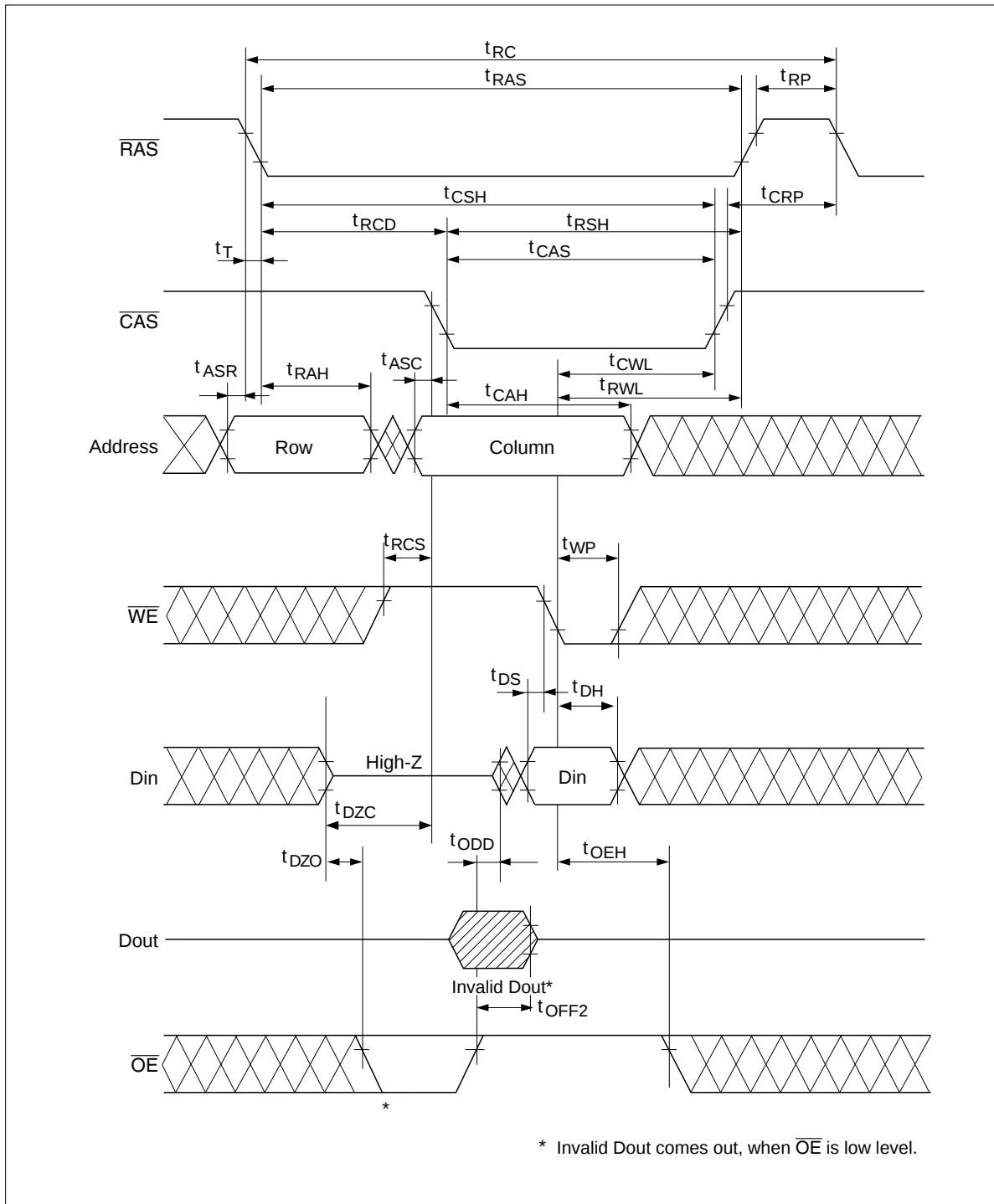
When the address, clock and input pins are not described on timing waveforms, their pins must be applied V_{IH} or V_{IL} .

Early Write Cycle

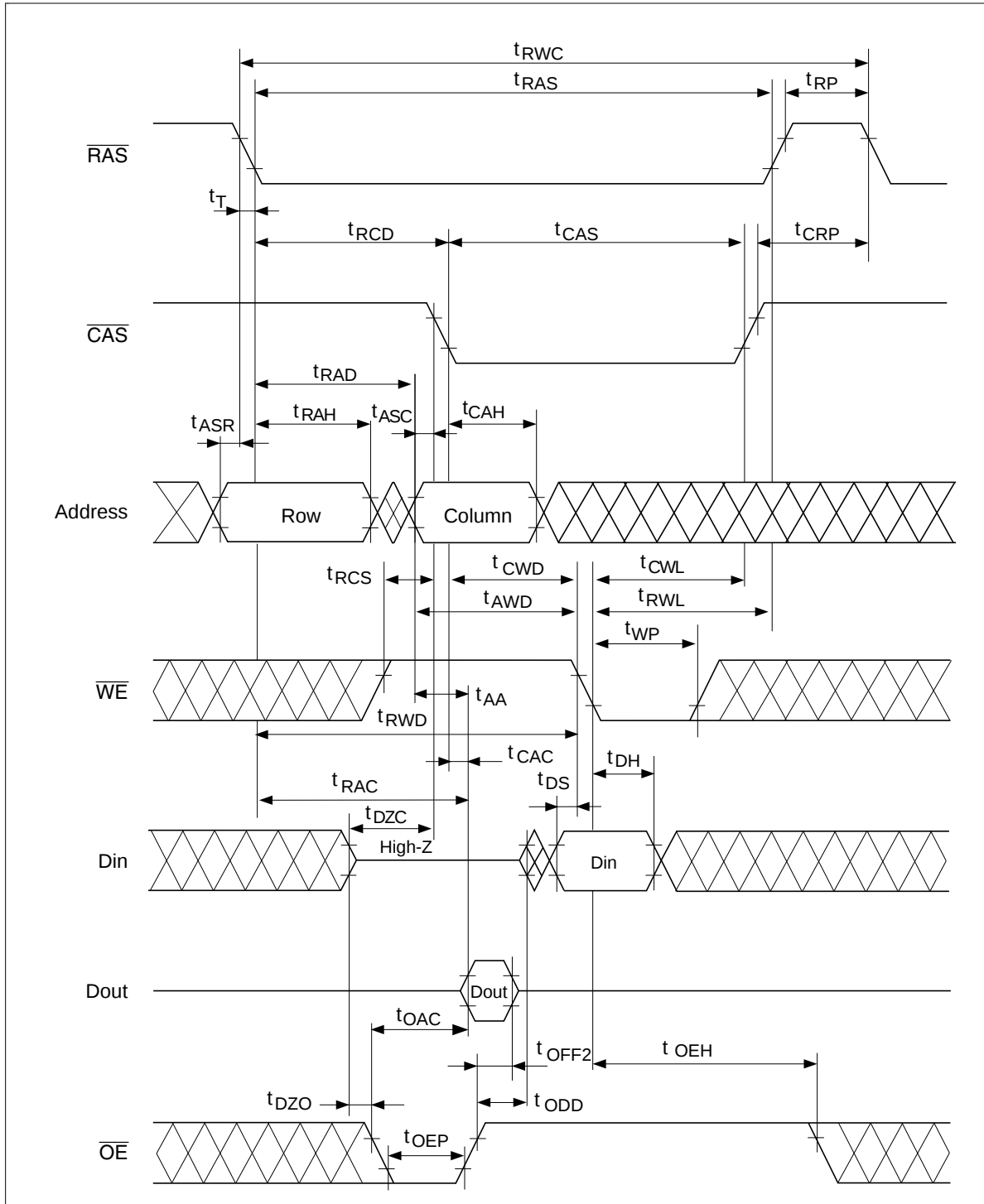


HM51W4405BS Series

Delayed Write Cycle

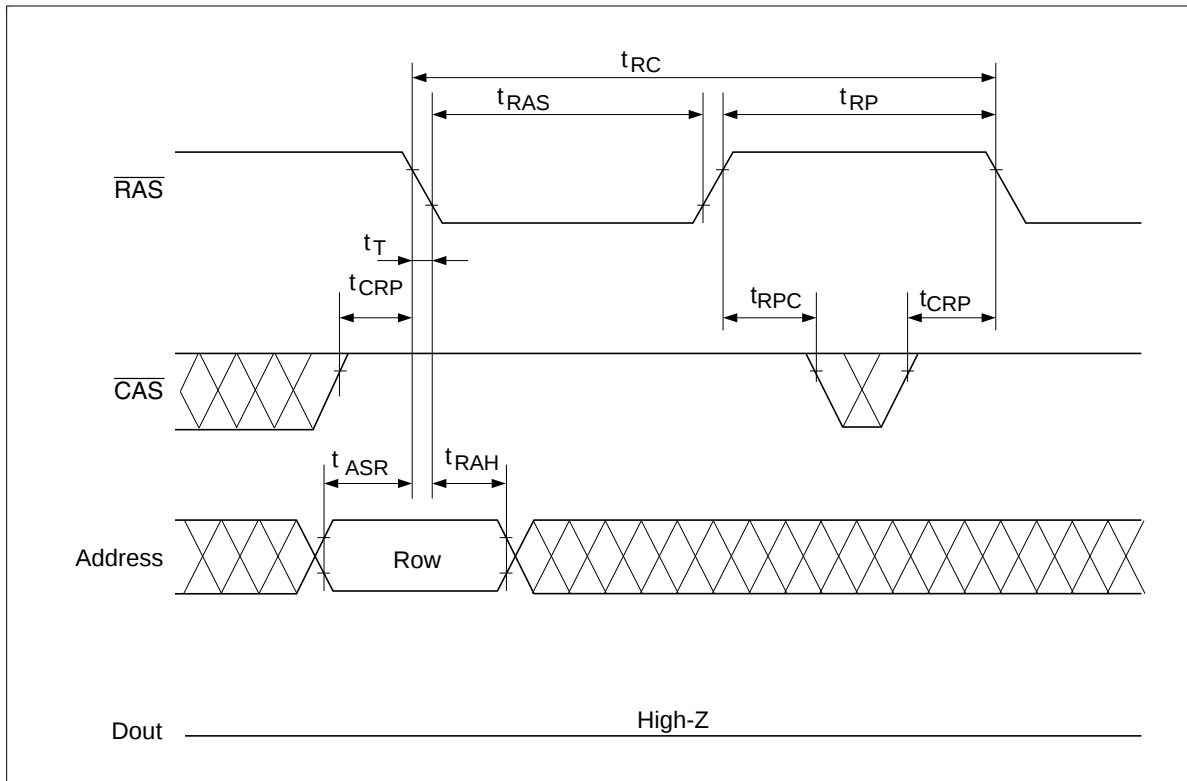


Read-Modify-Write Cycle

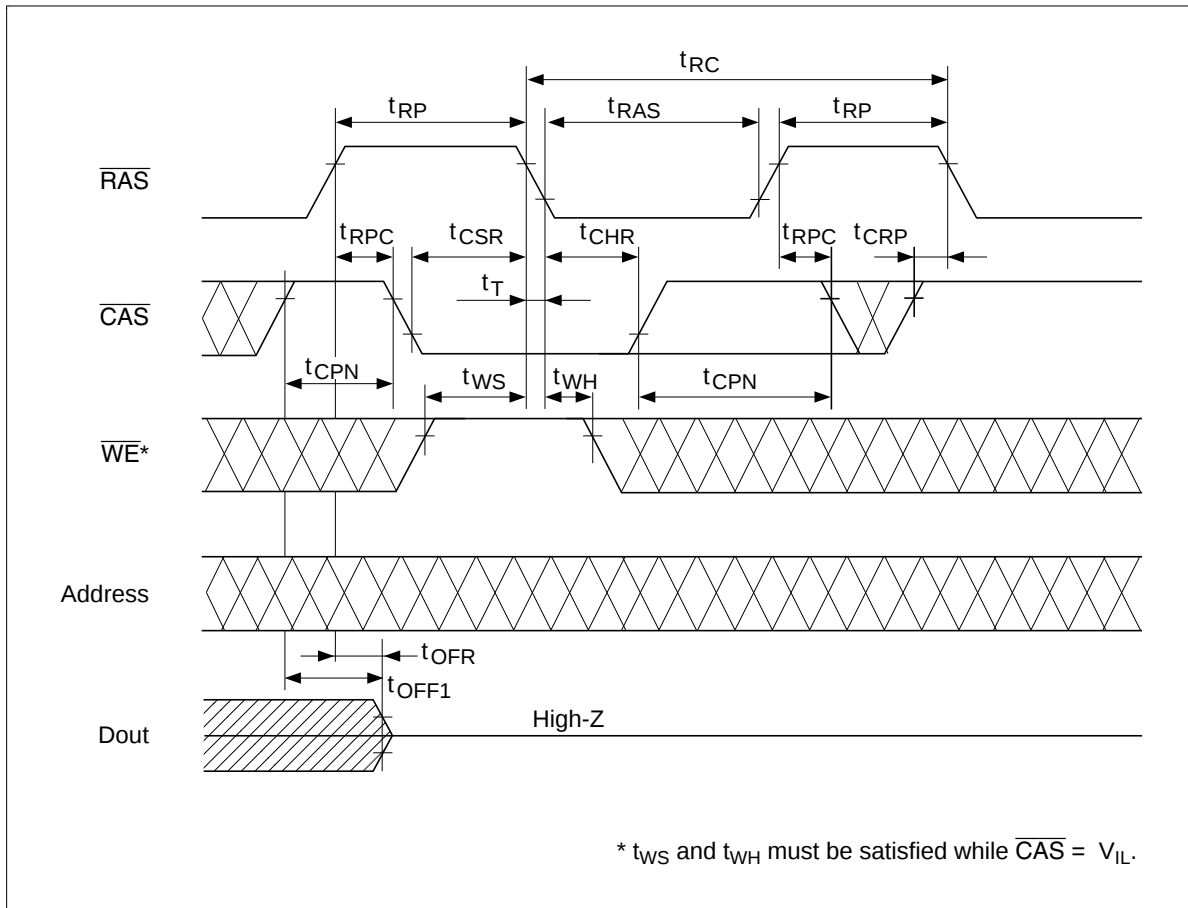


HM51W4405BS Series

$\overline{\text{RAS}}$ -Only Refresh Cycle

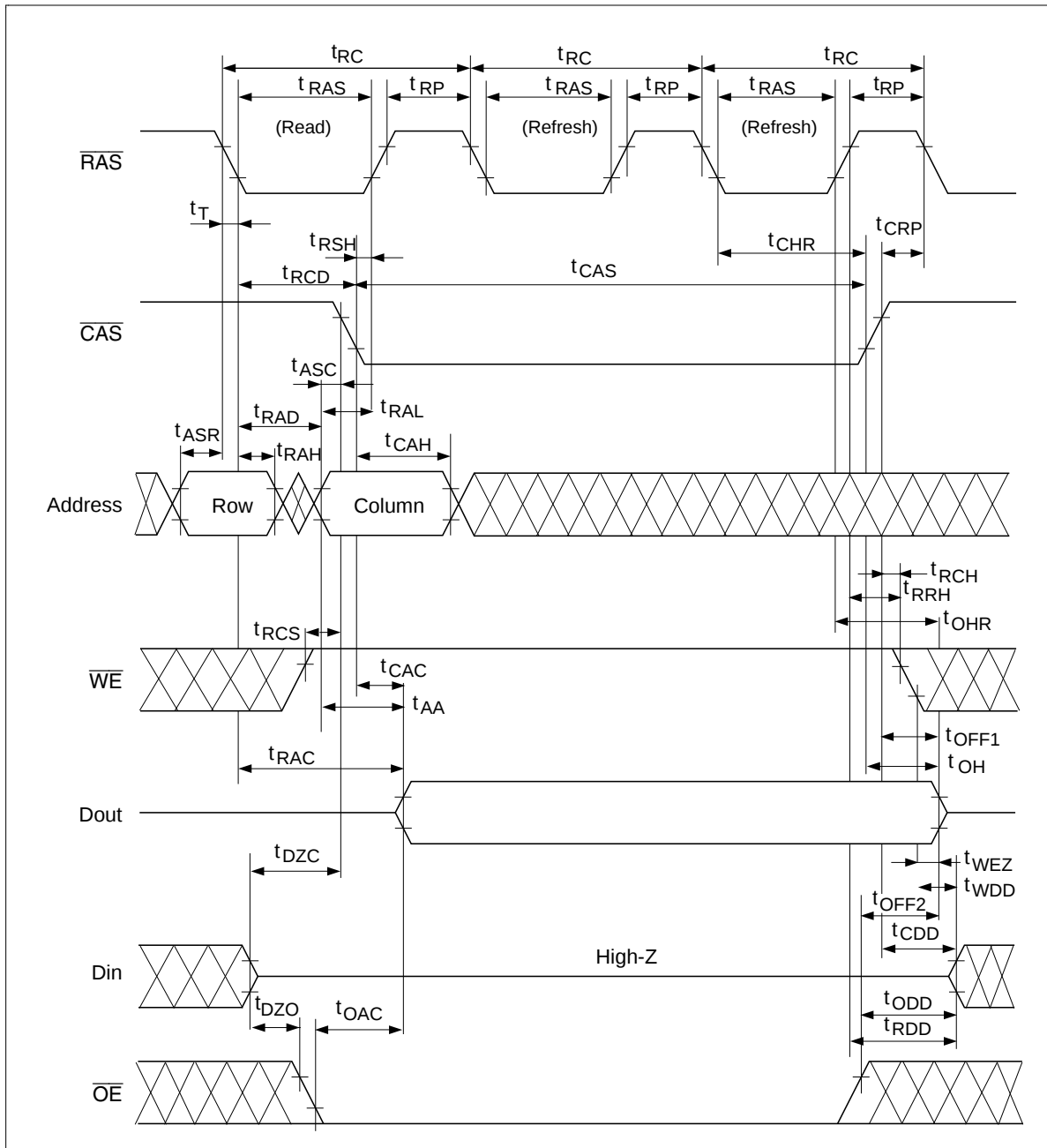


$\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$ Refresh Cycle

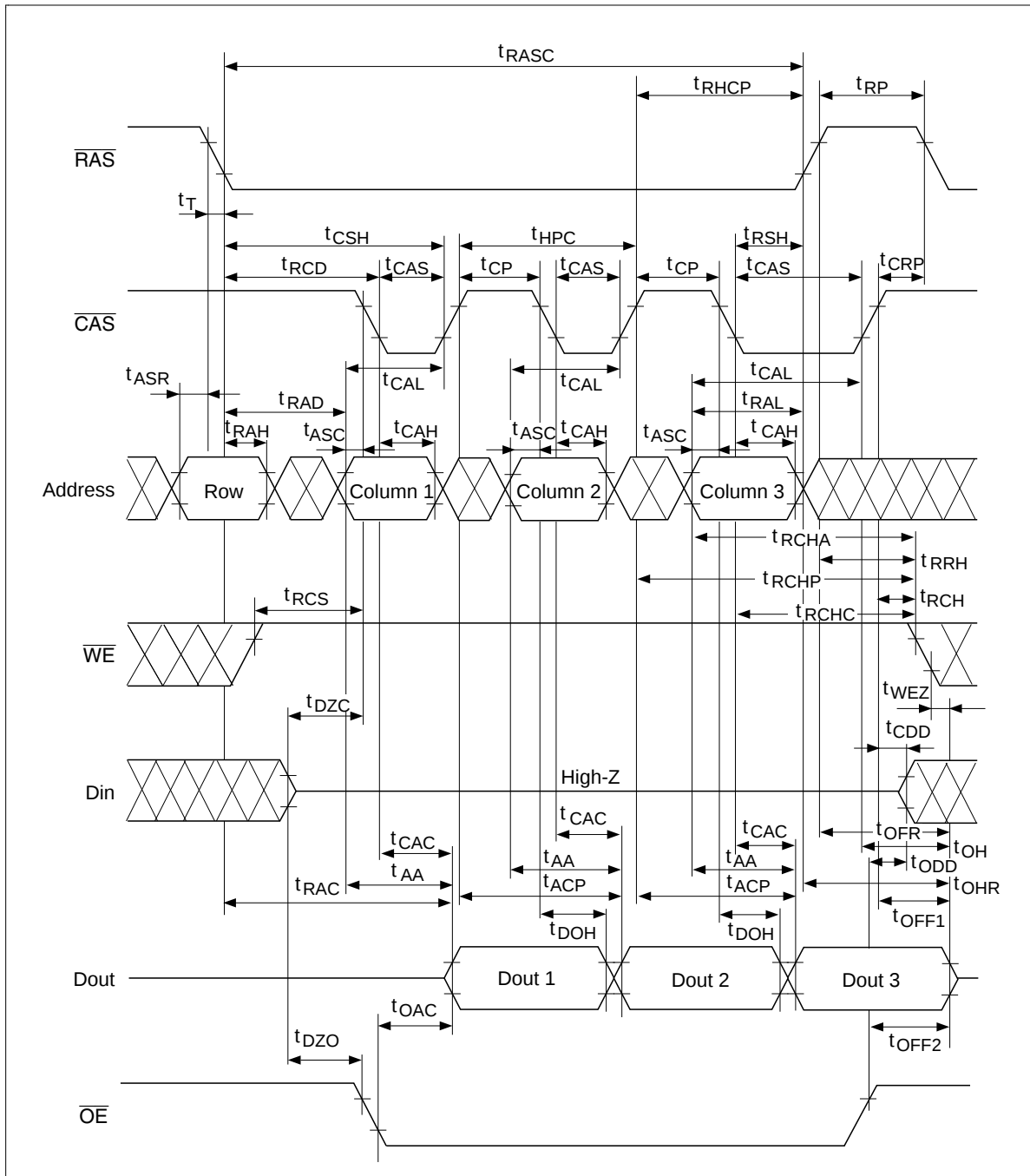


HM51W4405BS Series

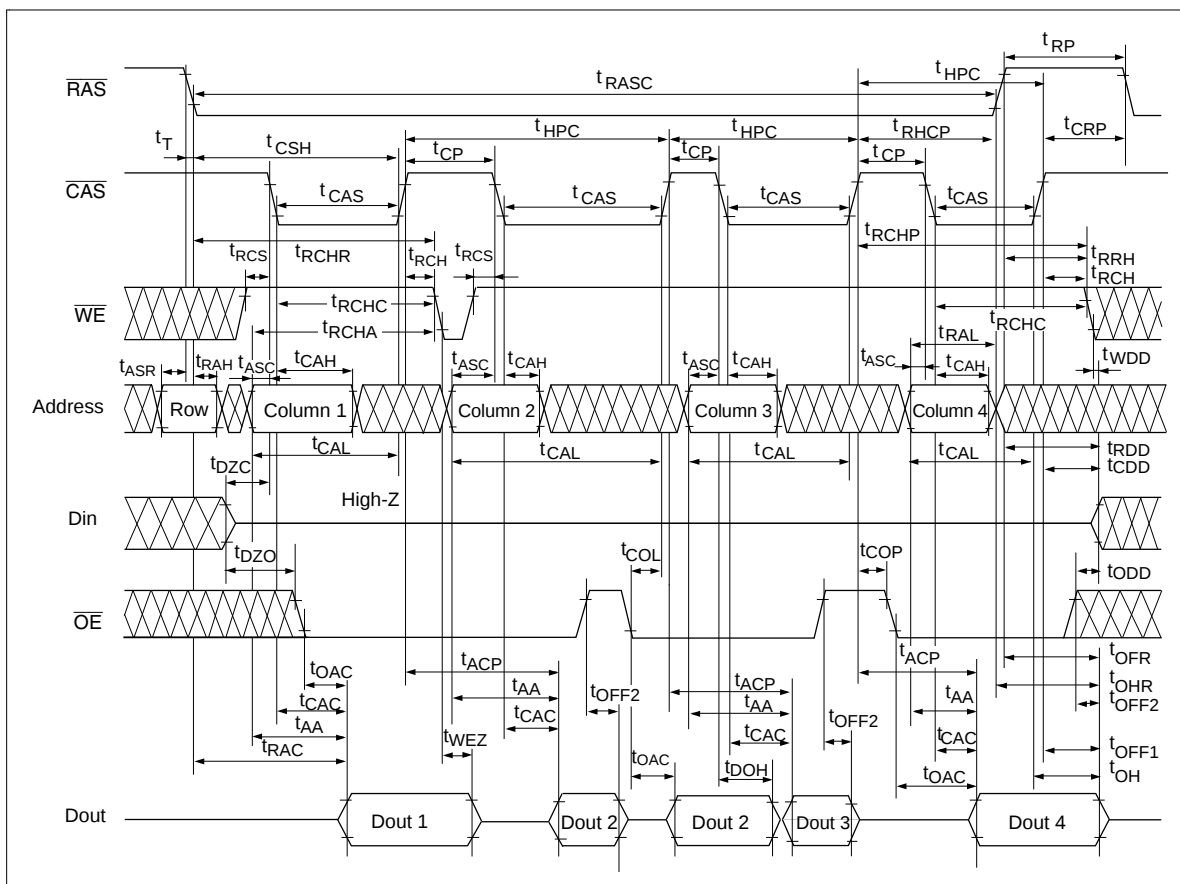
Hidden Refresh Cycle



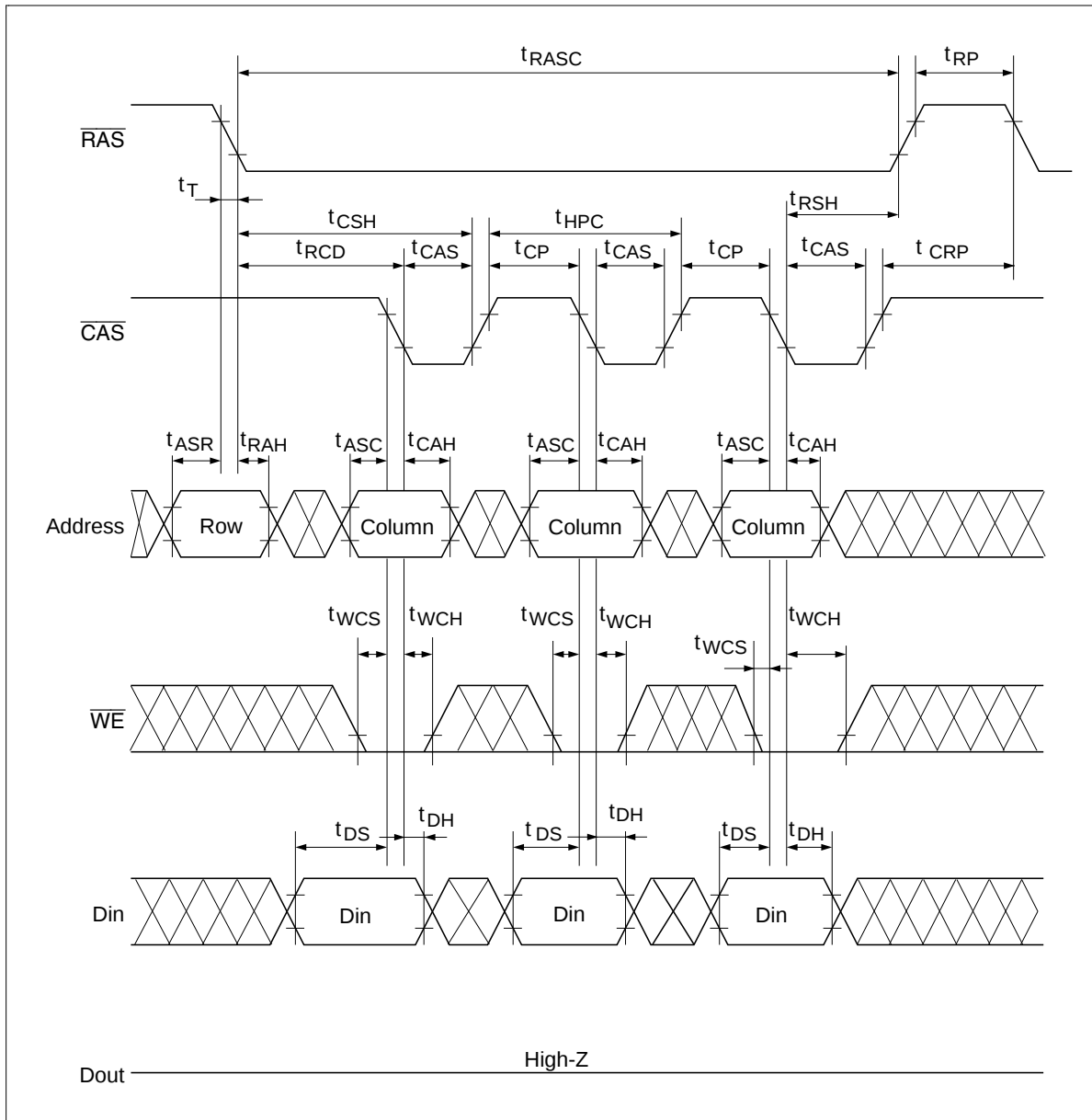
EDO Page Mode Read Cycle (t_{HPC} minimum cycle operation)



EDO Page Mode Read Cycle (High-Z control by $\overline{\text{WE}}$ and $\overline{\text{OE}}$)

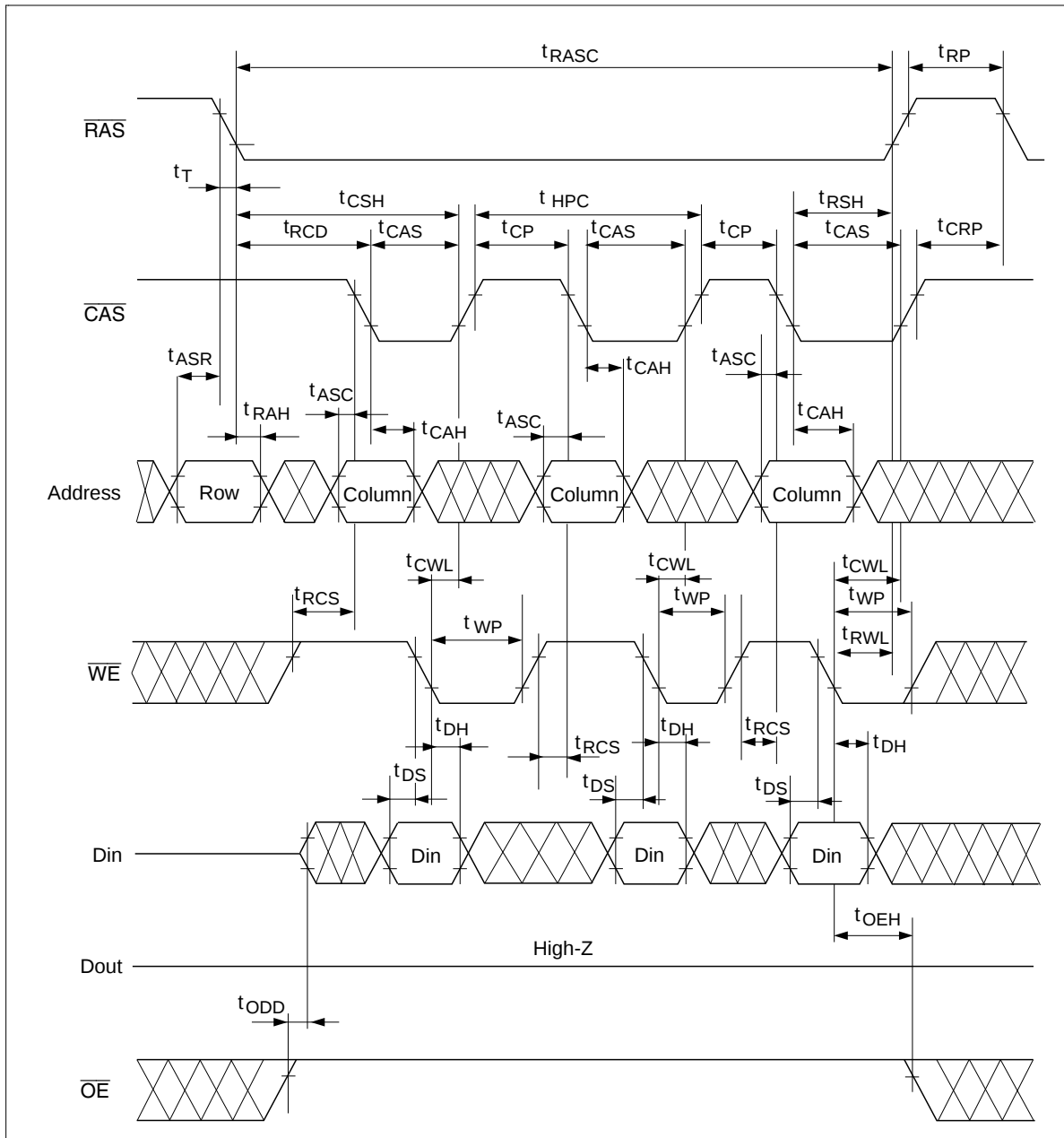


EDO Page Mode Early Write Cycle (t_{HPC} minimum cycle operation)

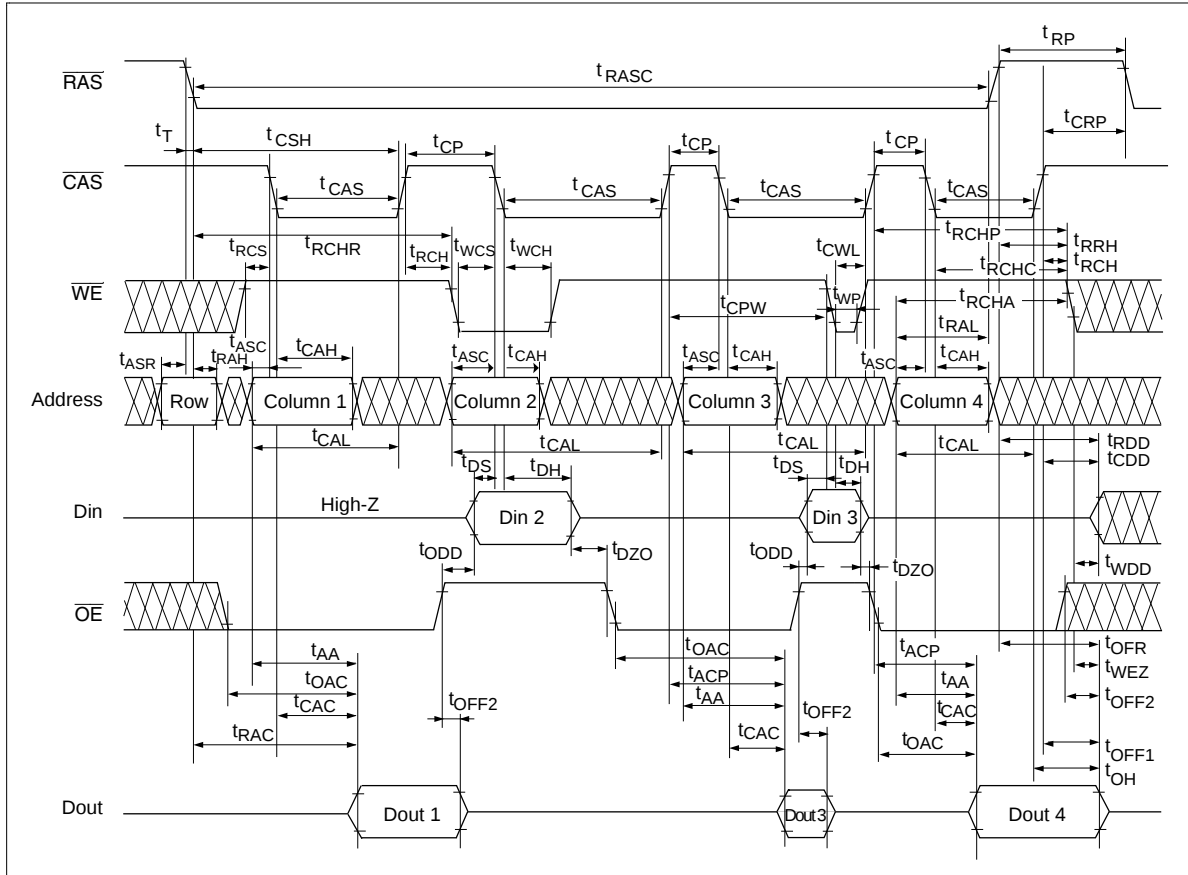


HM51W4405BS Series

EDO Page Mode Delayed Write Cycle

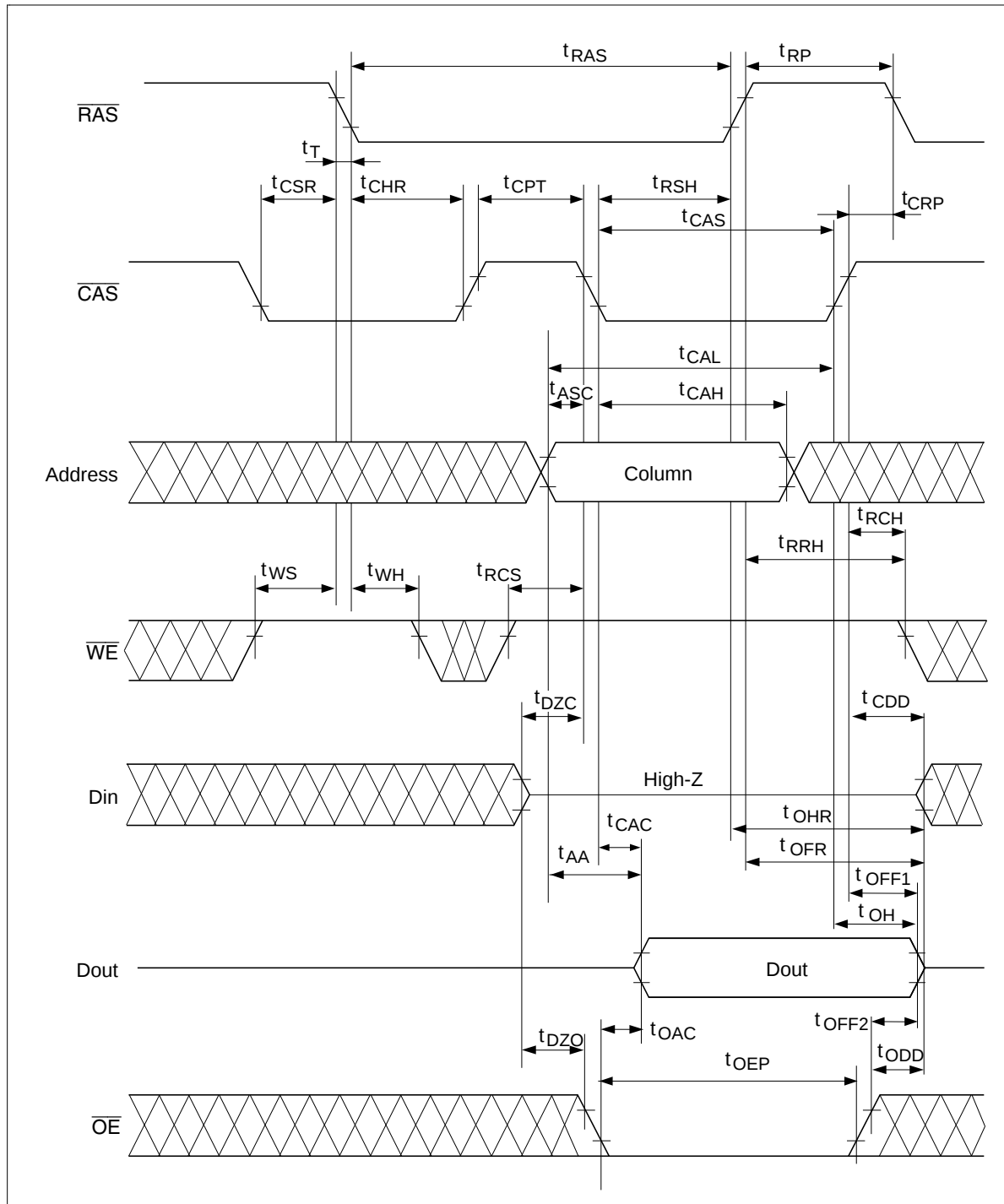


EDO Page Mode Mix Cycle (2) ^{*20}

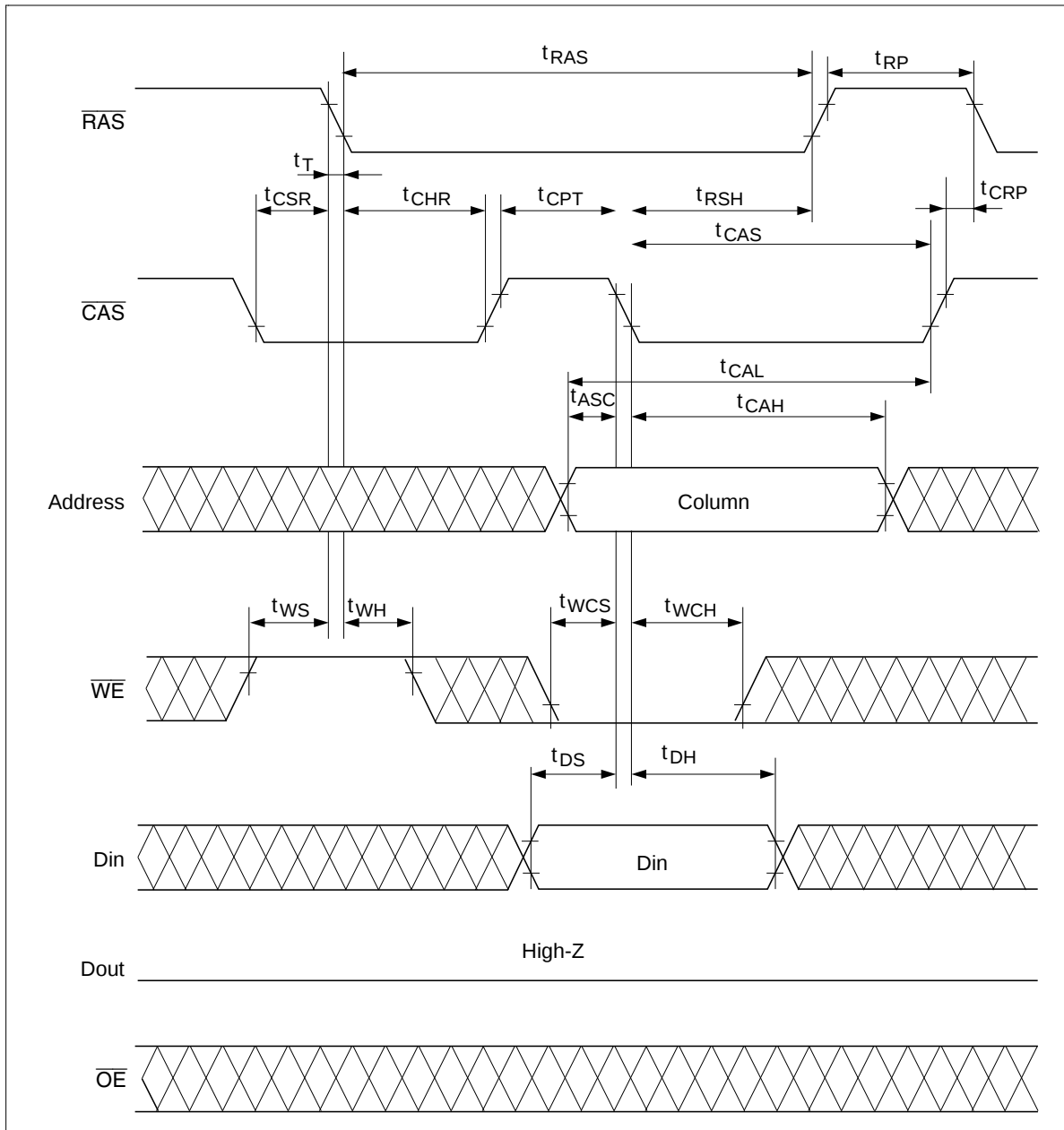


HM51W4405BS Series

$\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$ Refresh Counter Check Cycle (Read)



$\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$ Refresh Counter Check Cycle (Write)

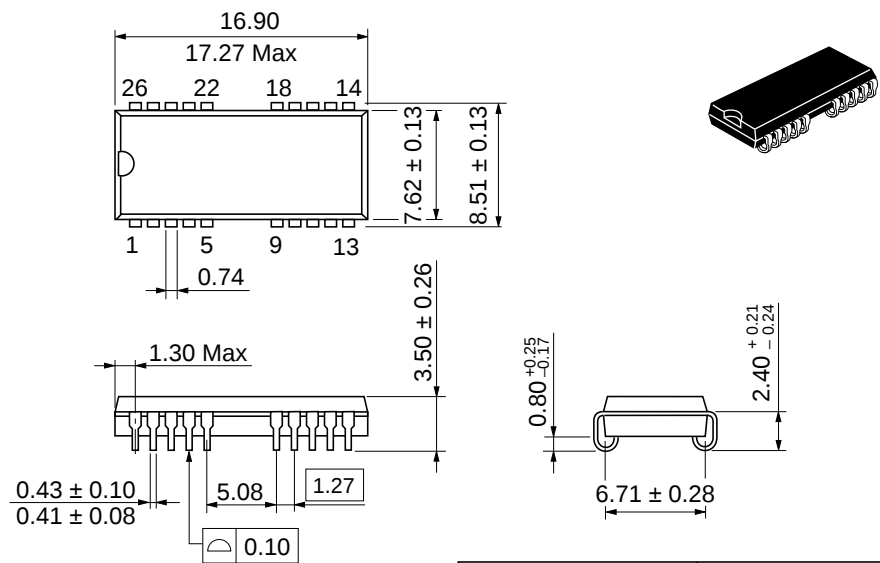


HM51W4405BS Series

Package Dimensions

HM51W4405BS Series (CP-26/20D)

Unit: mm



Hitachi Code	CP-26/20D
JEDEC Code	MO-077-AA
EIAJ Code	SC-633A
Weight	0.6 g

Disclaimer

When using this document, keep the following in mind:

1. This document may, wholly or partially, be subject to change without notice.
2. All rights are reserved: No one is permitted to reproduce or duplicate, in any form, the whole or part of this document without Hitachi's permission.
3. Hitachi will not be held responsible for any damage to the user that may result from accidents or any other reasons during operation of the user's unit according to this document.
4. Circuitry and other examples described herein are meant merely to indicate the characteristics and performance of Hitachi's semiconductor products. Hitachi assumes no responsibility for any intellectual property claims or other problems that may result from applications based on the examples described herein.
5. No license is granted by implication or otherwise under any patents or other rights of any third party or Hitachi, Ltd.
6. **MEDICAL APPLICATIONS:** Hitachi's products are not authorized for use in **MEDICAL APPLICATIONS** without the written consent of the appropriate officer of Hitachi's sales company. Such use includes, but is not limited to, use in life support systems. Buyers of Hitachi's products are requested to notify the relevant Hitachi sales offices when planning to use the products in **MEDICAL APPLICATIONS**.

Sales Offices

HITACHI

Hitachi, Ltd.

Semiconductor & IC Div.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100, Japan
Tel: Tokyo (03) 3270-2111
Fax: (03) 3270-5109

For further information write to:

Hitachi America, Ltd.
Semiconductor & IC Div.
2000 Sierra Point Parkway
Brisbane, CA. 94005-1835
U S A
Tel: 415-589-8300
Fax: 415-583-4207

Hitachi Europe GmbH
Electronic Components Group
Continental Europe
Dornacher Straße 3
D-85622 Feldkirchen
München
Tel: 089-9 91 80-0
Fax: 089-9 29 30 00

Hitachi Europe Ltd.
Electronic Components Div.
Northern Europe Headquarters
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA
United Kingdom
Tel: 0628-585000
Fax: 0628-778322

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 0104
Tel: 535-2100
Fax: 535-1533

Hitachi Asia (Hong Kong) Ltd.
Unit 706, North Tower,
World Finance Centre,
Harbour City, Canton Road
Tsim Sha Tsui, Kowloon
Hong Kong
Tel: 27359218
Fax: 27306071

HM51W4405BS Series

Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
1.0	Nov. 29, 1996	Initial issue		
