Description

The GM71C4260D/DL is the new generation dynamic RAM organized 262,144 x 16 bit. GM71C4260D/DL has realized higher density, higher performance and various functions by utilizing advanced CMOS process technology. The GM71C4260D/DL offers Fast Page Mode as a high speed access mode. Multiplexed address inputs permit the GM71C4260D/DL to be packaged in standard 400 mil 40 pin plastic SOJ, and standard 400 mil 40 pin plastic TSOP II. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V ± 10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

Features

- 262,144 Words x 16 Bit Organization
- Fast Page Mode Capability
- Single Power Supply (5V ± 10%)
- Fast Access Time & Cycle Time

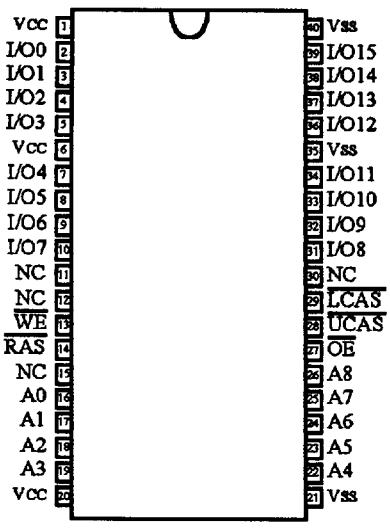
(Unit: ns)

	t_{RAC}	t_{CAC}	t_{RC}	t_{PC}
GM71C4260D/DL-60	60	15	104	45
GM71C4260D/DL-70	70	18	124	50
GM71C4260D/DL-80	80	20	144	55

- Low Power
  Active : 715/660/605 mW(MAX)
  Standby : 5.5mW (CMOS level : MAX)
  1.1mW (L-series)
- $\overline{RAS}$ Only Refresh, $\overline{CAS}$ before $\overline{RAS}$ Refresh, Hidden Refresh Capability
- All inputs and outputs TTL Compatible
- 512 Refresh Cycles/8ms
- 512 Refresh Cycles/128ms (L-series)
- Battery Back Up Operation (L-series)
- 2 $\overline{CAS}$ byte Control
- Self-Refresh Operation (GM71CS4260D/DL)

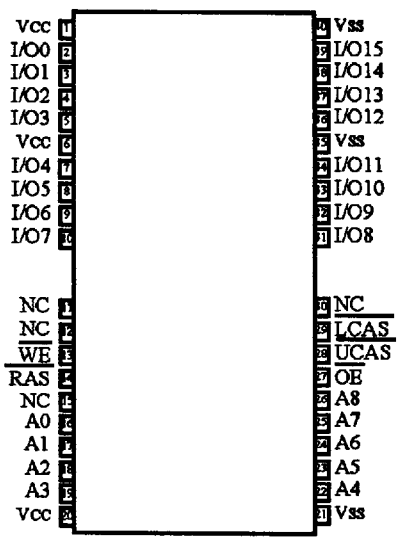
Pin Configuration

40 SOJ



(Top View)

40 (44) TSOP II



(Normal)

(Top View)

Pin Description

Pin	Function	Pin	Function
A0-A8	Address Inputs	$\overline{WE}$	Read/Write Enable
A0-A8	Refresh Address Inputs	$\overline{OE}$	Output Enable
I/O0-I/O15	Data-In/Out	Vcc	Power (+5V)
$\overline{RAS}$	Row Address Strobe	Vss	Ground
$\overline{UCAS}$, $\overline{LCAS}$	Column Address Strobe	NC	No Connection

Ordering Information

Type No.	Access Time	Package
GM71C4260D-/DLJ-60 GM71C4260D-/DLJ-70 GM71C4260D-/DLJ-80	60ns 70ns 80ns	400 Mil 40 Pin Plastic SOJ
GM71C4260D-/DLT-60 GM71C4260D-/DLT-70 GM71C4260D-/DLT-80	60ns 70ns 80ns	400 Mil 40 (44) Pin Plastic TSOP II (Normal Type)
GM71CS4260D-/DLJ-60 GM71CS4260D-/DLJ-70 GM71CS4260D-/DLJ-80	60ns 70ns 80ns	400 Mil 40 Pin Plastic SOJ
GM71CS4260D-/DLT-60 GM71CS4260D-/DLT-70 GM71CS4260D-/DLT-80	60ns 70ns 80ns	400 Mil 40 (44) Pin Plastic TSOP II (Normal Type)

Absolute Maximum Ratings*

Symbol	Parameter	Rating	Unit
T_A	Ambient Temperature under Bias	0 ~ 70	℃
T_{STG}	Storage Temperature (Plastic)	-55 ~ 125	℃
V_{IN}/V_{OUT}	Voltage on any Pin Relative to V_{SS}	-1.0 ~ 7.0	V
V_{CC}	Voltage on V_{CC} Relative to V_{SS}	-1.0 ~ 7.0	V
I_{OUT}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	1.0	W

*Note: Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

Recommended DC Operating Conditions* (T_A = 0 ~ 70℃)

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	-	6.5	V
V_{IL}	Input Low Voltage	-1.0	-	0.8	V

*Note: All voltage reffered to Vss

Truth Table

$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{WE}$	$\overline{OE}$	I/O0-I/O7	I/O8-I/O15	Operation
H	H	H	H	H	High-Z	High-Z	Standby
L	H	H	H	H	High-Z	High-Z	Refresh
L	L	H	H	L	D_{OUT}	High-Z	Lower Byte Read
L	H	L	H	L	High-Z	D_{OUT}	Upper Byte Read
L	L	L	H	L	D_{OUT}	D_{OUT}	Word Read
L	L	H	L	H	D_{IN}	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	D_{IN}	Upper Byte Write
L	L	L	L	H	D_{IN}	D_{IN}	Word Write
L	L	L	H	H	High-Z	High-Z	
H to L	L	H	-	-	High-Z	High-Z	CBR Refresh or Self Refresh
H to L	H	L	-	-	High-Z	High-Z	
H to L	L	L	-	-	High-Z	High-Z	

DC Electrical Characteristics (V_{CC} = 5V ± 10%, T_A = 0 ~ 70℃)

Symbol	Parameter		Min	Max	Unit	Note
V_{OH}	Output Level Output "H" Level Voltage (I_{OUT} = -2mA)		2.4	Vcc	V	
V_{OL}	Output Level Output "L" Level Voltage (I_{OUT} = 2mA)		0	0.4	V	
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{LCAS}$ or $\overline{UCAS}$ Cycling: t_{RC} = t_{RC} min)	60ns	-	130	mA	1, 2
		70ns	-	120		
		80ns	-	110		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$ = V_{IH}, D_{OUT} = High-Z)		-	2	mA	
I_{CC3}	$\overline{RAS}$-Only Refresh Current Average Power Supply Current (t_{RC} = t_{RC} min)	60ns	-	130	mA	2
		70ns	-	120		
		80ns	-	110		
I_{CC4}	Fast Page mode current Average Power Supply Current (t_{HPC} = t_{HPC} min)	60ns	-	130	mA	1, 3
		70ns	-	120		
		80ns	-	110		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$, $\overline{WE}$, $\overline{OE}$ ≥ Vcc-0.2V, D_{OUT}=High-Z)		-	1	mA	4
			-	200	μA	4,5
I_{CC6}	$\overline{CAS}$-before-$\overline{RAS}$ Refresh Current (t_{RC} = t_{RC} min)	60ns	-	130	mA	
		70ns	-	120		
		80ns	-	110		
I_{CC7}	Battery Back Up Current (Standby with CBR Refresh) (t_{RC}=125μs, t_{RAS} ≤ 1μs, $\overline{WE}$, $\overline{OE}$=V_{IH}, $\overline{LCAS}$, $\overline{UCAS}$=V_{IL}, D_{OUT}=High-Z)		-	300	μA	4, 5
I_{CC8}	Standby Current $\overline{RAS}$ = V_{IH} $\overline{LCAS}$ or $\overline{UCAS}$ = V_{IL} D_{OUT} = Enable		-	5	mA	1
I_{CC9}	Self-Refresh Mode Current ($\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$ ≤ 0.2V, D_{OUT} = High-Z)	GM71CS4260D	-	1	mA	6
		GM71CS4260DL	-	200	μA	
$I_{I(L)}$	Input Leakage Current Any Input (0V ≤ V_{IN} ≤ 6.5V)		-10	10	μA	
$I_{O(L)}$	Output Leakage Current (D_{OUT} is Disabled, 0V ≤ V_{OUT} ≤ 6.5V)		-10	10	μA	

Note: 1. Icc depends on output load condition when the device is selected. Icc(max) is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{LCAS}$ and $\overline{UCAS}$ = V_{IH}.
4. V_{IH} ≥ Vcc-0.2V, 0 ≤ V_{IL} ≤ 0.2V, Address can be changed once or less while $\overline{RAS}$=V_{IL}.
5. L-Series.
6. Self-refresh series. (GM71CS4260D/DL))

Capacitance (V_{CC} = 5V ± 10%, T_A = 25℃)

Symbol	Parameter	Min	Max	Unit	Note
C_{I1}	Input Capacitance (Address)	-	5	pF	1
C_{I2}	Input Capacitance (Clocks)	-	7	pF	1
$C_{I/O}$	Output Capacitance (Data-In/Out)	-	7	pF	1, 2

Note: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{OE}$= V_{IH} to disable D_{OUT}.

AC Characteristics (V_{CC} = 5V ± 10%, T_A = 0 ~ 70℃, Notes 1, 14, 15, 17, 18)

Test Conditions

Input rise and fall times : 2ns
Input level : V_{IL} = 0V , V_{IH} = 3.0V
Input timing reference level : 0.8V, 2.4V
Output timing reference level : 0.8V, 2.0V
Output load : 1TTL gate + C_L (100pF)
(Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Symbol	Parameter	GM71C(S)4263 D/DL-60		GM71C(S)4263 D/DL-70		GM71C(S)4263 D/DL-80		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	110		130	-	150	-	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	-	50	-	60	-	ns	
t_{CP}	$\overline{CAS}$ Percharge Time	10		10	-	10	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	70	10,000	80	10,000	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15		20	10,000	20	10,000	ns	
t_{ASR}	Row Address Set-up Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	10	-	10	-	ns	
t_{ASC}	Column Address Set-up Time	0	-	0	-	0	-	ns	19
t_{CAH}	Column Address Hold Time	15		15	-	15	-	ns	19
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	20	50	20	60	ns	8
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	ns	9
t_{RSH}	$\overline{RAS}$ Hold Time	15	-	20	-	20	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	-	70	-	80	-	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5	-	5	-	ns	20
t_{OED}	$\overline{OE}$ to D_{IN} Delay Time	15	-	20	-	20	-	ns	25
t_{DZO}	$\overline{OE}$ Delay Time from D_{IN}	0	-	0	-	0	-	ns	
t_{DZC}	$\overline{CAS}$ Setup Time from D_{IN}	0	-	0	-	0	-	ns	
t_T	TransitionTime (Rise and Fall)	3	50	3	50	3	50	ns	7
t_{REF}	Refresh Period	-	8	-	8	-	8	ms	
	Refresh Period (L-Series)	-	128	-	128	-	128	ms	

Read Cycle

Symbol	Parameter	GM71C(S)4260 D/DL-60		GM71C(S)4260 D/DL-70		GM71C(S)4260 D/DL-80		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	-	60	-	70	-	80	ns	2, 3
t_{CAC}	Access Time from $\overline{CAS}$	-	15	-	20	-	20	ns	3, 4, 13
t_{AA}	Access Time from Address	-	30	-	35	-	40	ns	3, 5, 13
t_{OAC}	Access Time from $\overline{OE}$	-	15	-	20	-	20	ns	3
t_{RCS}	Read Command Setup Time	0	-	0	-	0	-	ns	19
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	-	0	-	0	-	ns	16, 19
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	0	-	0	-	0	-	ns	16
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	-	35	-	40	-	ns	
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	-	0	-	0	-	ns	
t_{OH}	Output Data Hold Time	5	-	5	-	5	-	ns	
t_{OHO}	Output Data Hold Time from $\overline{OE}$	5	-	5	-	5	-	ns	
t_{OFF}	Output Buffer Turn-off Time	0	15	0	20	0	20	ns	6
t_{OEZ}	Output Buffer Turn-off Time from $\overline{OE}$	0	15	0	20	0	20	ns	6
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	15	-	20	-	20	-	ns	25
t_{OHR}	Output Data Hold Time from $\overline{RAS}$	5	-	5	-	5	-	ns	
t_{OFR}	Output Buffer Turn-off Time from $\overline{RAS}$	0	15	0	15	0	15	ns	6
t_{WEZ}	Output Buffer Turn-off Time from $\overline{WE}$	0	15	0	15	0	15	ns	6
t_{WED}	$\overline{WE}$ to D_{IN} Delay Time	15	-	20	-	20	-	ns	
t_{RDD}	$\overline{RAS}$ to D_{IN} Delay Time	15	-	20	-	20	-	ns	

Write Cycle

Symbol	Parameter	GM71C(S)4260 D/DL-60		GM71C(S)4260 D/DL-70		GM71C(S)4260 D/DL-80		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{WCS}	Write Command Setup Time	0	-	0	-	0	-	ns	10, 19
t_{WCH}	Write Command Hold Time	15	-	15	-	15	-	ns	19
t_{WP}	Write Command Pulse Width	10	-	10	-	10	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15	-	20	-	20	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15	-	20	-	20	-	ns	21
t_{DS}	Data-in Setup Time	0	-	0	-	0	-	ns	11, 21
t_{DH}	Data-in Hold Time	15	-	15	-	15	-	ns	11, 21

Read- Modify-Write Cycle

Symbol	Parameter	GM71C(S)4260 D/DL-60		GM71C(S)4260 D/DL-70		GM71C(S)4260 D/DL-80		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{RWC}	Read-Modify-Write Cycle Time	150	-	180	-	200	-	ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	80	-	95	-	105	-	ns	10
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	35	-	45	-	45	-	ns	10
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	50	-	60	-	65	-	ns	10
t_{OEH}	$\overline{OE}$ Hold Time from $\overline{WE}$	15	-	20	-	20	-	ns	

Refresh Cycle

Symbol	Parameter	GM71C(S)4260 D/DL-60		GM71C(S)4260 D/DL-70		GM71C(S)4260 D/DL-80		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	10	-	10	-	10	-	ns	19
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	10	-	10	-	10	-	ns	20
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	10	-	10	-	10	-	ns	19
t_{WRP}	WE Setup time(CBO refresh cycle)	10	-	10	-	10	-	ns	22

Fast Page Mode Cycle

Symbol	Parameter	GM71C(S)4260 D/DL-60		GM71C(S)4260 D/DL-70		GM71C(S)4260 D/DL-80		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	40	-	45	-	50	-	ns	
t_{RASC}	Fast Page Mode $\overline{RAS}$ Pulse Width	-	100,000	-	100,000	-	100,000	ns	12
t_{ACP}	Access Time from $\overline{CAS}$ Precharge	-	35	-	40	-	45	ns	3, 13, 20
t_{RHCP}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	35	-	40	-	45	-	ns	
t_{CPW}	Fast Page ModeRead-Modify-Write Cycle $\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	55	-	65	-	70	-	ns	10
t_{PCM}	Fast Page Mode Read-Modify-Write Cycle Time	80	-	95	-	100	-	ns	

Self-Refresh Mode

Symbol	Parameter	GM71CS4260 D/DL-60		GM71CS4260 D/DL-70		GM71CS4260 D/DL-80		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{RASS}	$\overline{RAS}$ Pulse Width (Self-Refresh)	100	-	100	-	100	-	us	
t_{RPS}	$\overline{RAS}$ Precharge Time (Self-Refresh)	110	-	130	-	150	-	ns	
t_{CHS}	$\overline{CAS}$ Hold Time (Self-Refresh)	-50	-	-50	-	-50	-	ns	21

Notes:

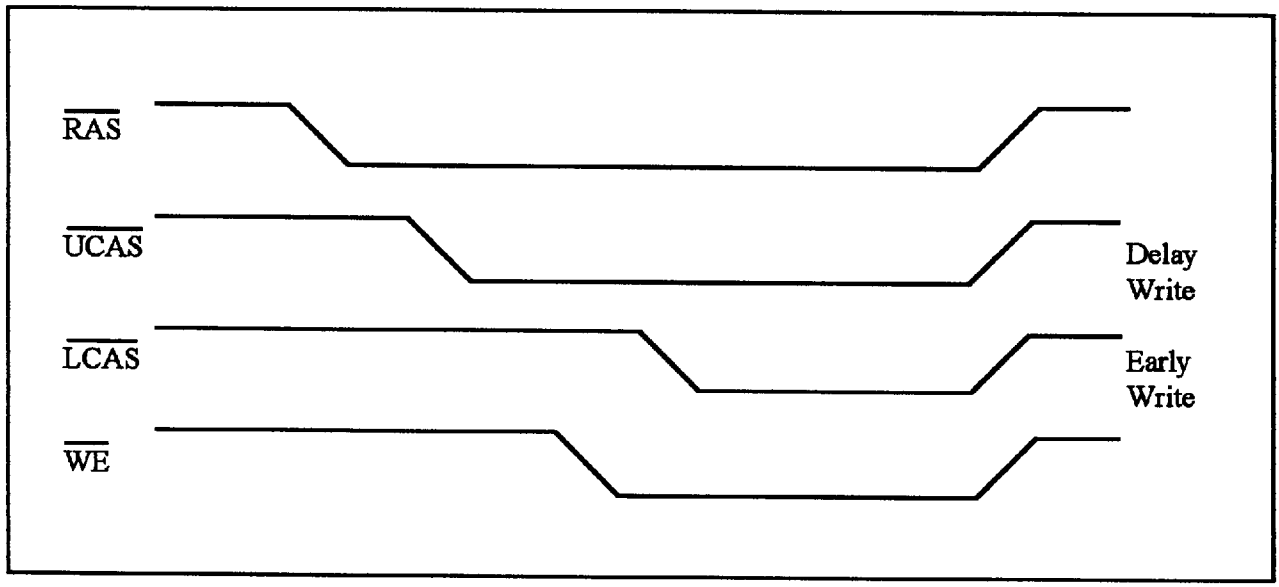
1. AC Measurements assume $t_T = 2$ns.
2. Assumes that $t_{RCD} \leq t_{RCD}(max)$ and $t_{RAD} \leq t_{RAD}(max)$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 1 TTL loads and 100pF.
4. Assumes that $t_{RCD} \geq t_{RCD}(max)$ and $t_{RAD} \leq t_{RAD}(max)$.
5. Assumes that $t_{RCD} \leq t_{RCD}(max)$ and $t_{RAD} \geq t_{RAD}(max)$.
6. $t_{OFF}(max)$, $t_{OEZ}(max)$, $t_{OFR}(max)$, and $t_{WEZ}(max)$ define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
7. $V_{IH}(min)$ and $V_{IL}(max)$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the $t_{RCD}(max)$ limit insures that $t_{RAC}(max)$ can be met, $t_{RCD}(max)$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{RCD}(max)$ limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the $t_{RAD}(max)$ limit insures that $t_{RAC}(max)$ can be met, $t_{RAD}(max)$ is specified as a reference point only; if t_{RAD} is greater than the specified $t_{RAD}(max)$ limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only ; if $t_{WCS} \geq t_{WCS}(min)$, the cycle is an early write cycle and thedata out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}(min)$, $t_{CWD} \geq t_{CWD}(min)$, $t_{AWD} \geq t_{AWD}(min)$ and $t_{CPW} \geq t_{CPW}(min)$, the cycle is a read modify write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referred to $\overline{UCAS}$ and $\overline{LCAS}$ leading edge in early write cycle and to $\overline{WE}$ leading edge in a delayed write or a read modify write cycle.
12. t_{RASC} defines $\overline{RAS}$ pulse width in Fast Page mode cycles.
13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
14. An initial pause of 100μs is required after power up followed by a minimum of eight initialization cycles ($\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle). If the internal refresh counter is used, a minimum of eitht $\overline{CAS}$ before $\overline{RAS}$ refresh cycles is required.

15. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device. After $\overline{RAS}$ is reset, if $t_{OEH} \geq t_{CWL}$, the I/O pin will remain open circuit (high impedance); if $t_{OEH} \geq t_{CWL}$, invalid data will be out at each I/O.
16. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
17. When both $\overline{LCAS}$ and $\overline{UCAS}$ go low at the same time, all 16-bits data are written into the device. $\overline{LCAS}$ and $\overline{UCAS}$ cannot be straggered within the same write/read cycles.
18. All the V_{CC} and V_{SS} pins shall be supplied with the same voltages.
19. t_{ASC}, t_{CAH}, t_{RCS}, t_{RCH}, t_{WCS}, t_{WCH}, t_{CSR} and t_{RPC} are determined by the earlier falling edge of $\overline{UCAS}$ or $\overline{LCAS}$.
20. t_{CRP}, t_{CHR}, t_{ACP} and t_{CPW} are determined by the later rising edge of $\overline{UCAS}$ or $\overline{LCAS}$.
21. t_{CWL}, t_{DH}, t_{DS} and t_{CHS} should be satisfied by both $\overline{UCAS}$ and $\overline{LCAS}$.
22. t_{CPN} and t_{CP} are determined by the time that both $\overline{UCAS}$ and $\overline{LCAS}$ are high.
23. When output buffers are enabled once, sustain the low impedance state until valid data is obtained. When output buffer is turned on and off within a very short time, generally it causes large V_{CC}/V_{SS} line noise, which causes to degrade V_{IH} min/V_{IL} max level.
24. Either t_{OED} or t_{CDD} most be satisfied.
25. Either t_{DZO} or t_{DZC} most be satisfied.

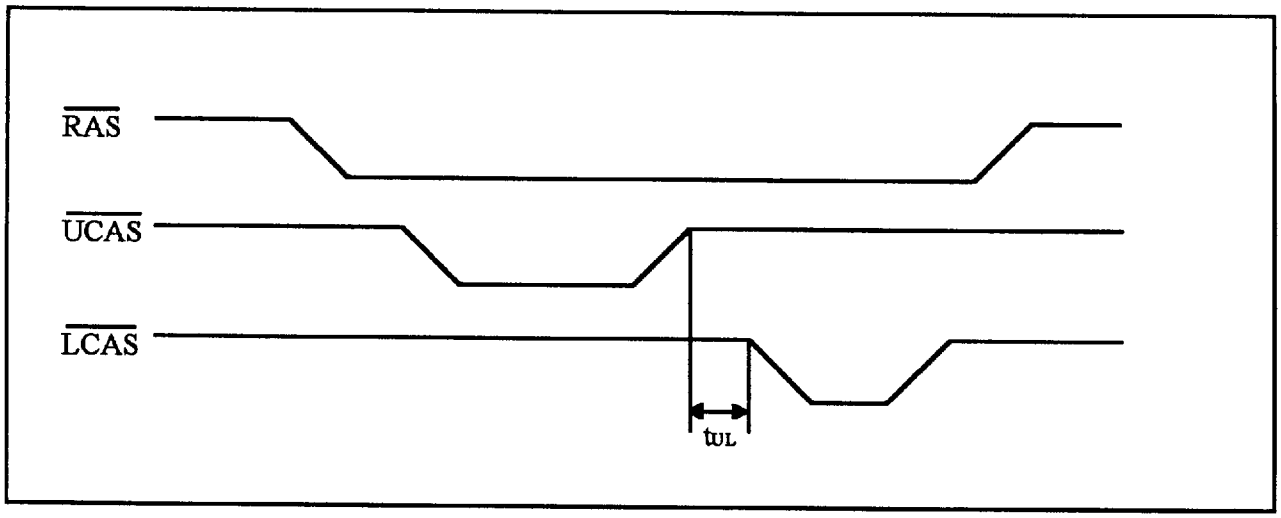
Notes concerning $\overline{2CAS}$ control

Please do not seperate the $\overline{UCAS}$/$\overline{LCAS}$ operation timing intentionally. However skew between $\overline{UCAS}$/$\overline{LCAS}$ are allowed under the following conditions.

1) Each of the $\overline{UCAS}$/$\overline{LCAS}$ should satisfy the timing specifications individually.
2) Different operation mode for upper/lower byte is not allowed; such as following.

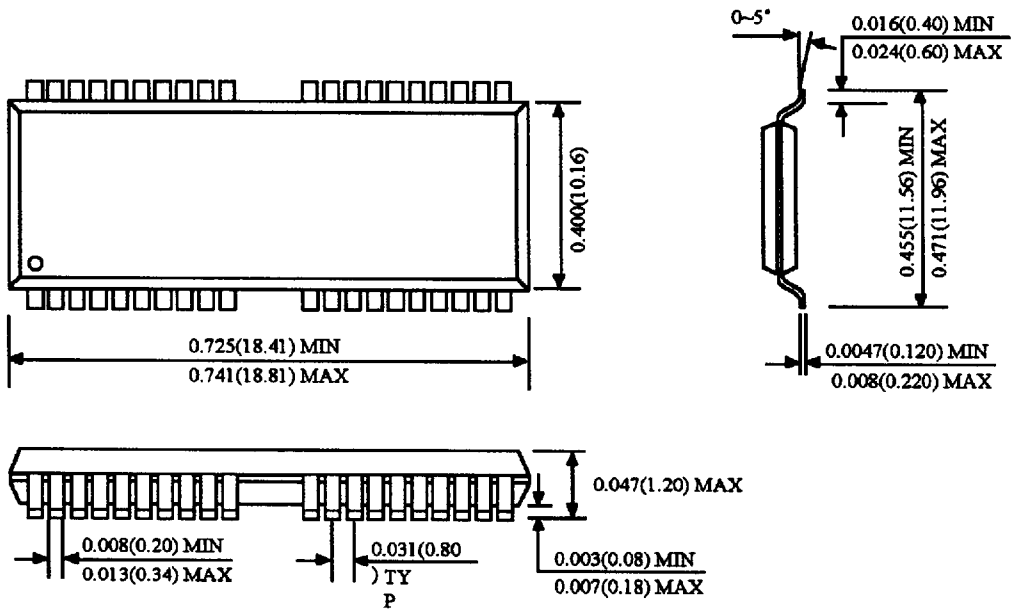


3) Closely seperated upper/lower byte control is not allowed. However when the conditon ($t_{CP} \leq t_{UL}$) is satisfied, fast page mode can be performed.



40(44) TSOP II

Unit: Inches (mm)



40 SOJ

Unit: Inches (mm)