

DALLAS SEMICONDUCTOR CORP 50E D 2614130 0004617 6 DAL

DALLAS
SEMICONDUCTOR

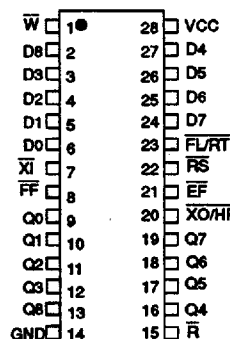
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DS2012
4096 x 9 FIFO Chip

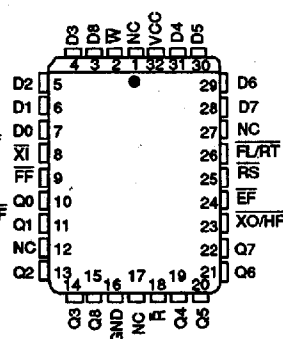
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FEATURES

- First-in, first-out memory-based architecture
- Flexible 4096 x 9 organization
- Low-power HCMOS technology
- Asynchronous and simultaneous read/write
- Bidirectional applications
- Fully expandable by word width or depth
- Empty and full warning flags
- Half-full flag capability in single-device mode
- Retransmit capability
- Available in 50 ns, 65 ns, 80 ns, and 120 ns access times
- Industrial temperature range -40°C to +85°C available, designated N, in 50 ns, 65 ns, 80 ns, and 120 ns access times

PIN ASSIGNMENT

28-Pin DIP (600 Mil)
See Mech. Drawing
Sect. 16, Pg. 4



32-Pin PLCC
See Mech. Drawing
Sect. 16, Pg. 11

PIN DESCRIPTION

W	- WRITE
R	- READ
RS	- RESET
FL/RT	- First Load/Retransmit
D ₀₋₈	- Data In
Q ₀₋₈	- Data Out
XI	- Expansion In
XO/HF	- Expansion Out/Half Full
FF	- Full Flag
EF	- Empty Flag
V _{CC}	- 5 Volts
GND	- Ground
NC	- No Connect

DESCRIPTION

The DS2012 FIFO Chip implements a first-in, first-out algorithm featuring asynchronous read/write operations, full, empty, and half full flags, and unlimited expansion capability in both word size and depth. The DS2012 is functionally and electrically equivalent to the DS2009

512 x 9 FIFO Chip, with the exceptions listed in the notes for DC Electrical Characteristics of the DS2009 data sheet. Refer to the DS2009 data sheet for detailed device description.