SONY

CXD2018AQ

Vertical Deflection Processing for TV

Description

The CXD2018AQ is a vertical deflection processing IC compatible with multi-standard TV systems.

Features

- I²C bus compatible
- Excellent synchronized stability performance and high precision deflection compensation are possible through software control.
- Non-interlace, double-speed deflection, wide-aspect processing and HDTV

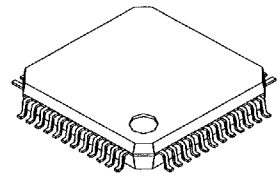
Applications

CRT

Structure

Silicon gate CMOS IC

48 pin QFP (Plastic)



Absolute Maximum Ratings (Ta=25 °C)

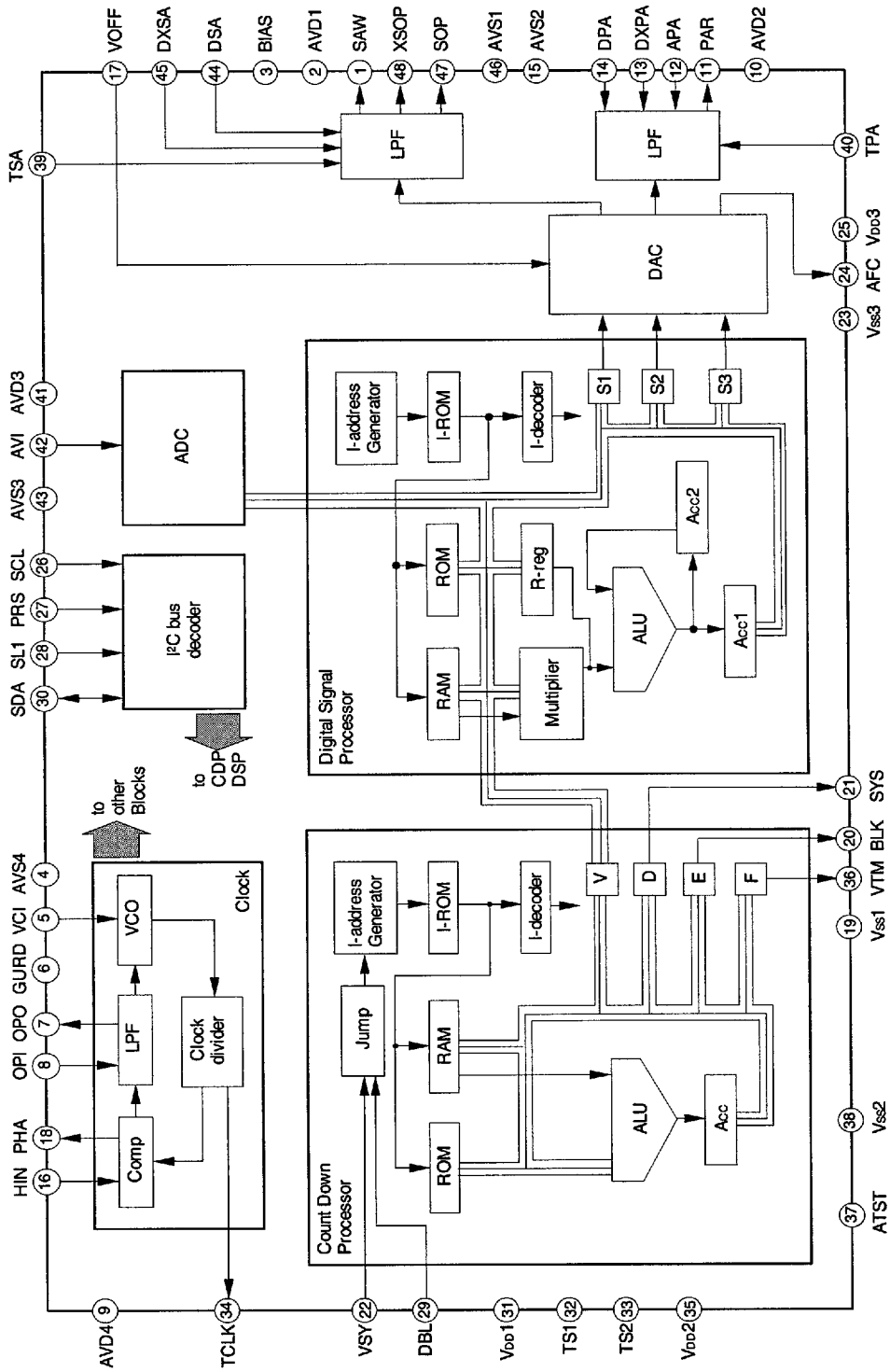
• Supply voltage	V_{DD}	V_{SS}–0.5 to +7.0	V
• Input voltage	V_I	V_{SS}–0.5 to V_{DD} +0.5	V
• Output voltage	V_O	V_{SS}–0.5 to V_{DD} +0.5	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–55 to +150	°C

Recommended Operating Conditions

• Supply voltage	Vcc	4.5 to 5.5	V
• Operating temperature	Topr	–20 to +75	°C

E96801-TE

Block Diagram



Pin Description

Pin No.	Symbol	I/O	Description
1	SAW	O	Sawtooth wave output
2	AVD1	—	Power supply for sawtooth wave output circuit (+5 V)
3	BIAS	I	Operational amplifier bias
4	AVS4	—	GND for PLL
5	VCI	I	VCO for PLL
6	GURD	—	GND connection
7	OPO	O	PLL operational amplifier output
8	OPI	I	PLL operational amplifier input
9	AVD4	—	PLL power supply (+5 V)
10	AVD2	—	Power supply for parabolic wave output circuit (–5 V)
11	PAR	O	Parabolic wave output for horizontal deflection compensation
12	APA	I	Capacitor for parabolic wave output circuit
13	DXPA	I	Capacitor for parabolic wave output circuit
14	DPA	I	Capacitor for parabolic wave output circuit
15	AVS2	—	Parabolic wave output circuit GND
16	HIN	I	Horizontal sync signal input
17	VOFF	I	Sawtooth wave output mute (Low: output; High: mute)
18	PHA	O	PLL phase comparison output
19	$V_{SS}1$	—	GND
20	BLK	O	Vertical blanking pulse output
21	SYS	O	System discrimination output (High: system M (60 Hz); Low: system B/G, I, L)
22	VSY	I	Vertical sync signal input
23	$V_{SS}3$	—	AFC compensation signal output GND
24	AFC	O	AFC compensation signal output
25	$V_{DD}3$	—	AFC compensation signal output power supply (+5 V)
26	SCL	I*	I^2C bus interface clock input
27	PRS	I	I^2C bus decoder power on reset
28	SL1	I	I^2C bus decoder slave address switching (Low: 86 (H); High: 8E (H))
29	DBL	I	Double scan enable (Low: forced normal scan; High: normal/double scan selected by I^2C bus)
30	SDA	I/O*	I^2C bus interface data I/O
31	$V_{DD}1$	—	Power supply (+5 V)
32	TS1	I	Test; normally fixed to "High"
33	TS2	I	Test; normally fixed to "High"
34	TCLK	O	Test; normally open
35	$V_{DD}2$	—	Power supply (+5 V)
36	VTM	O	Vertical sync timing pulse output
37	ATST	I	Test; normally open (Or GND connection)
38	$V_{SS}2$	—	GND
39	TSA	O	Test; normally open
40	TPA	O	Test; normally open

*The protective diode on the V_{DD} side for SCL and SDA pins has been eliminated.

Pin No.	Symbol	I/O	Description
41	AVD3	—	AD converter power supply
42	AVI	I	AD converter input
43	AVS3	—	AD converter GND
44	DSA	I	Capacitor for vertical deflection sawtooth wave output circuit
45	DXSA	I	Capacitor for vertical deflection sawtooth wave output circuit
46	AVS1	—	GND for vertical deflection sawtooth wave output circuit
47	SOP	O	External operational amplifier V + input for vertical deflection sawtooth wave output circuit
48	XSOP	O	External operational amplifier V – input for vertical deflection sawtooth wave output circuit

Electrical Characteristics

DC Characteristics V_{DD}=5 V±10 %, V_{SS}=0 V, Topr=–20 to +75 °C

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Input voltage 1	High level	V_{IH}		0.7 V_{DD}			V	
	Low level	V_{IL}				0.3 V_{DD}	V	
Input voltage 2		Vt+		0.8 V_{DD}			V	*1
		Vt–				0.2 V_{DD}	V	*1
	Hysteresis	Vt+–Vt–		0.7	0.9		V	*1
Output voltage 1		V_{OH}	I_{OH}=–2 mA	V_{DD}–0.8			V	
		V_{OL}	I_{OL}=4 mA			0.4	V	
Output voltage 2		V_{OH}	I_{OH}=–4 mA	V_{DD}–0.8			V	*2
		V_{OL}	I_{OL}=4 mA			0.4	V	*2
Input leak current		I_{LI}	Bi-directional pin input state	–40		40	µA	*3
Output leak current		I_{LZ}	High-impedance state	–40		40	µA	*4

*1. HIN, VSY pins, *2. PHA pin, *3. SDA pin, *4. PHA, SDA pins

I/O Pin Capacitance V_{DD}=V_I=0 V, f=1 MHz

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input pin	C_{IN}				9	pF
Output pin	C_{OUT}				11	pF
I/O pin	$C_{I/O}$				11	pF

Description of Function

1. Description

The CXD2018AQ is a vertical deflection processing IC compatible with multi-standard TV systems. This device basically consists of two different functional sections: countdown processor (CDP) and digital signal processor (DSP), which are respectively controlled through software. The CDP, by performing complex processing under the control of software, yields excellent synchronized stability performance to signals that contain a great deal of noise or that are missing a synchronizing component. Synchronization tracking performance during CH/VIDEO switching, system switching, and special playback operations for VCR is also outstanding in comparison with earlier systems. In addition, by performing high-level operation processing for various parameters set via the I²C bus system, the DSP permits high precision deflection compensation, making it possible to display images on large screens with little distortion. Furthermore, this IC is compatible with non-interlace, double-speed deflection, wide-aspect processing and HDTV.

2. I²C Bus System

2.1. I²C Bus Register Map

SLAVE ADDRESS 86H, 8EH: RECEIVER MODE
87H, 8FH: TRANSMITTER MODE

SUB ADDRESS	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
00 (H)	0	0	V-SIZE					
01 (H)	0	0	V-SHIFT					
02 (H)	S-CORRECTION				V-LINEARITY			
03 (H)	0	0	H-SIZE					
04 (H)	1	PIN-AMP						0
05 (H)	0	0	0	TILT				
06 (H)	UPPER-CORNER-PIN				LOWER-CORNER-PIN			
07 (H)	V-BOW				V-ANGLE			
08 (H)	1	HV-COMP-V			1	HV-COMP-H		
09 (H)	*	†1	†2	*	†3	†4	†5	†6
0A (H)	0	H-SHIFT						0

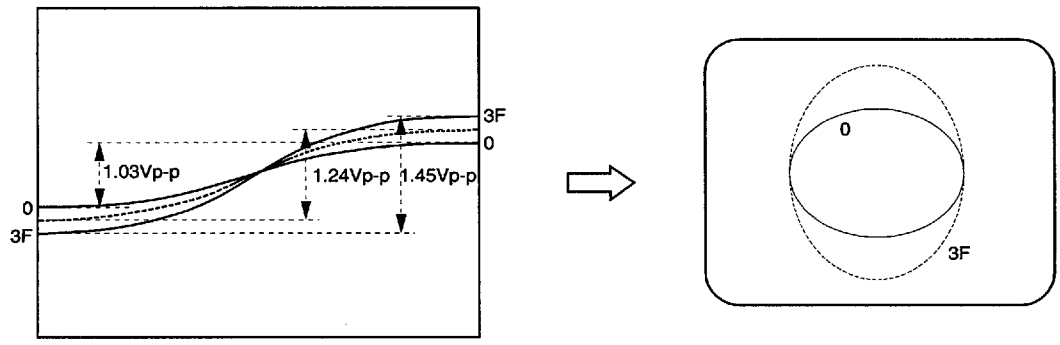
†1 Wide Aspect Ratio Frame Position (0: center; 1 : upper)
†2 60 Hz Fixed Mode for HDTV (0: off; 1 : on)
†3 System in Double Scan Mode (0: 100 Hz; 1 : 120 Hz)
†4 Aspect Ratio (0: 3:4; 1 : 9:16)
†5 Vertical Scan Speed (0: 50/60 Hz; 1: 100/120 Hz)
†6 Scan Type (Interlace/Non Interlace) (0: normal; 1 : reverse)
* don't care

2.2. Description of Operation for Each Register

2.2.1. V-SIZE

This register is used to adjust the size of the image in the vertical direction by changing the amplitude of the sawtooth wave used for vertical deflection. Because this register uses 6 bits, the size can be adjusted over a range of 64 steps. The range of adjustment is:

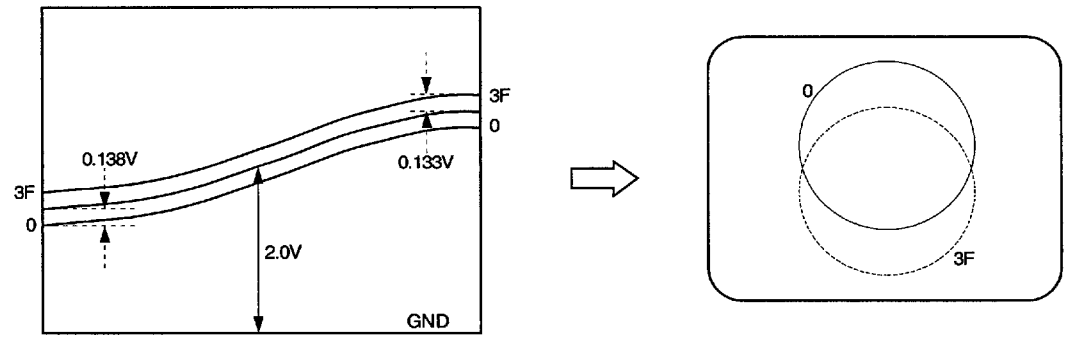
Maximum: 1.45 Vp-p (data = 3 F)
Typical: 1.24 Vp-p (data = 20)
Minimum: 1.03 Vp-p (data = 0)



2.2.2. V-SHIFT

This register is used to adjust the position of the image in the vertical direction by changing the DC component of the sawtooth wave used for vertical deflection. Because this register uses 6 bits, the position can be adjusted over a range of 64 steps. Using a reference value of 2.0 V, the range of adjustment is:

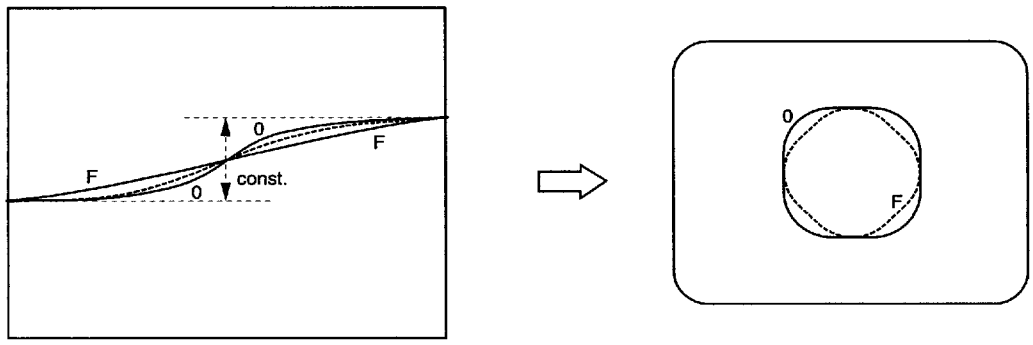
Maximum: +0.133 V (data = 3 F)
Typical: 0 V (data = 20)
Minimum: –0.138 V (data = 0)



2.2.3. S-CORRECTION

This register is used to compensate for the linearity for the screen in the vertical direction by changing the S compensation of the sawtooth wave used for vertical deflection. Because this register uses 4 bits, the linearity can be adjusted over a range of 16 steps. Note that, in this case, compensation is being applied so that the V-SIZE is roughly constant while on an actual screen the image changes by approximately 0.4-exposure. The adjustment method is:

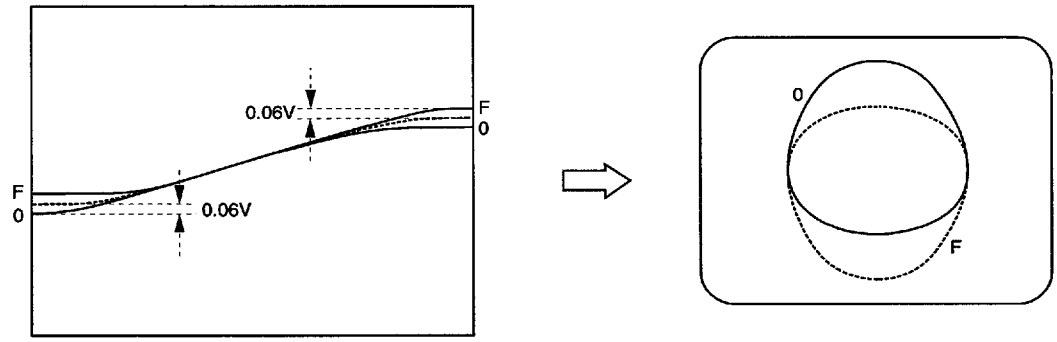
Maximum:	Strong S compensation	(data = 0)
Typical:	Moderate S compensation	(data = 8)
Minimum:	Weak S compensation	(data = F)



2.2.4 V-LINEARITY

This register is used to compensate for the linearity for the top and bottom edges of the screen by leaving the center portion of the sawtooth wave used for vertical deflection unchanged while applying compensation in the same direction at both ends. Because this register uses 4 bits, the linearity can be adjusted over a range of 16 steps. The range of adjustment is:

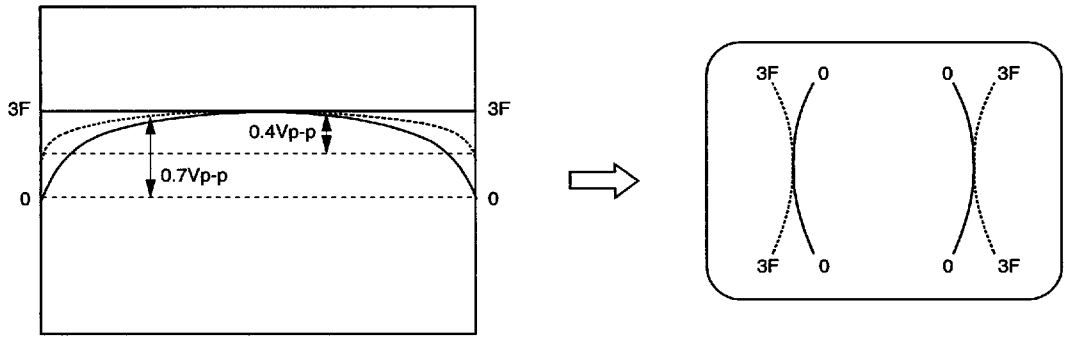
Maximum:	+0.06 V	(data = 0)
Typical:	0 V	(data = 8)
Minimum:	–0.06 V	(data = F)



2.2.5. PIN-AMP

This register is used to compensate for the pin distortion by changing the amplitude of the parabolic wave used for horizontal deflection compensation. Because this register uses 6 bits, the pin distortion can be adjusted over a range of 64 steps. The range of adjustment is:

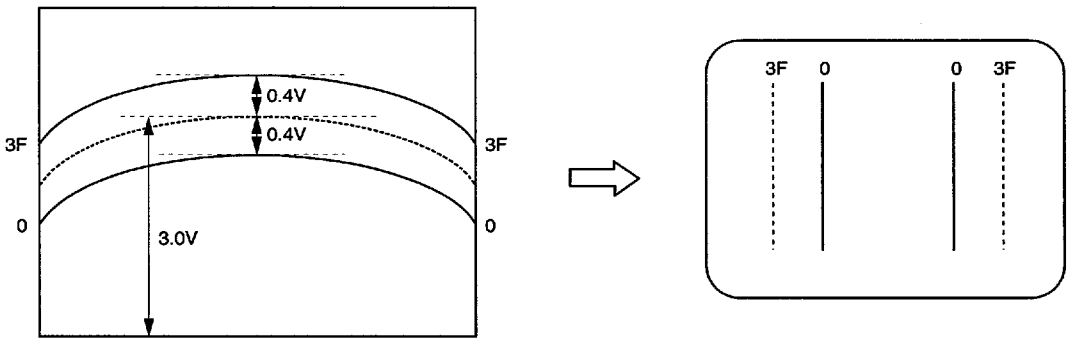
Maximum:	0.7 Vp-p	(data = 0)
Typical:	0.4 Vp-p	(data = 20)
Minimum:	0V p-p	(data = 3 F)



2.2.6. H-SIZE

This register is used to adjust the size of image in the horizontal direction by changing the DC component of the parabolic wave used for horizontal deflection compensation. Because this register uses 6 bits, the size can be adjusted over a range of 64 steps. Using a reference value of 2.5 V, the range of adjustment is:

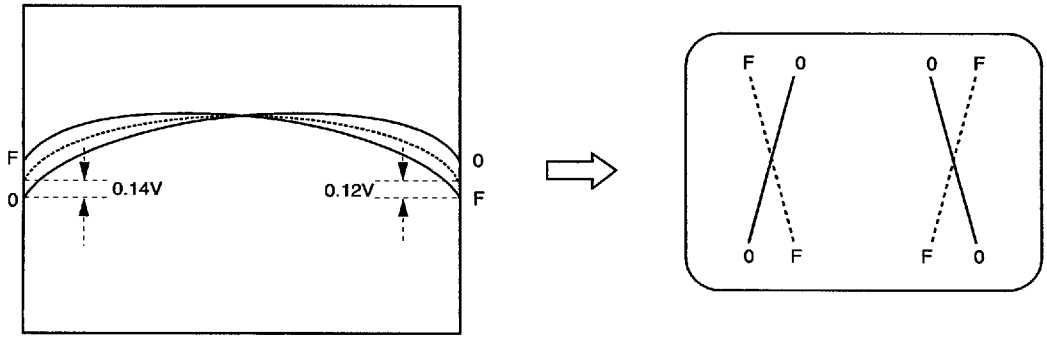
Maximum:	+0.4 V	(data = 3 F)
Typical:	0 V	(data = 20)
Minimum:	–0.4 V	(data = 0)



2.2.7. TILT

This register is used to compensate for the trapezoidal distortion by changing the slope of the parabolic wave used for horizontal deflection compensation. Because this register uses 4 bits, the trapezoidal distortion can be adjusted over a range of 16 steps. The range of adjustment is:

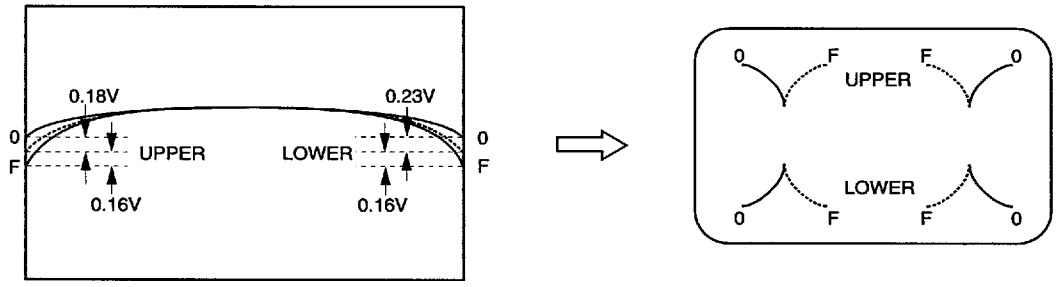
Clockwise:	+0.24 V	(data = F)
Standard:	0 V	(data = 8)
Counterclockwise:	–0.28 V	(data = 0)



2.2.8. CORNER-PIN

This register is used to independently compensate for the linearity of the upper and lower corners of the image by partially compensating for the parabolic wave used for horizontal deflection compensation. Because this register uses 4 bits, the linearity can be adjusted over a range of 16 steps. The range of adjustment is:

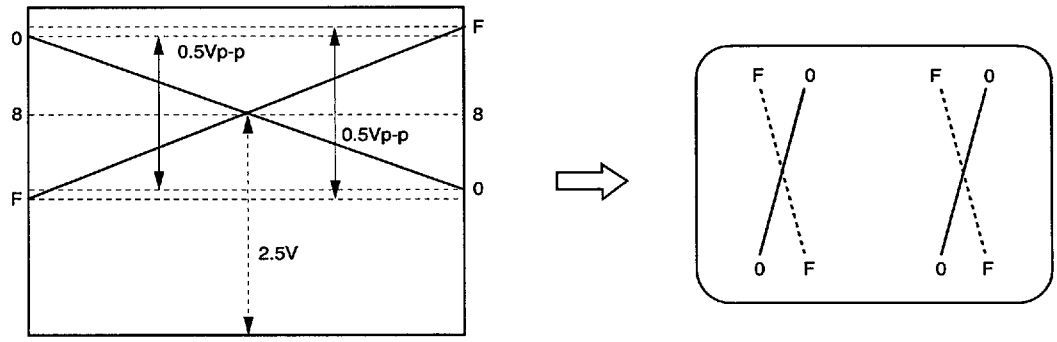
(UPPER)			(LOWER)	
Maximum:	+0.18 V	(data = 0)	Maximum:	+0.23 V
Typical:	0 V	(data = 8)	Typical:	0 V
Minimum:	–0.16 V	(data = F)	Minimum:	–0.16 V



2.2.9. V-ANGLE

This register is used to compensate for the parallelogram distortion by changing the slope of the AFC compensation wave. Because this register uses 4 bits, the parallelogram distortion can be adjusted over a range of 16 steps. The range of adjustment is:

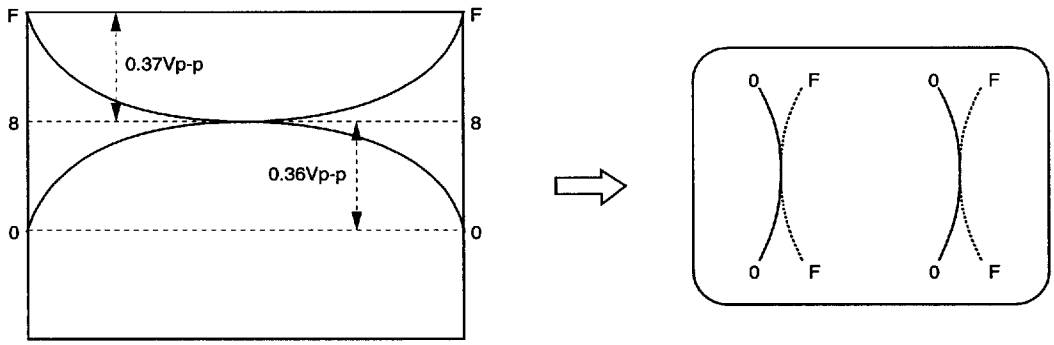
Up right:	0.5 Vp-p	(data = F)
Standard:	0 Vp-p	(data = 8)
Down right:	0.5 Vp-p	(data = 0)



2.2.10. V-BOW

This register is used to compensate for the bowing in the vertical direction by changing the amplitude of the AFC compensation wave. Because this register uses 4 bits, the bowing in the vertical direction can be adjusted over a range of 16 steps. The range of adjustment is:

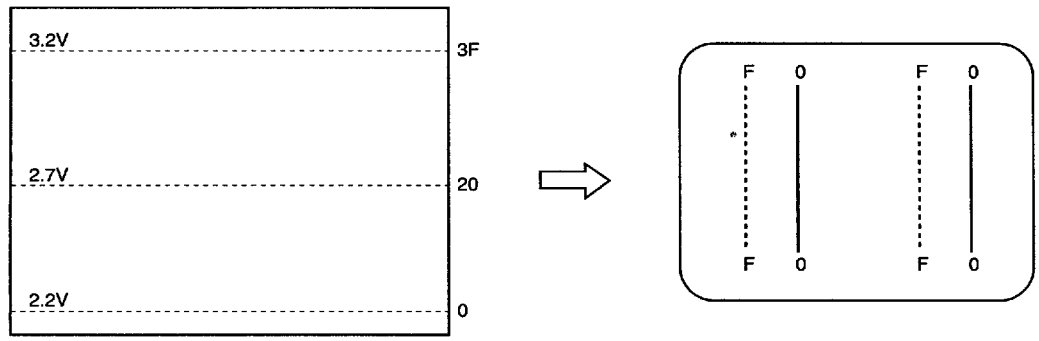
Positive direction:	0.37 Vp-p	(data = F)
Standard:	0 Vp-p	(data = 8)
Negative direction:	0.36 Vp-p	(data = 0)



2.2.11. H-SHIFT

The H-SHIFT function is used to adjust the position of the image in the horizontal direction by changing the DC component of the AFC compensation wave. Because this bus register uses 6 bits, the position can be adjusted over a range of 64 steps. The range of adjustment is:

Maximum:	3.2 V	(data = 0)
Typical:	2.7 V	(data = 20)
Minimum:	2.2 V	(data = 3 F)



Note 1:

When the variable range for the angle compensation has been set to ±1 °, the allowable variable range for H-SHIFT is ±1 µs. Therefore, when using this device in combination with the CXA1587S, make the adjustment through the CXA1587S, not using the H-SHIFT function.

Note 2:

When H-SHIFT is used together with V-ANGLE or V-BOW, restrictions on the dynamic range of the DSP and the DA converter make it necessary to use each parameter within the half of its variable range. Therefore, the usable ranges for each parameter are as follows:

V-ANGLE:	4 H to BH	(8 steps)
V-BOW:	4 H to BH	(8 steps)
H-SHIFT:	10 H to 2 FH	(32 steps)

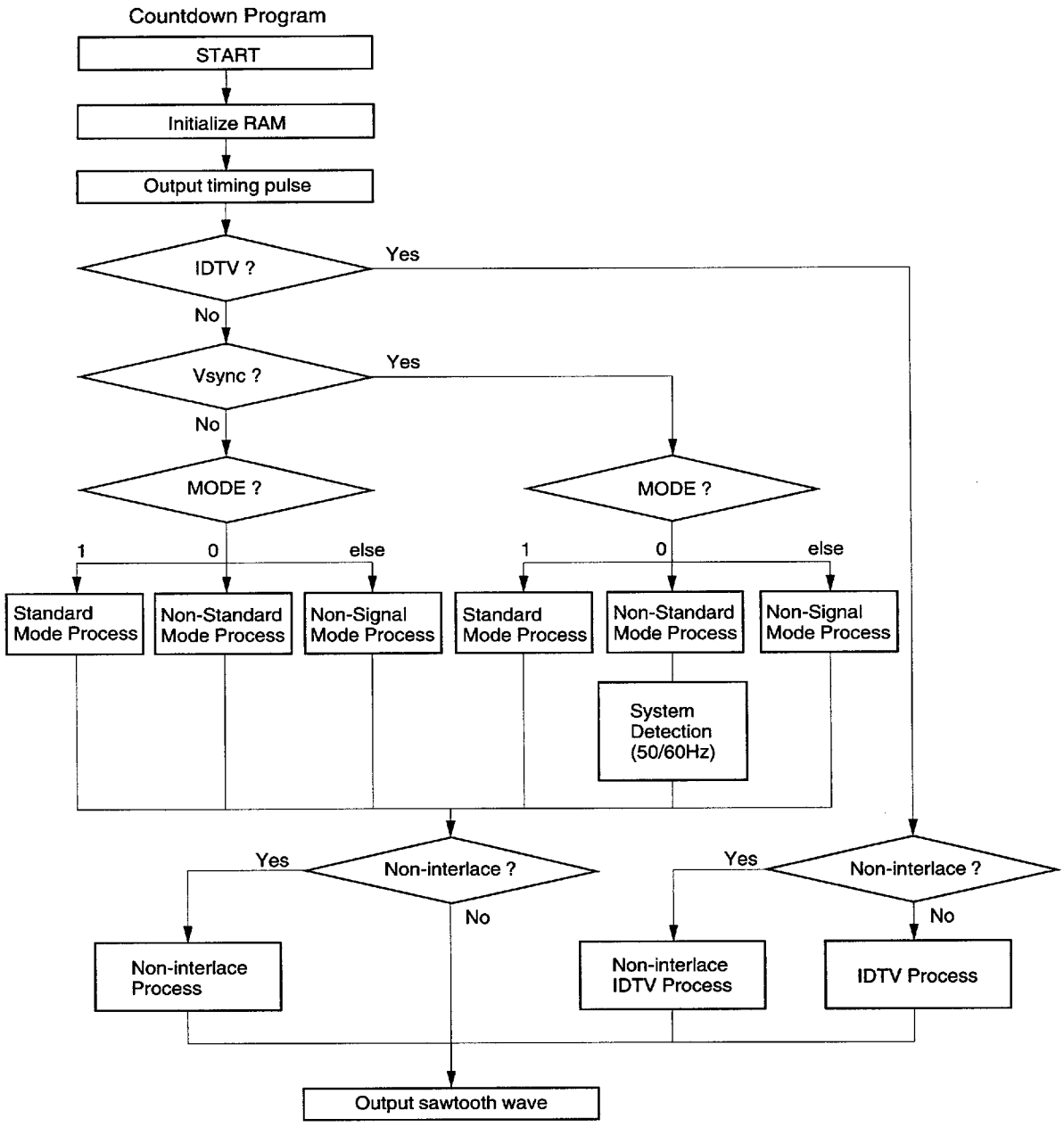
This restriction is controlled by software. In addition, it is also necessary to double the adjustment ranges for H-SHIFT, V-ANGLE, and V-BOW.

3. Internal Block Functions

3.1. Countdown Processor (CDP)

The countdown processor consists of ALU, RAM and ROM, and is operated by internal program stored in ROM. The CDP outputs count value, 50/60 Hz discrimination result, and timing pulse.

The major processing performed by the CDP is described below.



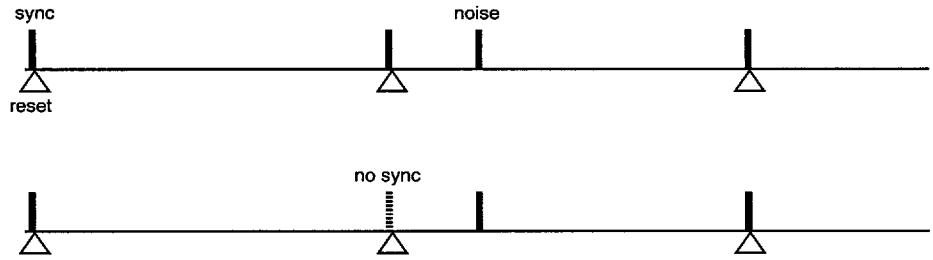
3.1.1. Normal Scan Processing

When normal scan processing is to be executed, the mode is classified into three types (standard mode, non-standard mode, and no signal mode) according to the vertical synchronizing pulse cycle of the input signal, and the processing that seems to be optimal for each signal is performed. The operation of each mode is described below.

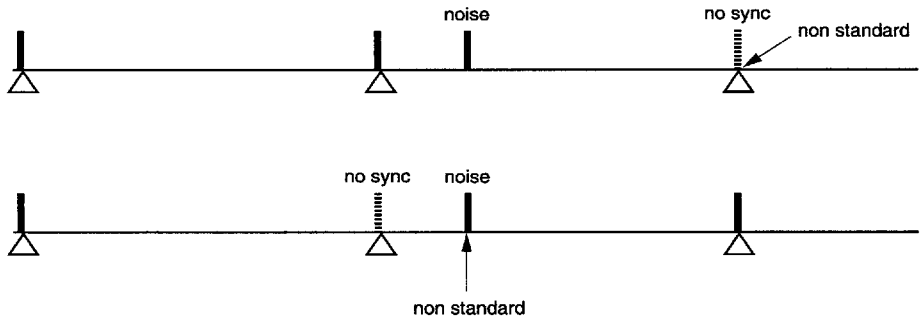
(1) Standard mode

When 1 V = 262.5 H/312.5 H (const.) signal is identified as the standard signal, processing is performed in this mode. The main feature of this mode is that it can compensate for V-sync loss, noise, etc., without sacrificing synchronizing tracking during channel switching, VCR/RGB switching, or VCR special playback operations. This mode processing is as follows.

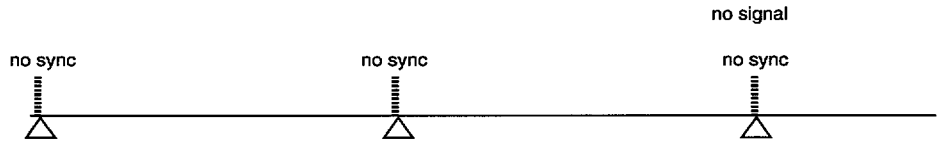
- When the signal is stable and in standard mode, V-sync separation output in other than the regular position is regarded as noise and ignored. When that is missing, it is automatically reset in the regular position.



- When the V-sync is missing after noise, or when noise appears after the V-sync is missing, it is assumed that channel switching, VCR/RGB switching, or a VCR special playback operation is performed, and the mode switches to non-standard mode.



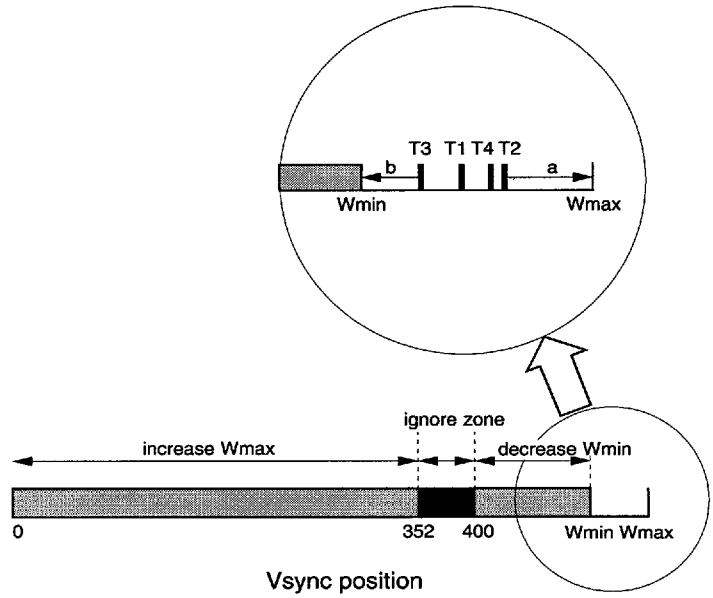
- When V-sync is missing for three or more V intervals, the mode switches to no signal mode.



(2) Non-standard mode

When the V-sync signal is present and the relationships in standard mode have been fulfilled, the signal is identified as a non-standard signal and processing is performed in this mode. The feature of this mode is to use a "variable window" in order to perform stable synchronizing tracking to noise, missing V-sync signals or frequency fluctuation.

The "variable window" is created by adding up the margins (a and b) calculated based on the state of V-sync fluctuation using both the maximum and minimum values for the past four V-sync signals (T1, T2, T3, and T4). Processing is performed as follows, according to the position of V-sync separation output.



Vsync position

- When V-sync is detected in the range from 0 H to 352 H, the V cycle is assumed to become longer and the upper edge of the window (Vmax.) is lifted.
- When V-sync is detected in the range from 353 H to 400 H, it is assumed to be noise and ignored.
- When V-sync is detected in the range from 401 H to Wmin. (the bottom edge of the window), the V cycle is assumed to have become shorter and Wmin is lowered.
- When V-sync is detected within the window, it is assumed to be the regular sync signal and a reset is applied.
- When V-sync is not detected, even in excess of Wmax., forced reset is applied immediately.

When V-sync is missing for three or more V intervals, the mode switches to no signal mode; when V-sync is detected in the standard position for eight or more V intervals, the mode switches to standard mode.

(3) No signal mode

When V-sync is not detected, it is identified as no signal and processing is performed in this mode. As long as no signal state continues in this mode, a reset is continuously applied according to the cycle (50 Hz/60 Hz) determined by the I²C bus. As soon as V-sync is detected, the mode switches to non-standard mode.

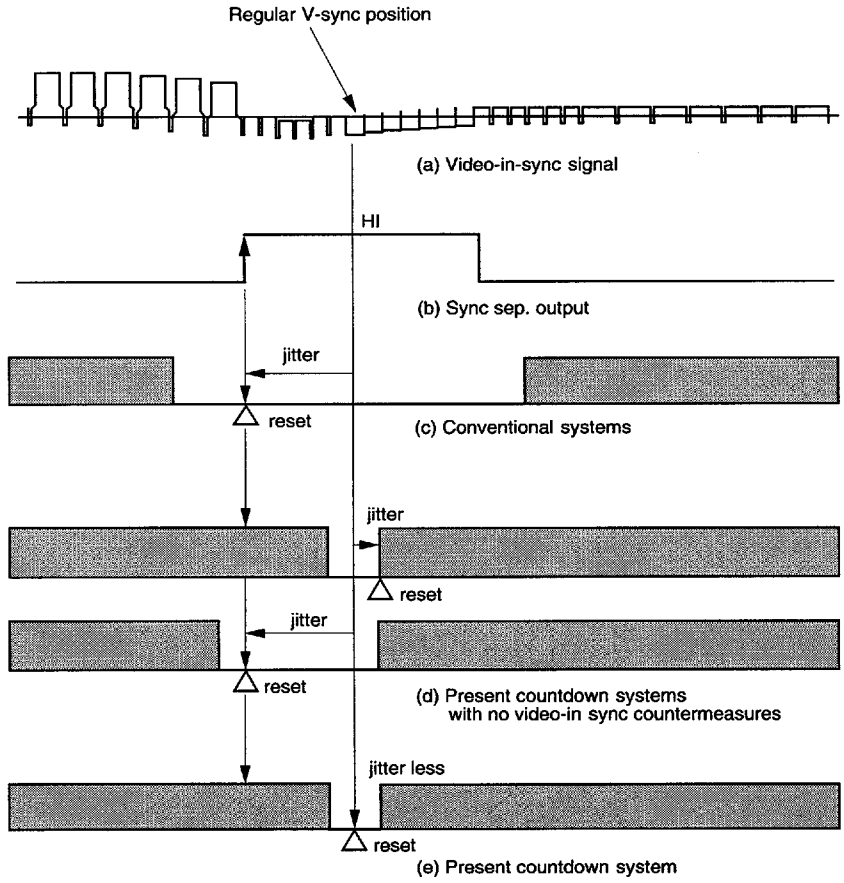
3.1.2. Video-In-Sync Countermeasures

"Video-in-sync" is a phenomenon where either an equivalent pulse is detected in a position prior to the regular V-sync position or else V-sync is detected at a position in a video interval. This phenomenon usually results from a rapid change in APL or a trouble of a relay device. (See Figures (a) and (b) below.)

In conventional systems, the window was wide as shown in Figure (c) so that the deviation in the position of the rising edge of the sync separation output in the video-in-sync state appeared as jitter. In this countdown system as well, when no countermeasures are taken, jitter will also occur. (See Figure (d) below.)

In the programmable countdown system, however, by taking advantage of the fact that there is no window in the standard state and that the normal window is very small in the non-standard state (±1 H), fulfillment of the following conditions is deemed to indicate a video-in-sync state, making it possible to keep jitter to a minimum. (See Figure (e) below.)

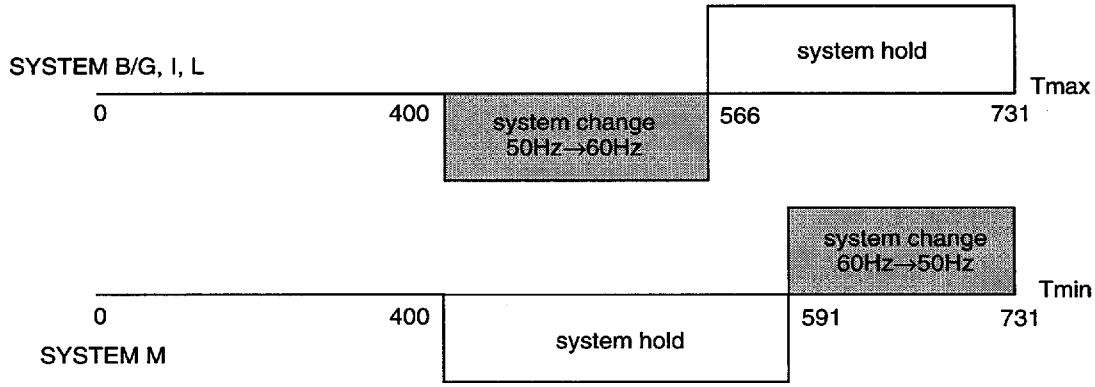
- Detection method
  When the count value X reaches the system's specified value (525/625), and the V-sync separation output is high with no rising edge.
- Processing method
  Reset is applied in the same way as when the sync signal was detected in the regular V-sync position.



3.1.3. Automatic System Discrimination Processing

The world's broadcasting systems can be broadly classified according to their vertical deflection frequency into two groups; system M (60 Hz) and systems B/G, I and L (50 Hz). The CXD2018AQ is designed to be compatible with all of these systems and needs to identify on its own to which group a system belongs. Countdown processing is performed by software in the CXD2018AQ, and quickly and accurately system identification can be realized by using the variable window used in the countdown processing. The method is described below.

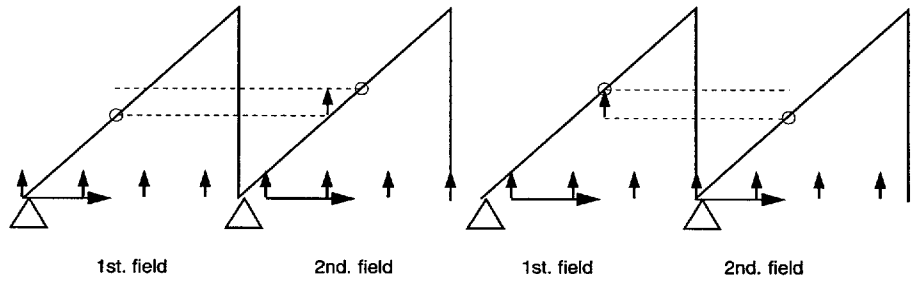
The system is switched only when the window is open in non-standard mode. The reason for this is that system switching is always required only after entering non-standard mode once. Non-standard mode is explained below.



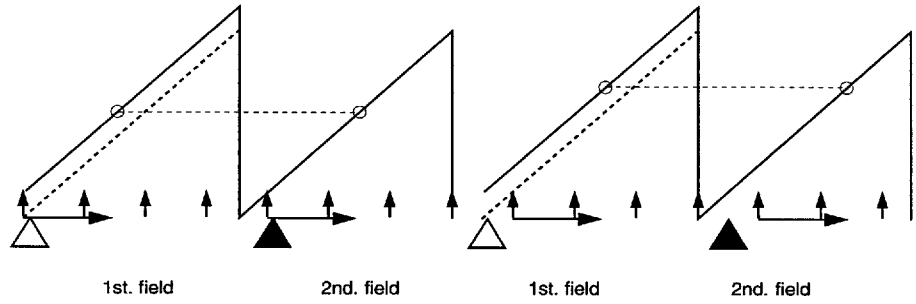
First, in the case of systems B/G, I, and L (50 Hz), the window is supposed to be open in the vicinity of LC = 625; the system is never switched when in this state. However, after switching to system M, the window is supposed to shift downwards to the vicinity of LC = 525. This characteristic is used in order to determine whether to switch from 50 Hz to 60 Hz by monitoring the maximum value (Tmax.) of the last four V cycles (T1 to T4); when Tmax. < 566, the system switches to system M. In the case of system M, the same basic concept is used, when the minimum value (Tmin.) of the last four V cycles (T1 to T4) is monitored and Wmin. > 591, the system switches to system B/G, I, and L. Using this method greatly reduces the likelihood of misoperation resulting from noise or frequency fluctuations, while allowing system switching with a short discrimination time (four V cycles after sync is pulled-in).

3.1.4. Non-Interlace Processing

In addition to normal interlace processing, the CXD2018AQ is also capable of non-interlace processing, making it suitable for use with teletext broadcasts. In the normal interlace method, the relationship between the vertical deflection sawtooth wave and the video signal is as shown in the figure below; the same information as in field 1 comes in field 2 in a position with a 0.5 H difference. In non-interlace processing, the information in fields 1 and 2 must be in the same position. In the CXD2018AQ, non-interlace processing is implemented by adding "+1" to the value in the first (second) field during the count value output, and then, in the second (first) field, delaying by 0.5 H the V timing pulse output that is used to output the text signal.



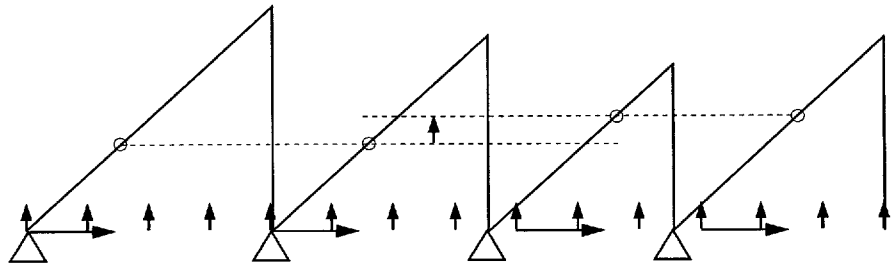
Normal interlace processing



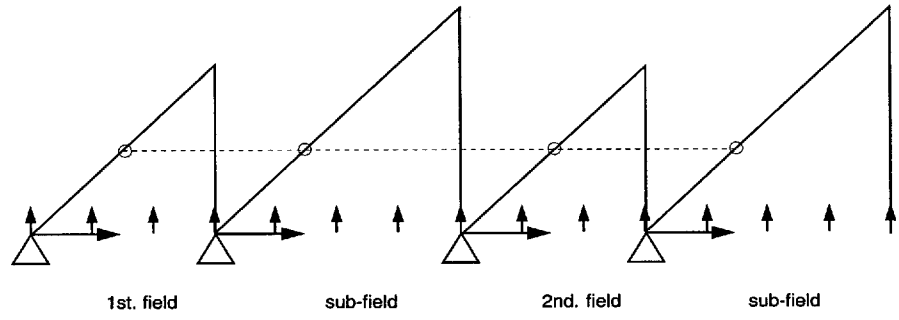
Non-interlace processing

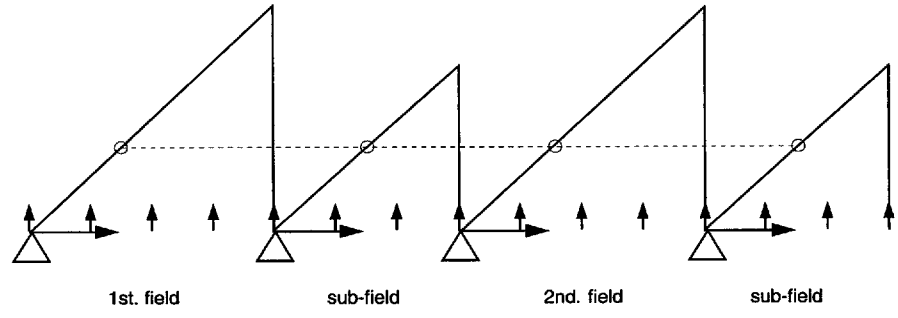
3.1.5. Double-Scan Processing

When the CXD2018AQ is used with a flicker-free TV IC, double-scan processing is also possible. In the case of interlace processing, the 2 V output of the flicker-free TV ICs are almost perfect trigger type. (Before being pulled-in, up to 50 H is masked in order to protect the deflection portion; after being pulled-in, from 215 H to 365 H is the fixed window.)



In the case of non-interlace processing, the 2 V output is not actively synchronized, but synchronized non-interlace processing can be easily implemented by generating a vertical deflection sawtooth waves that fluctuates as follows: 1 V = 313 H, 312 H.

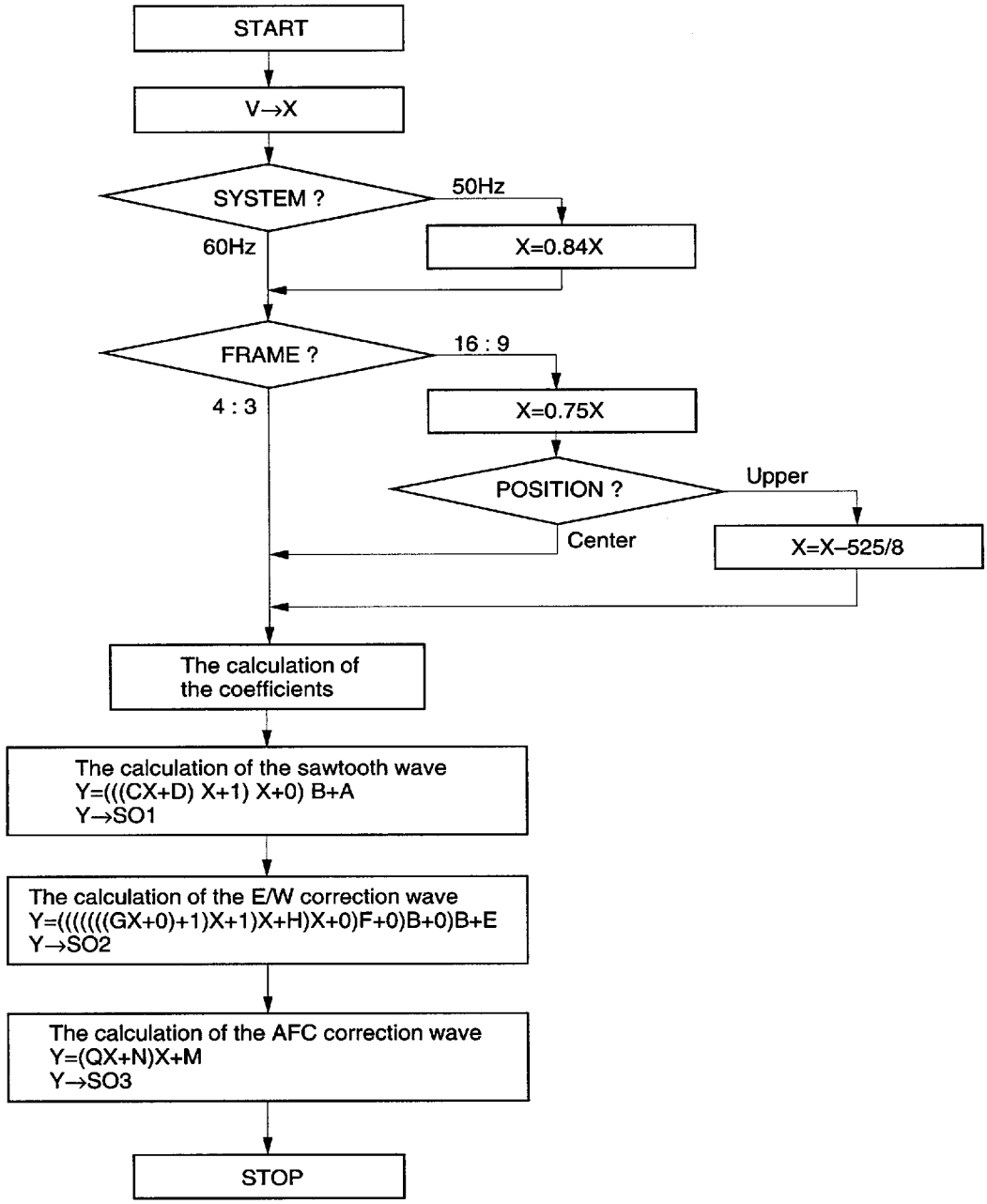




3.2. Digital Signal Processor (DSP)

The DSP consists of ALU, multiplier, RAM and ROM. Based on the count value information received from the countdown processor, an internal program generates the vertical deflection sawtooth wave, the horizontal deflection compensation parabolic wave, and the AFC compensation wave and outputs them through a Δ-Σ type 1-bit D/A converter. The processing performed there is described below.

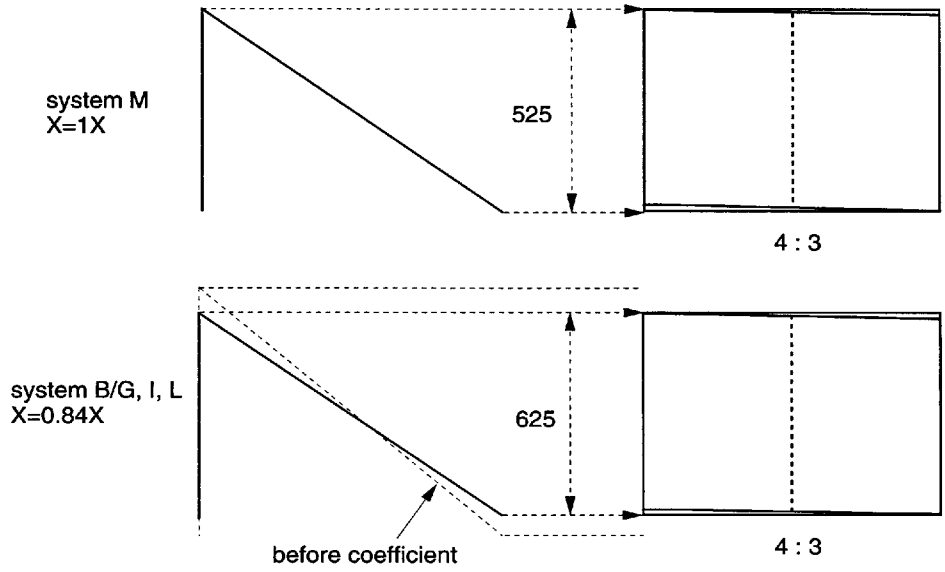
Deflection Compensation Processing Program



3.2.1. Count Value Optimization Processing

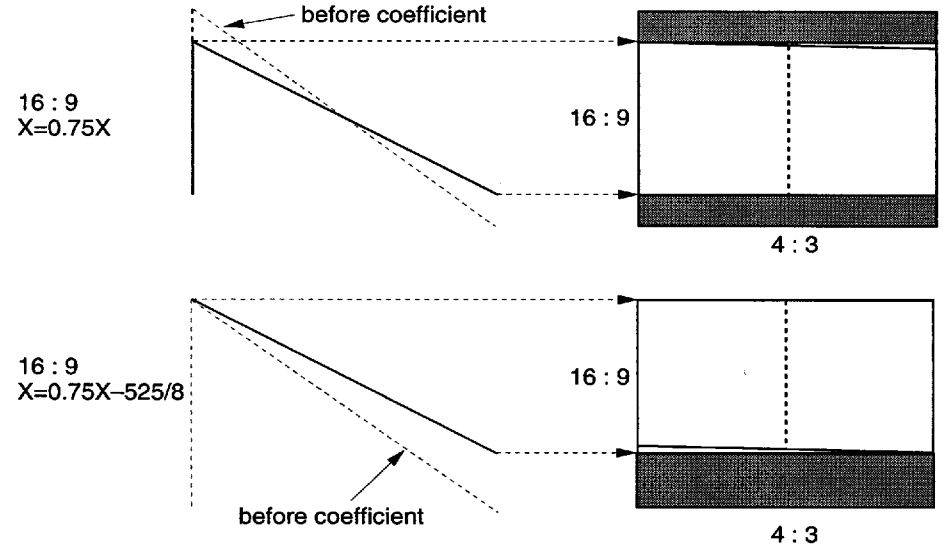
(1) 50/60 Hz optimization

As the amplitude of the output from the countdown processor for system M (60 Hz) differs from systems B/G, I, and L (50 Hz), process using the values as it is, requires to adjust all of the deflection compensation parameters for each system and is inconvenience. To avoid this, in the case of systems B/G, I, or L, processing is performed after the count value is multiplied by 0.84 (525/625) and converted to the same amplitude as that used in system M.



(2) 16:9 optimization

In order to provide immediate compatibility with the 16:9 wide-aspect ratio, this device is provided with a mode in which the count value to be input from the countdown processor is multiplied by 0.75. In addition, whether the frame position is to be centered in the 4:3 screen or located in the upper portion of the 4:3 screen can be selected through the I²C bus.



3.2.2. Deflection Compensation Processing

◆ Vertical deflection sawtooth wave output

The vertical deflection sawtooth wave Y2 is derived using the following formula after the count value optimization processing described earlier is performed on the input X from CDP:

$$Y2 = (CX^3 + DX^2 + X)\,B + A$$

where

A :	V-shift adjustment parameter	V-SHIFT
B :	$B = B1 - S \times P1$	
	B1 : V-size adjustment parameter	V-SIZE
	S : A/D converter output coefficient	
	P1 : V high-pressure compensation parameter	HV-COMP-V
C :	S compensation parameter	S-CORRECTION
D :	Linearity compensation parameter	V-LINEARITY

◆ Horizontal deflection parabolic wave output

The horizontal deflection parabolic wave Y1 is derived using the following formula after the count value optimization processing described earlier is performed on the input X from the CDP:

$$Y1 = (GX^4 + X^2 + HX)\,FB^2 + E$$

where

E :	$E = E1 - S \times P2$	
	E1 : H-size adjustment parameter	H-SIZE
	S : A/D converter output coefficient	
	P2 : H high-pressure compensation parameter	HV-COMP-H
F :	Pin distortion compensation parameter	PIN-AMP
G :	G = G1 or G2	
	G1 : Upper corner pin compensation parameter	UPPER-CORNER-PIN
	G2 : Lower corner pin compensation parameter	LOWER-CORNER-PIN
H :	Trapezoidal distortion compensation parameter	TILT

◆ AFC compensation wave output

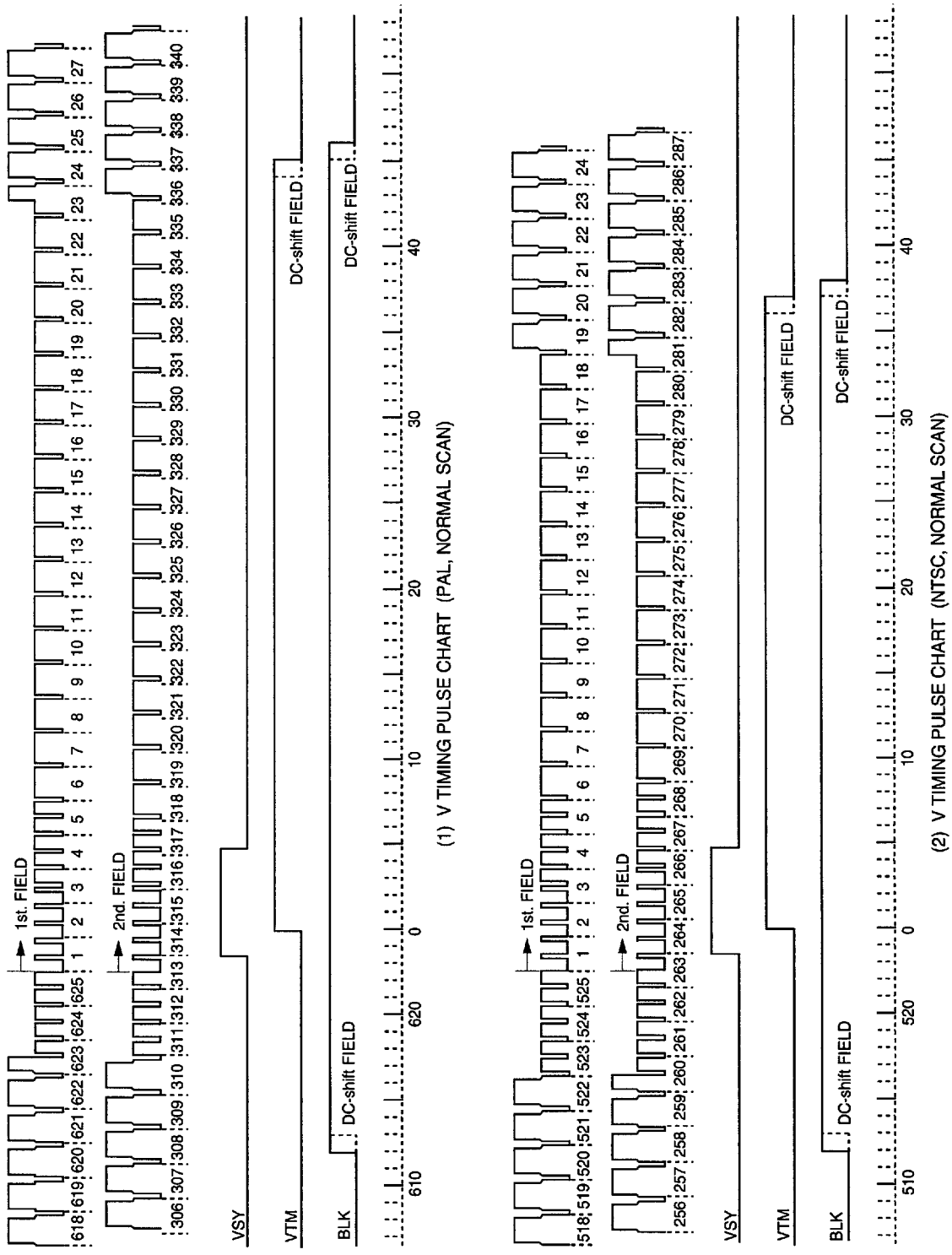
The AFC compensation wave Y3 is derived using the following formula after the count value optimization processing described earlier is performed on the input X from the CDP:

$$Y3 = QX^2 + NX + M$$

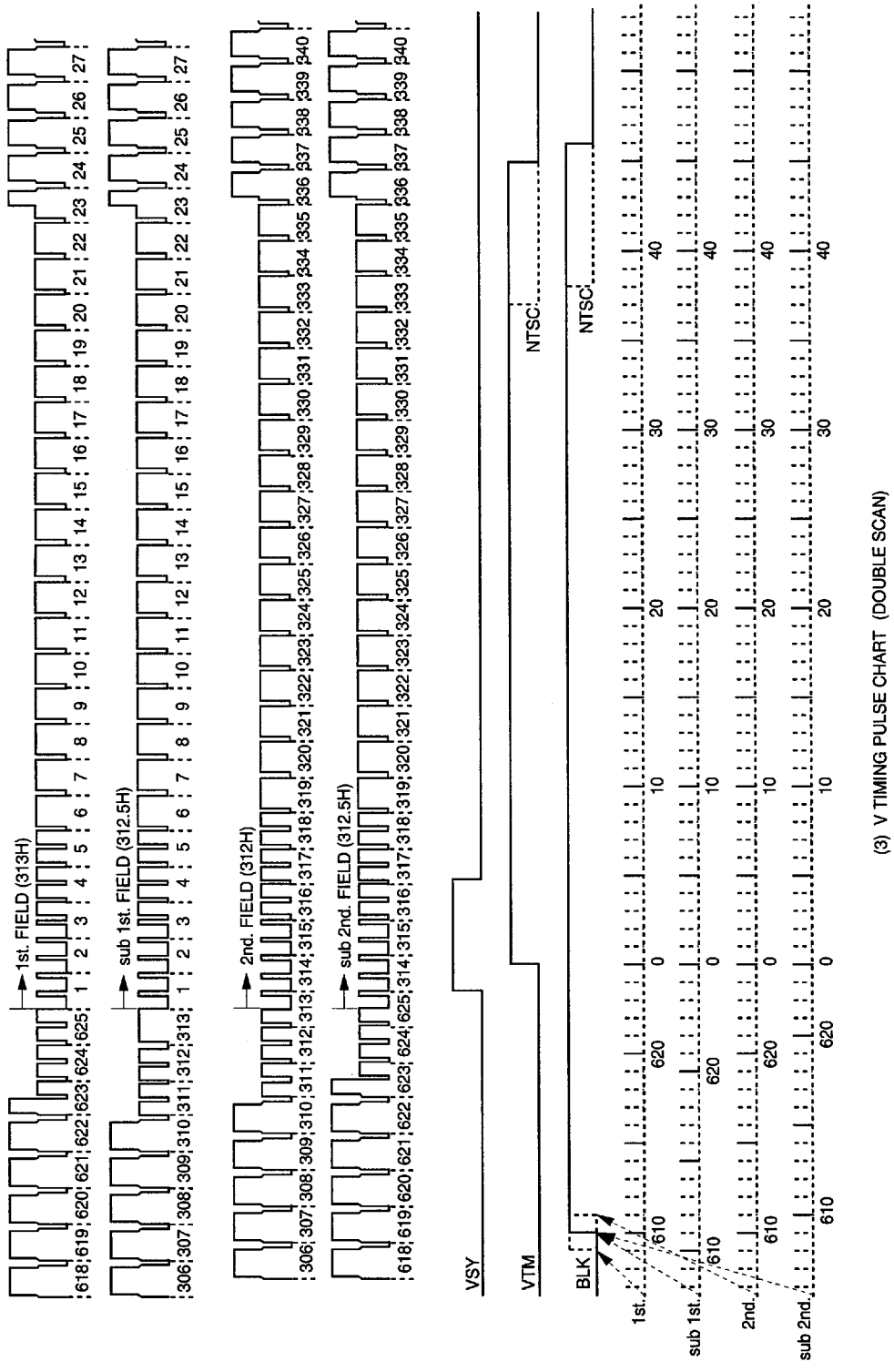
where

Q :	Vertical bowing compensation parameter	V-BOW
N :	Parallelogram distortion compensation parameter	V-ANGLE
M :	H-shift adjustment parameter	H-SHIFT

Timing Charts (1) and (2)



Timing Chart (3)



(3) V TIMING PULSE CHART (DOUBLE SCAN)

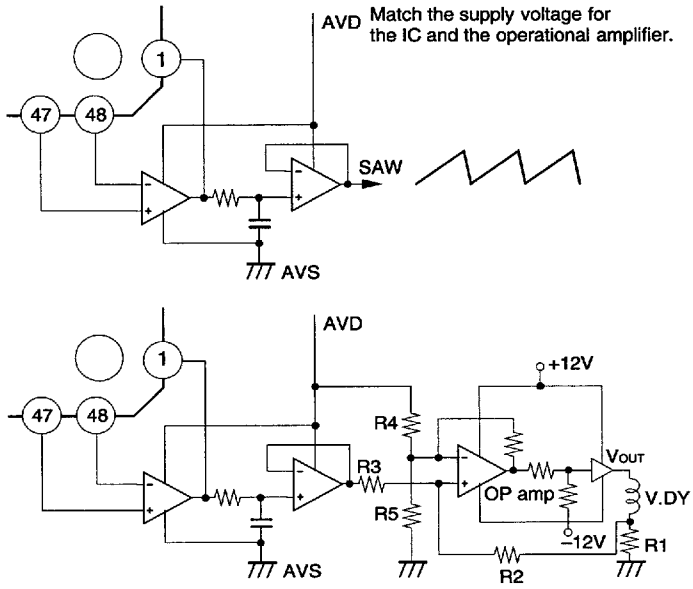
4. Notes on Operation

4.1. Sawtooth Wave Output Circuit

For sawtooth wave output as shown at right, the supply voltage characteristics for V-size and V-shift are shown below.

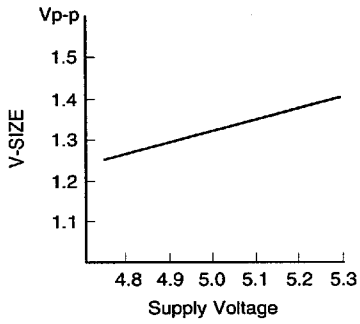
For the actual vertical deflection output circuit, by sharing the reference voltage of the operational amplifier with the IC supply voltage as shown at the lower right, the effect caused by V-shift supply voltage fluctuation can be canceled.

The supply voltage characteristics of PIN-AMP and H-SIZE are also shown below.

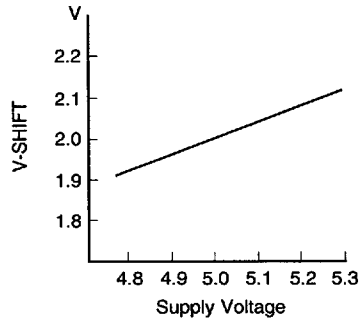


Note:

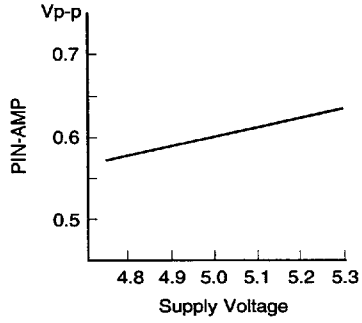
When the VOFF pin (Pin 17) is set to the MUTE state against the sawtooth wave, about 2 V DC voltage is output. Design the VOUT circuit with this electric potential as the center electric potential for V-shift.



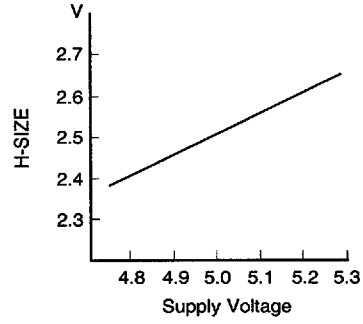
The dependence of Supply Voltage and V-SIZE.



The dependence of Supply Voltage and V-SHIFT.



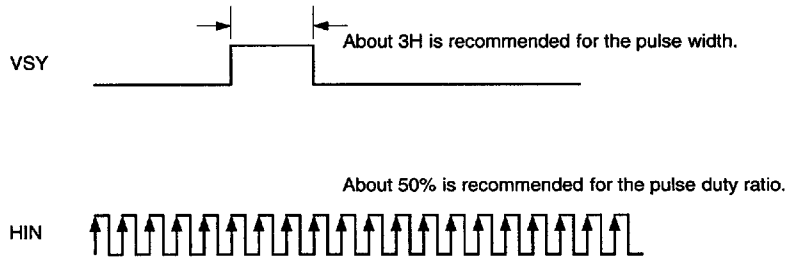
The dependence of Supply Voltage and PIN-AMP.



The dependence of Supply Voltage and H-SIZE.

4.2. Input Sync Signal

Input of vertical sync signal (Pin 22) and horizontal sync pulse (Pin 16)
(Both the vertical sync signal and the horizontal sync pulse use a Schmitt trigger-type input cell.)

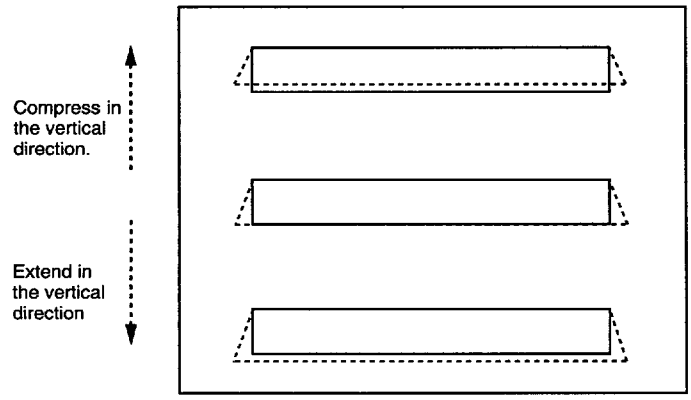


4.3. Double-Speed Mode

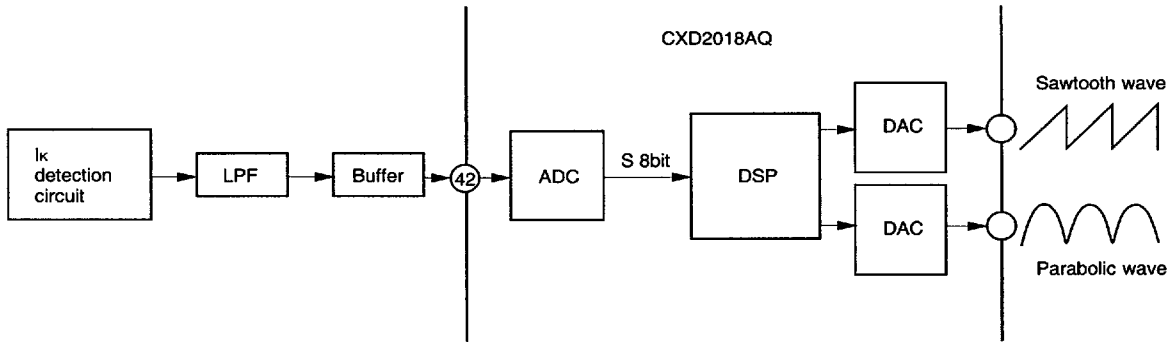
In double-speed mode, the vertical deflection sawtooth wave is used at the vertical output circuit directly connected to DC.
(The AC coupling causes problems with interlacing.)

4.4. High-Pressure Compensation Circuit

The CXD2018AQ permits both vertical and horizontal zooming and ripple compensation by inputting a cathode current or ABL current detection waveform. (Note: When using the ABL detection waveform, it is sufficiently integrated so that only zooming compensation is performed.)
"Ripple compensation" is described below.



The block diagram of the CXD2018AQ high-pressure compensation system is shown below.



Block Diagram of High-Pressure Compensation System

After detecting and integrating the cathode current, it is input to A/D converter in the IC. The dynamic range of this A/D converter is from 0 to 5 V, and provides a resolution of 8 bits and a sampling frequency of 2 fH (31.468 kHz) with no clamp.
Based on the detection data, the DSP performs the following compensation on sawtooth and parabolic waves. The first explanation is for vertical high-pressure compensation. The operations for the sawtooth wave and the vertical high-pressure compensation are shown below.

$V2 = (CX^3 + DX^2 + X)\,B + A$

$B : B = B1 - S \times P1$

B1 : V-size adjustment parameter
S : A/D converter output coefficient
P1 : Vertical high-pressure compensation parameter

For the vertical high-pressure compensation, the detection data S is multiplied by the coefficient P1 and the result is used to compensate the V-size coefficient B1. P1 is equivalent to the HV-COMP-V of upper three bits of subaddress 08 H, and is used with eight steps, from 0 to 7. Note that adjustment value 0 means that vertical high-pressure compensation is off.
The method for adjusting HV-COMP-V is as follows. First, the detection resistor is decided so that HV-COMP-V is in the range from 2 to 5. Then, the LPF time constant is determined so that the tracking of the zooming compensation and the ripple compensation will match. Finally, HV-COMP-V is set so that the V-size remains constant even if the picture is changed.
Next, horizontal high-pressure compensation. The operations for the parabolic wave and the horizontal high-pressure compensation are shown below.

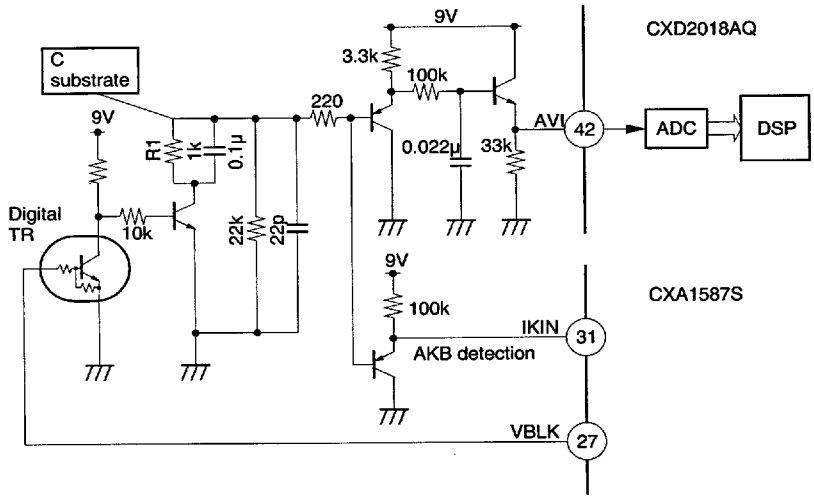
$$Y1 = (GX^4 + X^2 + HX)\,FB^2 + E$$

E : $E = E1 - S \times P2$

E1 : H-size adjustment parameter
S : A/D converter output coefficient
P2 : Horizontal high-pressure compensation parameter

For the horizontal high-pressure compensation, the detection data S is multiplied by the coefficient P2 and the result is used to compensate the H-size coefficient E1. E1 is equivalent to the HV-COMP-H of lower three bits of subaddress 08 H, and is used with eight steps, from 0 to 7. Adjustment value 0 means that horizontal high-pressure compensation is off.
Note that HV-COMP-H adjustment conforms with the HV-COMP-V adjustment.

(Reference) Example of cathode current detection circuit



Note: The level of the cathode current detection voltage is controlled by the value of R1.

4.5. Bus Setting Table By System

			SUB ADDRESS 09 (H)						
			bit6	bit5	bit3	bit2	bit1	bit0	29 pin
			†1	†2	†3	†4	†5	†6	DBL
50 Hz /60 Hz	Conventional (3:4)	Normal screen	*	0	*	0	0	0	0
		Text screen	*	0	*	0	0	1	0
	Wide-aspect (9:16)	Normal screen	Note1	0	*	1	0	0	0
		Text screen	Note1	0	*	1	0	1	0
100 Hz /120 Hz	Flicker-free conventional (3:4)	Normal screen	*	0	Note2	0	1	0	1
		Text screen	*	0	Note2	0	1	1	1
	Flicker-free wide-aspect (9:16)	Normal screen	Note1	0	Note2	1	1	0	1
		Text screen	Note1	0	Note2	1	1	1	1
60 Hz	HDTV		0	1	*	1	0	0	Note4

†1: Frame position switching

(**Note 1:** This switch is effective when the aspect ratio is switched to 9:16 in †4; "0" moves the frame position to the center, and "1" moves it to the upper portion of the screen.)

†2: HDTV mode switching

†3: Flicker-free system switching

(**Note 2:** Switching flicker-free system is performed with this setting; this switch must be set to "0" at 100 Hz, and must be set to "1" at 120 Hz.)

†4: Aspect ratio switching

†5: Flicker-free switching

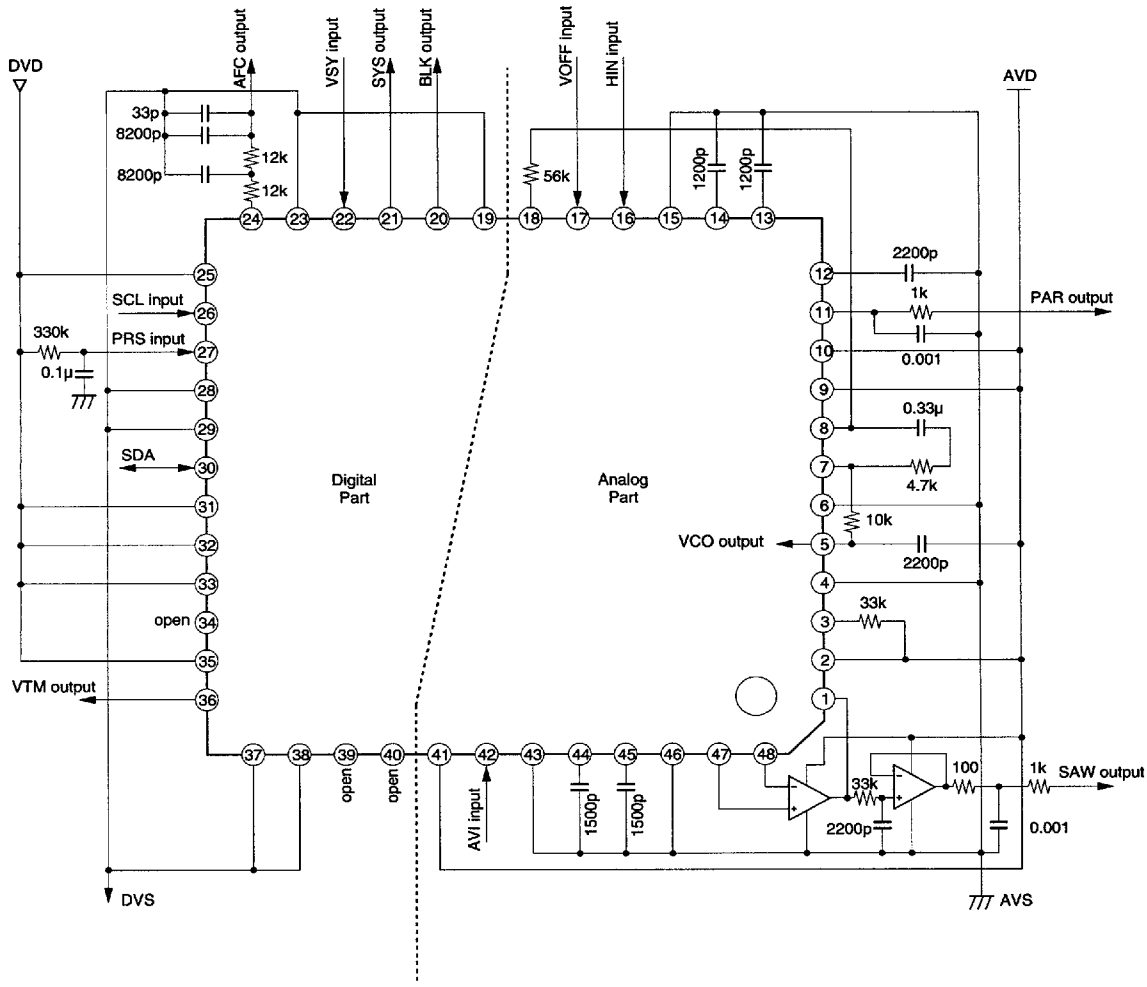
(**Note 3:** This switching is effective only when DBL is set to "1"; when "0", the system operates at 50/60 Hz only, regardless of this switching.)

†6: Text screen switching

DBL: Flicker-free enable pin (Pin 29 of the IC)

(**Note 4:** This is a protective pin for sets that only operate at 50/60 Hz; this pin disables the flicker-free switching †5. Therefore, in HDTV sets, set this pin to "0" for EDTV compatibility and to "1" for flicker-free compatibility.)

Application Circuit



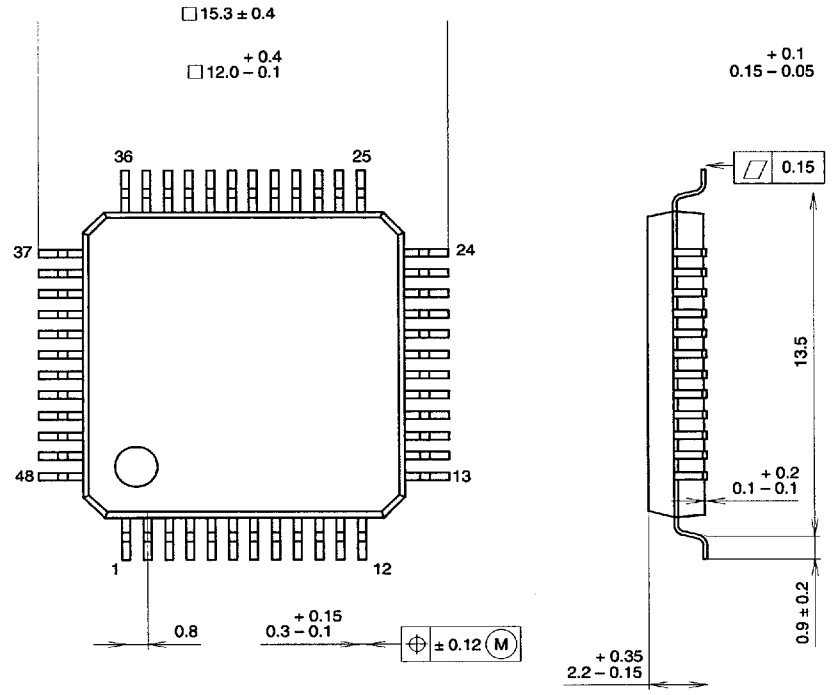
Note 1: The analog and digital power supplies are separated.

Note 2: The resistor for Pin 18 must be attached as close to the pin as possible.

Note 3: B-class temperature characteristics are specified for the capacitors.

Package Outline Unit : mm

48PIN QFP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	QFP-48P-L04
EIAJ CODE	*QFP048-P-1212-B
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER / PALLADIUM PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	0.7g