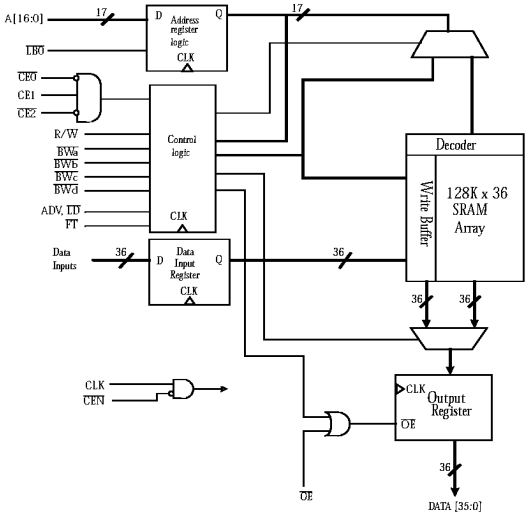
AS7C3128K32Z
AS7C3128K36Z

3.3V 128K×32/36 synchronous burst SRAM with NTD™

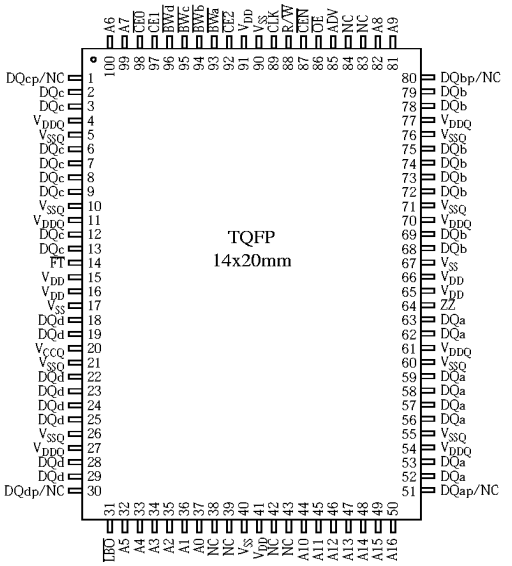
Features

- Organization: 131,072 words × 32 or 36 bits
- NTD™ architecture for efficient bus operation
- Fast clock speeds to 166 MHz
- Fast clock to data access: 3.5/3.8/4/5 ns
- Fast $\overline{OE}$ access time: 3.5/3.5/3.8/4 ns
- Fully synchronous register-to-register operation
- Single register 'flow-through' mode
- 4 word burst mode
- Synchronous and Asynchronous output enable control
- Economical 100-pin TQFP package
- ZZ sleep mode for lower power
- Byte write enables
- Single R/$\overline{W}$ control pin
- Clock enable for operation hold
- Multiple chip enables for easy expansion
- 3.3V ± 5% core power supply
- 2.5V or 3.3V I/O operation with separate V_{DDQ}
- Automatic power down: 10 mW typical standby power
- Pipeline burst architecture available (AS7C3128K32P)

Logic block diagram



Pin arrangement



Note: pins 1,30,51,80 are NC for ×32

Selection guide

	7C3128K36-3.5	7C3128K36-3.8	7C3128K36-4	7C3128K36-5	Units
Minimum cycle time	6	6.7	7.5	10	ns
Maximum clock frequency	166.7	150	133.3	100	MHz
Maximum pipelined clock access time	3.5	3.8	4	5	ns
Maximum operating current	350	325	300	250	mA
Maximum standby current	60	60	60	60	mA
Maximum CMOS standby current (DC)	5	5	5	5	mA

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Functional description

The AS7C3128K32Z and AS7C3128K36Z are high performance 4Mbit CMOS Synchronous SRAMs organized as 131,072 words × 32 or 36 bits which incorporate a two stage register-register pipeline for highest frequency on any given technology.

This variation of the 4Mb sychronous SRAM uses the No Turnaround Delay (NTD™) architecture, featuring an enhanced write operation that improves bandwidth over pipeline burst devices. In a normal pipeline burst device, the write data, command, and address are all applied to the device on the same clock edge. If a read command follows this write information, the system must wait for two 'dead' cycles for valid data to become available. These dead cycles can significantly reduce overall bandwidth for applications requiring random access or read-modify-write operations.

NTD™ devices use the memory bus more efficiently by introducing a write 'latency' which matches the two cycle read latency. Write data is applied two cycles after the write command and address, allowing the read pipeline to clear. With NTD™, write and read operations can be used in any order without producing dead bus cycles.

The single register flow-through mode of the AS7C3128K32Z (and AS7C3128K36Z) can disable output circuit registers. This allows the device to operate in 2-1-1-1 mode rather than 3-1-1-1 found in two-stage pipeline architecture timing. The single register flow-through mode sacrifices access and cycle times for lower latency. Consult AC timing parameters for more details.

Assert R/$\overline{W}$ low to perform write cycles. Byte write enable controls write access to specific bytes, or can be tied low for full 32/36 bit writes. Write enable signals, along with the write address, are registered on a rising edge of the clock. Write data is applied to the device two clock cycles later. Unlike some asynchronous SRAMs, output enable $\overline{OE}$ does not need to be toggled for write operations; it can be tied low for normal operations. Outputs go to a high impedance state when the device is de-selected by any of the three chip enable inputs In pipeline mode, a two cycle deselect latency allows pending read or write operations to be completed.

Use the ADV (burst advance) input to perform burst read and write operations. When ADV is high, external addresses are ignored, and internal address counters increment in the count sequence specified by the $\overline{LBO}$ control. Any device operations, including burst, can be stalled using the $\overline{CEN}$ clock enable input. If $\overline{CEN}$ is high at the rising edge of clock, all operations are effectively stalled.

The AS7C3128K32Z and AS7C3128K36Z operate with a 3.3V ± 5% power supply for the device core (V_{DD}). DQ circuits use a separate power supply (V_{DDQ}) that operates across 3.3V or 2.5V ranges. They are packaged in a standard 100-pin TQFP.

Capacitance [1]

Parameter	Symbol	Signals	Test conditions	Max	Unit
Input capacitance	C_{IN}	Address and control pins	V_{in} = 0V	5	pF
I/O capacitance	$C_{I/O}$	I/O pins	V_{in} = V_{out} = 0V	7	pF

Write enable truth table (per byte)

$\overline{GWE}$	$\overline{BWE}$	$\overline{BWn}$	WRITEn
L	X	X	T
X	L	L	T
H	H	X	F
H	L	H	F [†]

Key: X = Don't Care, L = Low, H = High.
[†] Valid read.

Signal descriptions

Signal	I/O	Properties	Description
CLK	I	CLOCK	Clock. All inputs except $\overline{OE}$ are synchronous to this clock.
A0–A16	I	SYNC	Address. Sampled when all chip enables are active and $\overline{ADSC}$ or $\overline{ADSP}$ are asserted.
DQ[a,b,c,d]	I/O	SYNC	Data. Driven as output when the chip is enabled and $\overline{OE}$ is active.
$\overline{CE0}$	I	SYNC	Master chip enable. Sampled on clock edges when $\overline{ADSP}$ or $\overline{ADSC}$ is active. When $\overline{CE0}$ is inactive, $\overline{ADSP}$ is blocked. Refer to the SYNCHRONOUS TRUTH TABLE for more information.
CE1, $\overline{CE2}$	I	SYNC	Synchronous chip enables. Active HIGH and active Low, respectively. Sampled on clock edges when $\overline{ADSC}$ is active or when $\overline{CE1}$ and $\overline{ADSP}$ are active.
$\overline{ADSP}$	I	SYNC	Address strobe processor. Asserted LOW to load a new bus address or to enter standby mode.
$\overline{ADSC}$	I	SYNC	Address strobe controller. Asserted LOW to load a new address or to enter standby mode.
$\overline{ADV}$	I	SYNC	Advance. Asserted LOW to continue burst read/write.
$\overline{GWE}$	I	SYNC default = HIGH	Global write enable. Asserted LOW to write all 36 bits. When High, $\overline{BWE}$ and $\overline{WE0}$–$\overline{WE3}$ control write enable. *This signal is internally pulled High.*
$\overline{BWE}$	I	SYNC default = LOW	Byte write enable. Asserted LOW with $\overline{GWE}$ = HIGH to enable effect of $\overline{WE0}$–$\overline{WE3}$ inputs. *This signal is internally pulled Low.*
$\overline{BW[a,b,c,d]}$	I	SYNC	Write enables. Used to control write of individual bytes when $\overline{GWE}$ = HIGH and $\overline{BWE}$ = Low. If any of $\overline{BW[a:d]}$ is active with $\overline{GWE}$ = HIGH and $\overline{BWE}$ = LOW the cycle is a write cycle. If all $\overline{BW[a:d]}$ are inactive the cycle is a read cycle.
$\overline{OE}$	I	ASYNC	Asynchronous output enable. I/O pins are driven when $\overline{OE}$ is active and the chip is synchronously enabled.
$\overline{LBO}$	I	STATIC default = HIGH	Count mode. When driven High, count sequence follows Intel XOR convention. When driven Low, count sequence follows linear convention. *This signal is internally pulled High.*[18]
$\overline{FT}$	I	STATIC	Flow-through mode.When low, enables single register flow-through mode. Connect to V_{DD} if unused or for pipelined operation.
ZZ	I	ASYNC	Sleep. Places device in low power mode; data is retained. Connect to GND if unused.

Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Power supply voltage relative to GND	V_{DD}, V_{DDQ}	–0.5	+4.6	V
Input voltage relative to GND (input pins)	V_{IN}	–0.5	+4.6	V
Input voltage relative to GND (I/O pins)	V_{IN}	–0.5	V_{DDQ} + 0.5	V
Power dissipation	P_D	–	1.2	W
DC output current	I_{OUT}	–	30	mA
Storage temperature (plastic)	T_{stg}	–65	+150	°C
Temperature under bias	T_{bias}	–65	+135	°C

Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect reliability.

Synchronous truth table

$\overline{CE0}$	CE1	$\overline{CE2}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$WRITE_n$[†]	$\overline{OE}$	Address accessed	CLK	Operation
H	X	X	X	L	X	X	X	NA	L to H	Deselect
L	L	X	L	X	X	X	X	NA	L to H	Deselect
L	L	X	H	L	X	X	X	NA	L to H	Deselect
L	X	H	L	X	X	X	X	NA	L to H	Deselect
L	X	H	H	L	X	X	X	NA	L to H	Deselect
L	H	L	L	X	X	F	L	External	L to H	Begin read
L	H	L	L	X	X	F	H	External	L to H	Begin read
L	H	L	H	L	X	F	L	External	L to H	Begin read
L	H	L	H	L	X	F	H	External	L to H	Begin read
X	X	X	H	H	L	F	L	Next	L to H	Cont. read
X	X	X	H	H	L	F	H	Next	L to H	Cont. read
X	X	X	H	H	H	F	L	Current	L to H	Suspend read
X	X	X	H	H	H	F	H	Current	L to H	Suspend read
H	X	X	X	H	L	F	L	Next	L to H	Cont. read
H	X	X	X	H	L	F	H	Next	L to H	Cont. read
H	X	X	X	H	H	F	L	Current	L to H	Suspend read
H	X	X	X	H	H	F	H	Current	L to H	Suspend read
L	H	L	H	L	X	T	X	External	L to H	Begin write
X	X	X	H	H	L	T	X	Next	L to H	Cont. write
H	X	X	X	H	L	T	X	Next	L to H	Cont. write
X	X	X	H	H	H	T	H	Current	L to H	Suspend write
H	X	X	X	H	H	T	H	Current	L to H	Suspend write

Key: X = Don't Care, L = Low, H = High.
[†]See Write enable truth table for more information.

Recommended operating conditions

Parameter		Symbol	Min	Nominal	Max	Unit
Supply voltage		V_{DD}	3.135	3.3	3.6	V
		GND	0.0	0.0	0.0	V
I/O supply voltage		V_{DDQ}	2.35	2.5 or 3.3	3.6	V
		GND_Q	0.0	0.0	0.0	V
Input voltages	Address and control pins	V_{IH}	2.0	–	4.5	V
		V_{IL}	–0.5*	–	0.8	V
	I/O pins	V_{IH}	2.0	–	V_{DDQ} + 0.5	V
		V_{IL}	-0.5*	–	0.8	
Ambient operating temperature		T_A	0	–	70	℃

* V_{IL} min = –2.0V for pulse width less than 0.2 x t_{RC}.

DC electrical characteristics over operating range

Parameter	Symbol	Test conditions	-166 Min	-166 Max	-150 Min	-150 Max	-133 Min	-133 Max	-100 Min	-100 Max	Unit
Input leakage current	$\lvert I_{LI} \rvert$	V_{DD} = Max, V_{in} = GND to V_{DD}	–	2	–	2	–	2	–	2	µA
Output leakage current	$\lvert I_{LO} \rvert$	$\overline{OE} \geq V_{IH}$, V_{DD} = Max, V_{out} = GND to V_{DD}	–	2	–	2	–	2	–	2	µA
Operating power supply current	I_{CC}	$\overline{CE} = V_{IL}$, $CE = V_{IH}$, $\overline{CE} = V_{IL}$, f = f_{max}, I_{out} = 0 mA	–	350	–	325	–	300	–	250	mA
Standby power supply current	I_{SB}	Deselected, f = f_{max}	–	60	–	60	–	60	–	60	mA
	I_{SB1}	Deselected, f = 0, all $V_{IN} \leq 0.2V$ or $\geq V_{DD} - 0.2V$	–	5	–	5	–	5	–	5	mA
Output voltage	V_{OL}	I_{OL} = 8 mA, V_{DDQ} = 3.6V	–	0.4	–	0.4	–	0.4	–	0.4	V
	V_{OH}	I_{OH} = –8 mA, V_{DDQ} = 3.0V	2.4	–	2.4	–	2.4	–	2.4	–	V

Timing characteristics over operating range

Parameter	Symbol	-3.5 Min	-3.5 Max	-3.8 Min	-3.8 Max	-4 Min	-4 Max	-5 Min	-5 Max	Unit	Notes
Clock frequency	F_{MAX}	-	166	-	150	-	133	-	100	MHz	1
Cycle time (pipelined mode)	t_{CYC}	6	-	6.6	-	7.5	-	10	-	ns	
Clock access time (pipelined mode)	t_{CD}	-	3.5	-	3.8	-	4	-	5	ns	
Clock access time (flow-through mode)	t_{CDF}	-	6	-	6.6	-	7.5	-	10	ns	
Output enable Low to data valid	t_{OE}	-	3.5	-	3.5	-	3.8	-	4	ns	
Clock High to output Low Z	t_{LZC}	0	-	0	-	0	-	0	-	ns	8
Data output hold from clock High	t_{OH}	1.5	-	1.5	-	1.5	-	2	-	ns	8
Output enable Low to output Low Z	t_{LZOE}	1	-	1	-	1.5	-	2	-	ns	8
Output enable High to output High Z	t_{HZOE}	-	3	-	3.5	-	4	-	4	ns	8
Clock High to output High Z	t_{HZC}	-	2.5	-	3	-	3.5	-	3.5	ns	8
Clock High to output High Z	t_{HZCN}	-	1.5	-	1.5	-	2	-	2.5	ns	1,9
Clock High pulse width	t_{CH}	2.4	-	2.6	-	2.8	-	3	-	ns	
Clock Low pulse width	t_{CL}	2.4	-	2.6	-	2.8	-	3	-	ns	
Address and Control setup to clock High	t_{AS}	1	-	1.3	-	1.5	-	1.5	-	ns	
Data setup to clock High	t_{DS}	1	-	1.3	-	1.5	-	1.5	-	ns	
Write setup to clock High	t_{WS}	1	-	1.3	-	1.5	-	1.5	-	ns	
Chip select setup to clock High	t_{CSS}	1	-	1.3	-	1.5	-	1.5	-	ns	
Address hold from clock High	t_{AH}	0.5	-	0.5	-	0.5	-	0.5	-	ns	
Data hold from clock High	t_{DH}	0.5	-	0.5	-	0.5	-	0.5	-	ns	
Write hold from clock High	t_{WH}	0.5	-	0.5	-	0.5	-	0.5	-	ns	
Chip select hold from clock High	t_{CSH}	0.5	-	0.5	-	0.5	-	0.5	-	ns	
Output rise time (0 pF load)	t_R	1.5	-	1.5	-	1.5	-	1.5	-	V/ns	1
Output fall time (0 pF load)	t_F	1.5	-	1.5	-	1.5	-	1.5	-	V/ns	1

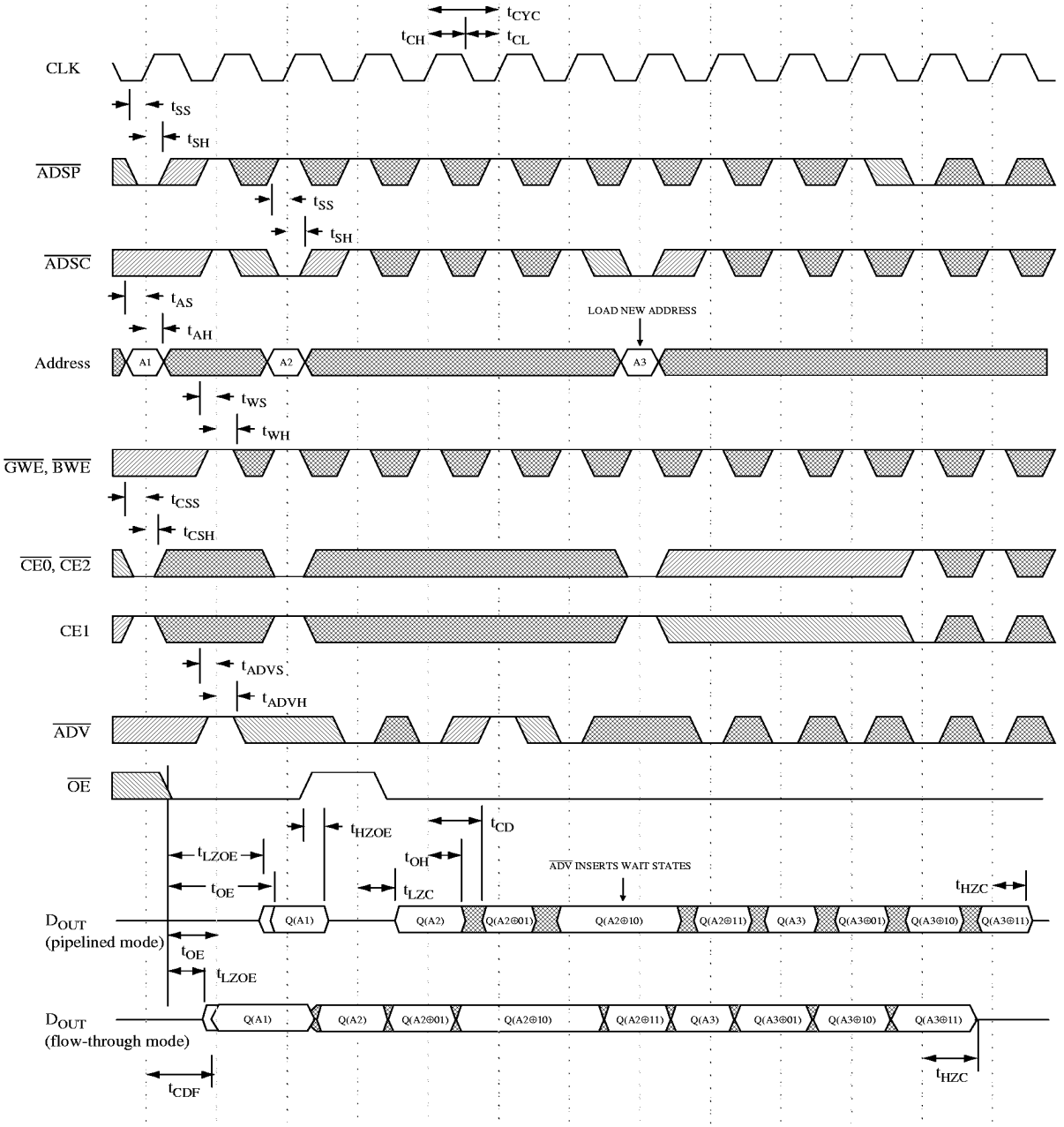
See "Notes" on page 187.

SRAM

Key to switching waveforms

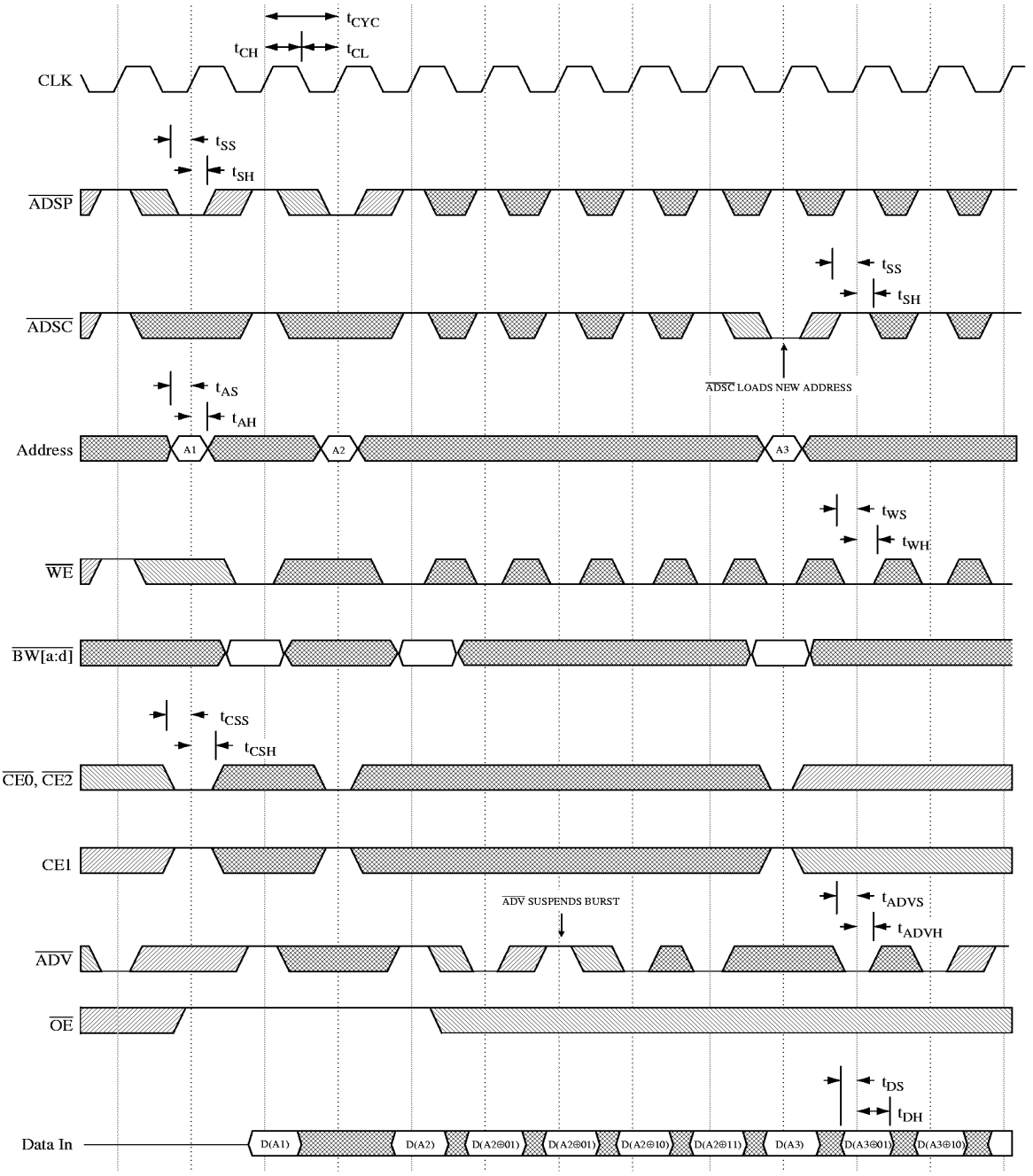
Rising input Falling input Undefined output/don't care

Timing waveform of read cycle



Note: ⊕ = XOR when MODE = High/No Connect; ⊕ = ADD when MODE = Low.
$\overline{WE}$[0:3] is don't care.

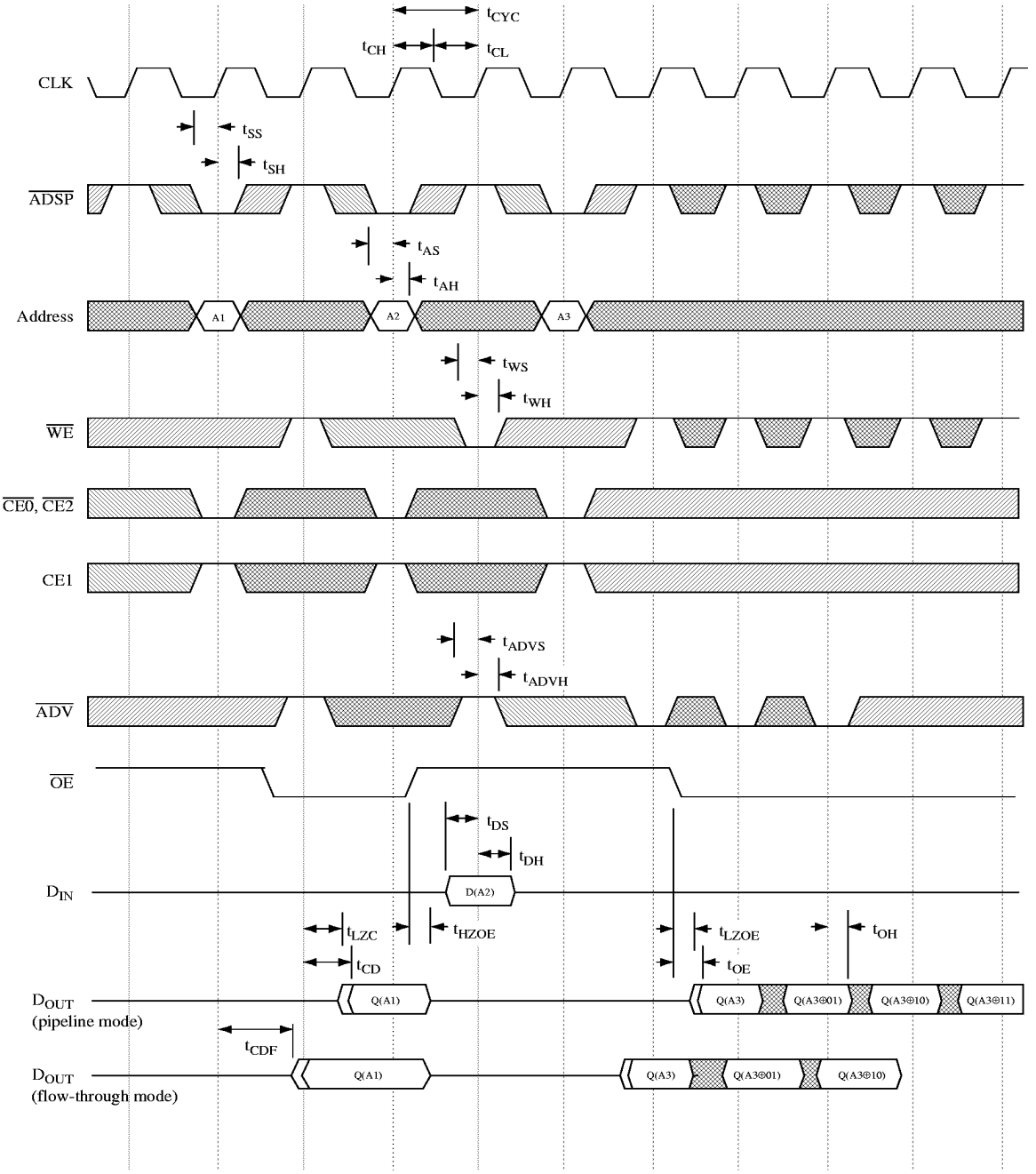
Timing waveform of write cycle



Note: ⊕ = XOR when MODE = High/No Connect; ⊕ = ADD when MODE = Low.

SRAM

Timing waveform of read/write cycle



Note: ⊕ = XOR when MODE = High/No Connect; ⊕ = ADD when MODE = Low.

Notes

1 This parameter is guaranteed but not tested.
2 For test conditions, see AC Test Conditions, Figures A, B, C.
3 This parameter is sampled and not 100% tested.
4 This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK. All other synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of CLK when chip is enabled.
5 Typical values measured at 3.3V, 25 ℃ and 10 ns cycle time.
6 I_{CC} given with no output loading. I_{CC} increases with faster cycle times and greater output loading.
7 Transitions are measured ±500 mV from steady state voltage. Output loading specified with C_L = 5 pF as in Figure C.
8 t_{HZOE} is less than t_{LZOE}; and t_{HZC} is less than t_{LZC} at any given temperature and voltage.
9 t_{HZCN} is a 'no load' parameter to indicate exactly when SRAM outputs have stopped driving.

AC test conditions

- Output Load: see Figure B, except for t_{LZC}, t_{LZOE}, t_{HZOE}, t_{HZC} see Figure C.
- Input pulse level: GND to 3V. See Figure A.
- Input rise and fall time (Measured at 0.3V and 2.7V): 2 ns. See Figure A.
- Input and output timing reference levels: 1.5V.

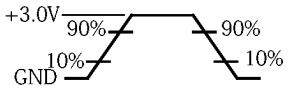


Figure A: Input waveform

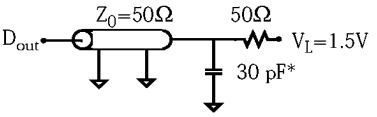


Figure B: Output load (A)

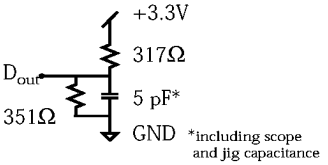


Figure C: Output load (B)

AS7C3128K36Z and AS7C3128K32Z ordering information

Package	Functionality	166 MHz	150 MHz	133 MHz	100 MHz
TQFP	PBSRAM	AS7C3128K32P-3.5TQC	AS7C3128K32P-3.8TQC	AS7C3128K32P-4TQC	AS7C3128K32P-5TQC
TQFP	PBSRAM	AS7C3128K36P-3.5TQC	AS7C3128K36P-3.8TQC	AS7C3128K36P-4TQC	AS7C3128K36P-5TQC

AS7C3128K36Z and AS7C3128K32Z part numbering system

AS7C	3	128K36	P	-XX	XX	C
SRAM prefix	Operating voltage	Part number, organization	Timing Z=NTD™ timing P=PBSRAM	access time (ns)	Package: TQ = TQFP	Commercial temperature, 0 ℃ to 70 ℃