SRAM

512K x 8 SRAM

ULTRA HIGH SPEED-PLASTIC SRAM
REVOLUTIONARY PINOUT

MILITARY TEMPERATURE
OPERATING RANGE -55ºC to +125ºC

FEATURES
- Ultra High Speed, 83MHz Asynchronous Operation
- Extended Testing Over -55ºC to +125ºC
- Fully Static, No Clocks
- Data Retention Functionality Testing
- Easy memory expansion with CE\ and OE\ options
- All inputs and outputs are TTL-compatible
- Plastic 36 pin PSOJ is fully compatible with the Ceramic 36 pin SOJ
- Single +5V Power Supply +/- 10%
- 3.3V Future Offering
- Industrial and Military Temperature Range
- Cost Economical Plastic Encapsulation

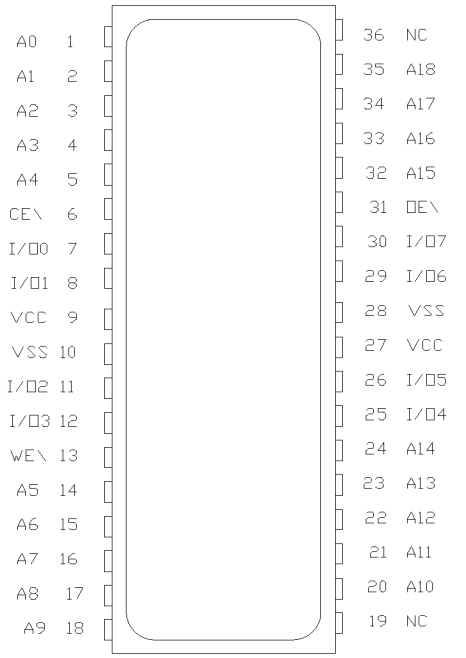
OPTIONS MARKING
- **Timing**

12ns access	-12
15ns access	-15
17ns access	-17
20ns access	-20

- **Package(s)**

Plastic SOJ	ECJ	No. 503

PIN ASSIGNMENT (Top View)
36-Pin PSOJ



GENERAL DESCRIPTION

The AS5C4008DJ offers the convenience and reliability of the AS5C4008 SRAM and has the cost advantage of a durable plastic.

The AS5C4008DJ is tested to military specifications. When a device is operated beyond commercial temperatures the overall characteristics of the device will change. ASI ensures that this device will behave in an expected manner in military applications due to the extensive characterizations performed to meet military standards.

. ASI certifies that the AS5C4008DJ will retain data in Data Retention Mode under operating conditions characterized during test conditions. This is a crucial point for systems that operate under extreme temperature conditions.

For flexibility in high-speed memory applications, ASI offers chip enable (CE\) and output enable (OE\) capabilities.

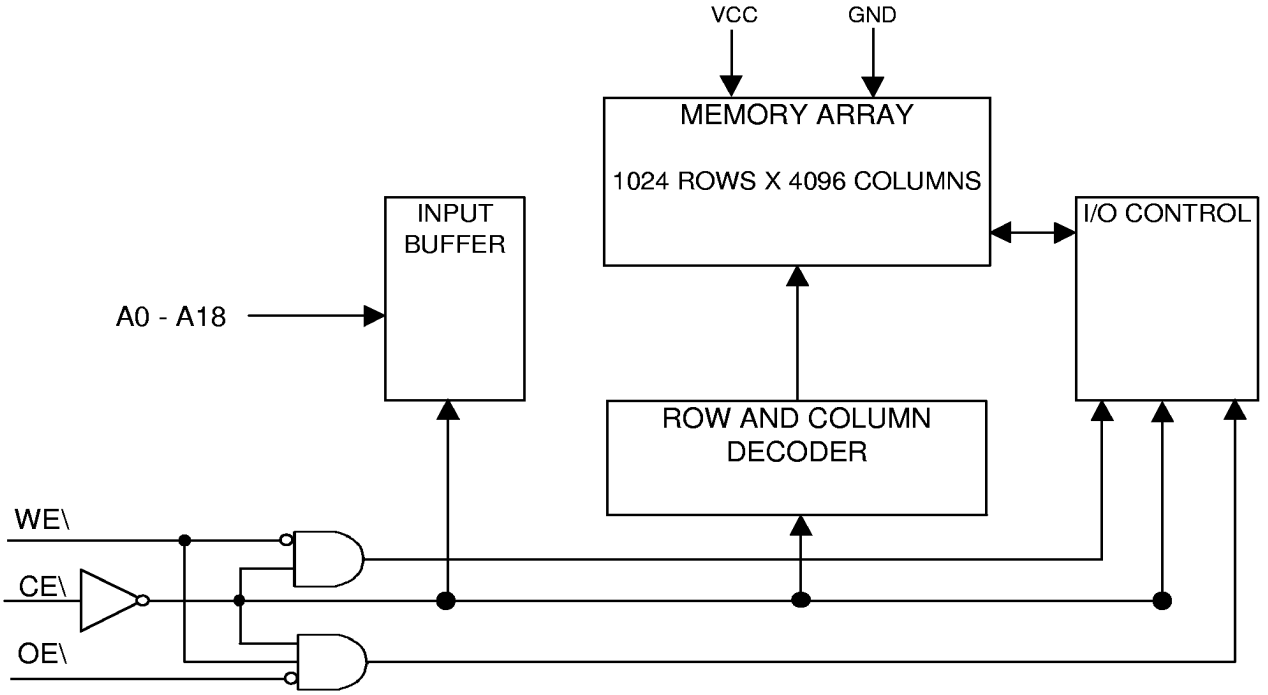
These features can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable (WE\) and CE\ inputs are both LOW. Reading is accomplished when WE\ remains HIGH and CE\ and OE\ go LOW.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL-compatible.

The AS5C4008DJ is PSOJ footprint compatible with SMD 5692-95600.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	OE\	CE\	WE\	I/O	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

X = Don't Care

PIN FUNCTIONS

A0 - A18	Address Inputs
WE\	Write Enable
CE\	Chip Enable
OE\	Output Enable
I/O_0 - I/O_7	Data Inputs/Outputs
V_{CC}	Power
V_{SS}	Ground
NC	No Connections

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss
Vcc .....-.5V to +7.0V
Storage Temperature (Plastics) .....-65°C to +150°C
Short Circuit Output Current (per I/O).....20mA
Voltage on any Pin Relative to Vss.....-5V to Vcc+1 mA
Junction Temperature**.....+150°C
Power Dissipation .....1 W

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
** Maximum junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow, and humidity (plastics).

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(-55°C ≤ T A ≤ 125°C; Vcc = 5V ±10%)- Military Temps

			-12		-15		-17		-20			
SYMBOL	DESCRIPTION	CONDITIONS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
I_{CC}	Power Supply Current: Operating	CE\ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^{t}RC OUTPUTS OPEN		215		210		200		190	mA	3
I_{SBT1}	Power Supply Current: Standby	CE\ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^{t}RC OUTPUTS OPEN		65		55		50		50	mA	
I_{SBC}		CE\ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0		10		10		10		10	mA	
V_{IH}	Input High (Logic 1) Voltage		2.2	VCC+.5	2.2	VCC+.5	2.2	VCC+.5	2.2	VCC+.5	V	1
V_{IL}	Input Low (Logic 0) Voltage		-0.5	0.8	-0.5	0.8	-0.5	0.8	-0.5	0.8		1,2
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	-5	5	-5	5	-5	5	-5	5	µA	
I_{LO}	Output Leakage Current	Output(s) disabled 0V ≤ V_{OUT} ≤ V_{CC}	-5	5	-5	5	-5	5	-5	5	µA	
V_{OH}	Output High Voltage	I_{OH} = -4.0 mA	2.4		2.4		2.4		2.4		V	1
V_{OL}	Output Low Voltage	I_{OL} =8 mA		0.4		0.4		0.4		0.4	V	1
V_{CC}	Supply Voltage		4.5	5.5	4.5	5.5	4.5	5.5	4.5	5.5	V	1

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(-40°C ≤ T A ≤ 80°C; Vcc = 5V ±10%)- Industrial Temps

			-12		-15		-17		-20			
SYMBOL	DESCRIPTION	CONDITIONS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
I_{CC}	Power Supply Current: Operating	CE\ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^{t}RC OUTPUTS OPEN		210		205		195		185	mA	3
I_{SBT1}	Power Supply Current: Standby	CE\ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^{t}RC OUTPUTS OPEN		50		50		50		50	mA	
I_{SBC}		CE\ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0		10		10		10		10	mA	
V_{IH}	Input High (Logic 1) Voltage		2.2	VCC+.5	2.2	VCC+.5	2.2	VCC+.5	2.2	VCC+.5	V	1
V_{IL}	Input Low (Logic 0) Voltage		-0.5	0.8	-0.5	0.8	-0.5	0.8	-0.5	0.8		1,2
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	-2	2	-2	2	-2	2	-2	2	µA	
I_{LO}	Output Leakage Current	Output(s) disabled 0V ≤ V_{OUT} ≤ V_{CC}	-2	2	-2	2	-2	2	-2	2	µA	
V_{OH}	Output High Voltage	I_{OH} = -4.0mA	2.4		2.4		2.4			2.4	V	1
V_{OL}	Output Low Voltage	I_{OL} = 8 mA		0.4		0.4		0.4		0.4	V	1
V_{CC}	Supply Voltage		4.5	5.5	4.5	5.5	4.5	5.5	4.5	5.5	V	1

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 5) (-55°C ≤ T_A ≤ 125°C; V_{CC} = 5V ±10%)

DESCRIPTION		-12		-15		-17		-20			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle											
READ cycle Time	t_{RC}	12		15		17		20		ns	
Address access time	t_{AA}		12		15		17		20	ns	
Chip Enable access time	t_{ACE}		12		15		17		20	ns	
Output hold from address change	t_{OH}	2		2		2		2		ns	
Chip Enable to output in Low-Z	t_{LZCE}	2		2		2		2		ns	4, 6, 7
Chip disable to output in High-Z	t_{HZCE}		6		7		8		8	ns	4, 6, 7
Chip Enable to power-up time	t_{PU}	0		0		0		0		ns	4
Chip disable to power-down time	t_{PD}		12		15		17		20	ns	4
Output Enable access time	t_{AOE}		6		7		8		8	ns	
Output Enable to output in Low-Z	t_{LZOE}	0		0		0		0		ns	4, 6, 7
Output disable to output in High-Z	t_{HZOE}		6		7		8		8	ns	4, 6, 7
WRITE Cycle											
WRITE cycle time	t_{WC}	12		15		17		20		ns	
Chip Enable to end of write	t_{CW}	9		10		11		12		ns	
Address valid to end of write	t_{AW}	9		10		11		12		ns	
Address setup time	t_{AS}	0		0		0		0		ns	
Address hold from end of write	t_{AH}	0		0		0		0		ns	
WRITE pulse width	t_{WP1}	9		10		11		12		ns	
WRITE pulse width	t_{WP2}	12		13		14		15		ns	
Data setup time	t_{DS}	6		7		7		8		ns	
Data hold time	t_{DH}	0		0		0		0		ns	
Write disable to output in Low-Z	t_{LZWE}	2		2		2		2		ns	4, 6, 7
Write Enable to output in High-Z	t_{HZWE}	0	6	0	7	0	8	0	8	ns	4, 6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

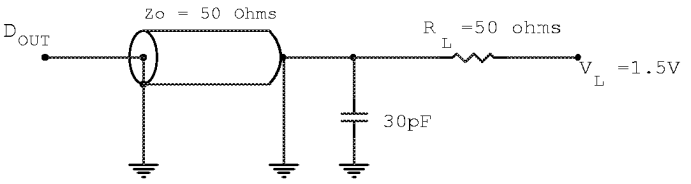


Fig. 1 Output Load Equivalent

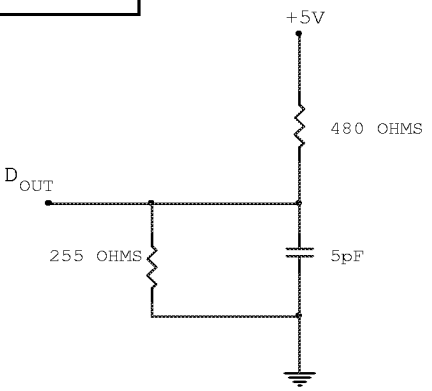


Fig. 2 Output Load Equivalent

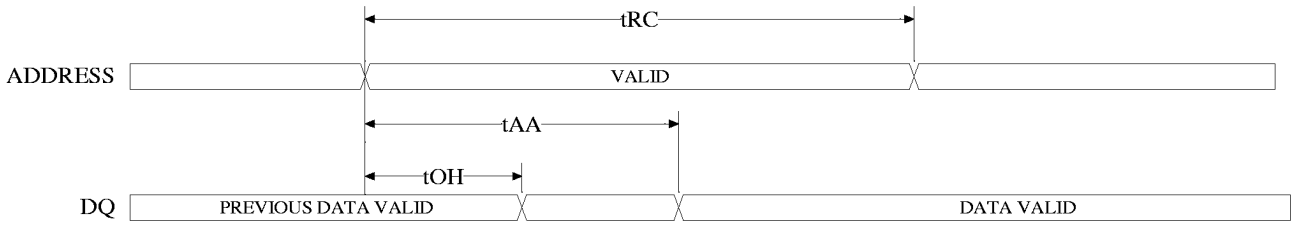
CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Output Capacitance	T_A = 25°C; 1 = MHz	C_I	8	pF	4
Input Capacitance	V_{CC} = 5V	C_O	8	pF	4

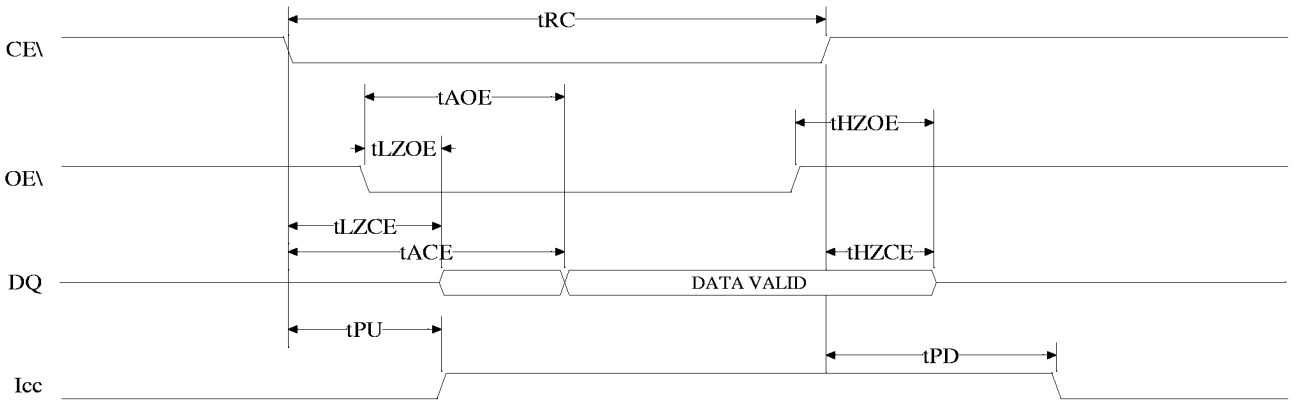
NOTES

1. All voltages referenced to V_{SS} (GND).
2. -2V for pulse width < 20ns
3. I_{CC} is dependent on output loading and cycle rates.
4. This parameter is guaranteed but not tested.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^tLZCE, ^tLZWE, ^tLZOE, ^tHZCE, ^tHZOE and ^tHZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±200mV from steady state voltage.
7. At any given temperature and voltage condition, ^tHZCE is less than ^tLZCE, and ^tHZWE is less than ^tLZWE.
8. WE\ is HIGH for READ cycle.
9. Device is continuously selected. Chip enables and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^tRC = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Output enable (OE\) is inactive (HIGH).
14. Output enable (OE\) is active (LOW).
15. ASI does not warrant functionality nor reliability of any product in which the junction temperature exceeds 150°C. Care should be taken to limit power to acceptable levels.

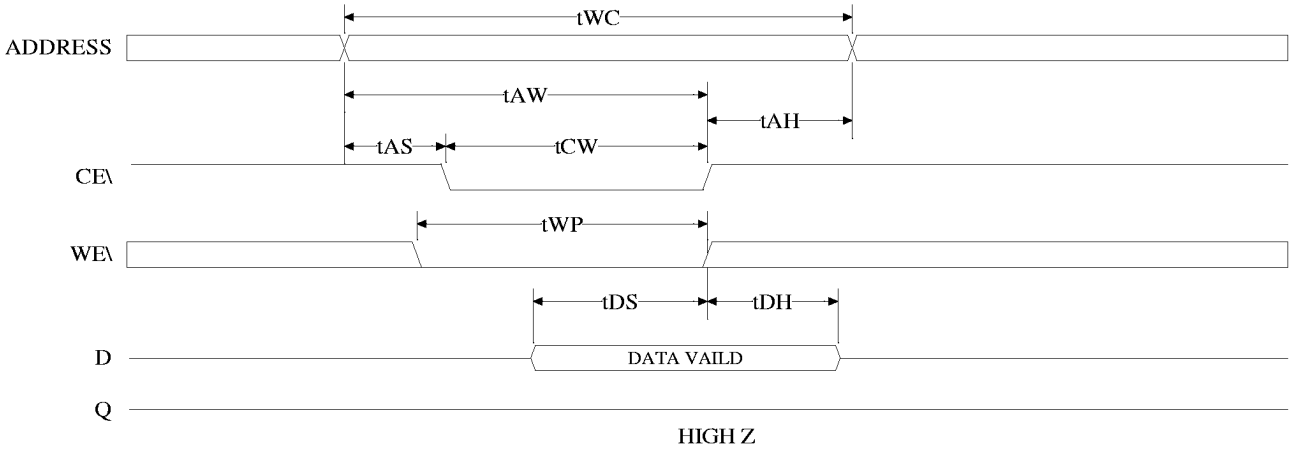
READ CYCLE NO. 1 [8,9]
(Write Enabled Controlled)



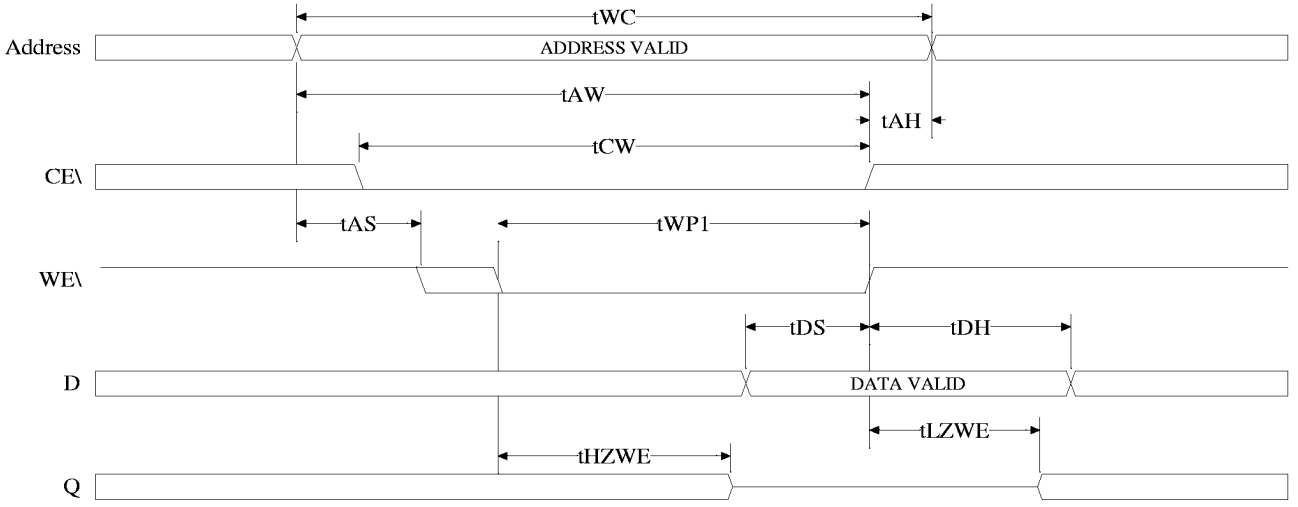
READ CYCLE NO. 2 [7,8,10]
(Write Enabled Controlled)



WRITE CYCLE NO. 1 [12]
(Chip Enabled Controlled)



WRITE CYCLE NO. 2 [12, 13]
(Write Enabled Controlled)



WRITE CYCLE NO. 3 [7, 12, 14]
(Write Enabled Controlled)