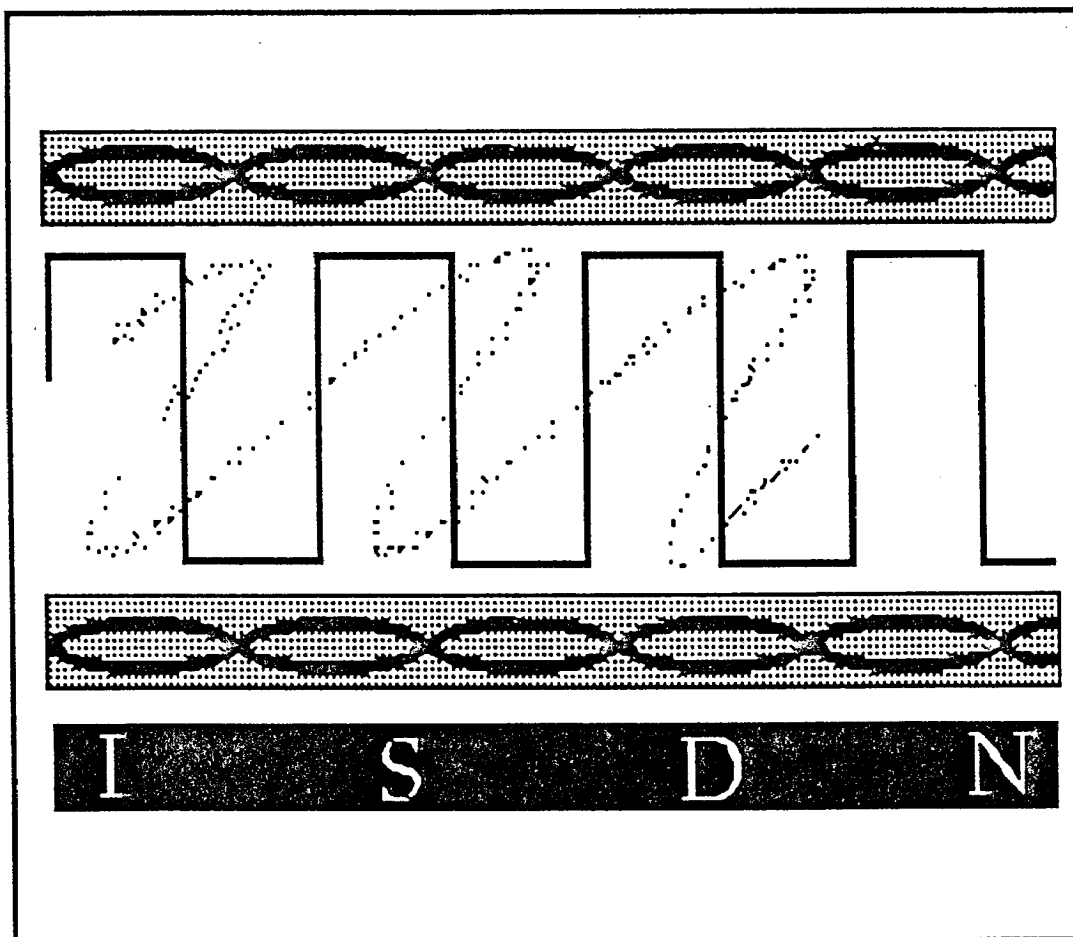




# Am2091 IEC-Q™ ISDN Echocancellation Circuit

Advanced  
Micro  
Devices

Preliminary Data Sheet  
Version C  
7/90



Publication #	Rev.	Amendment
11892	F	/0
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## 1. Basic System Functions

- Full duplex data transmission and reception at the U reference point according to the layer 1 Specification of the American National Standard Institute ANSI® T1.601-1988.
  - 144 kbps user bit rate over a two wire subscriber loop.
  - 2B1Q block code (2 binary, 1 quaternary).
  - 4 kbps maintenance channel for execution of data loop back commands and monitoring transmission errors.
  - Activation and deactivation procedure.
  - Satisfies transmission requirements for loop#1 through loop#15 of ANSI's 15 telephone plant test loops.
  - 2.5V nominal pulse amplitude
- IOM™2 interface
  - Optimized for working in conjunction with SBCX, ICC, EPIC™ and IDEC telecom ICs.
  - Handling of the commands and indications contained in the IOM™2 C/I channel for deactivation, activation, supervision of power supply unit and equipment for testing.
  - Data availability via MONITOR channel:
    - CRC transmission errors.
    - Measurement value of the loop current.
    - Echo canceler coefficients and internal status values.
  - Switching of test loops.
  - Generation of synchronized 7.68 MHz clock for SBCX in NT mode.
- Adaption of internal interfaces to the current signal direction by programmable operation modes:
  - LT: Line termination in public or private exchange
  - TE: Terminal mode
  - NT: Network termination connected to SBCX
  - NT-PABX: Trunk module (TDM)
- Built-in wake-up unit for activation from power-down state.
- Adaptive echo cancellation.
- Adaptive equalization.
- Automatic polarity adaption.
- Clock recovery (frame and bit synchronization) in all applications.
- Automatic gain control.
- Low power consumption:
  - standby: 45 mW
  - active: 340 mW
- 44 pin PLCC44 package.

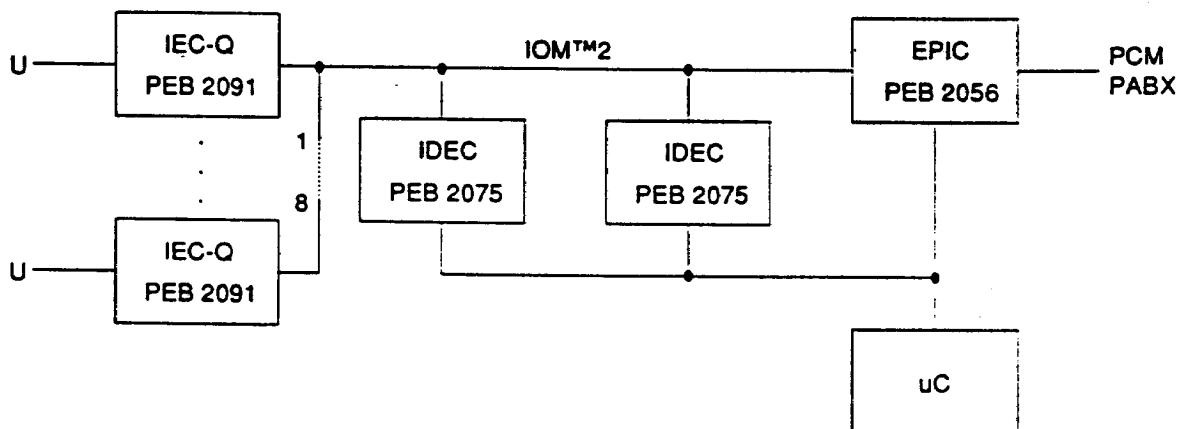
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## 2. Application Overview

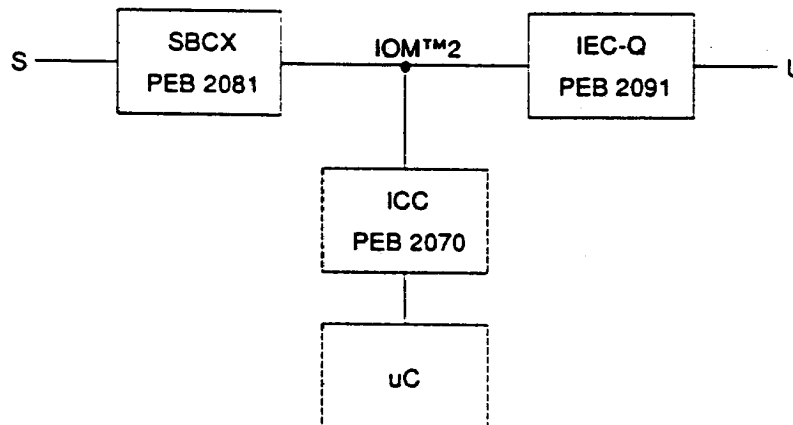
Different hardware configurations as well as different operating modes of the IEC-Q are selectable to cope with the different system requirements.

### LT Application



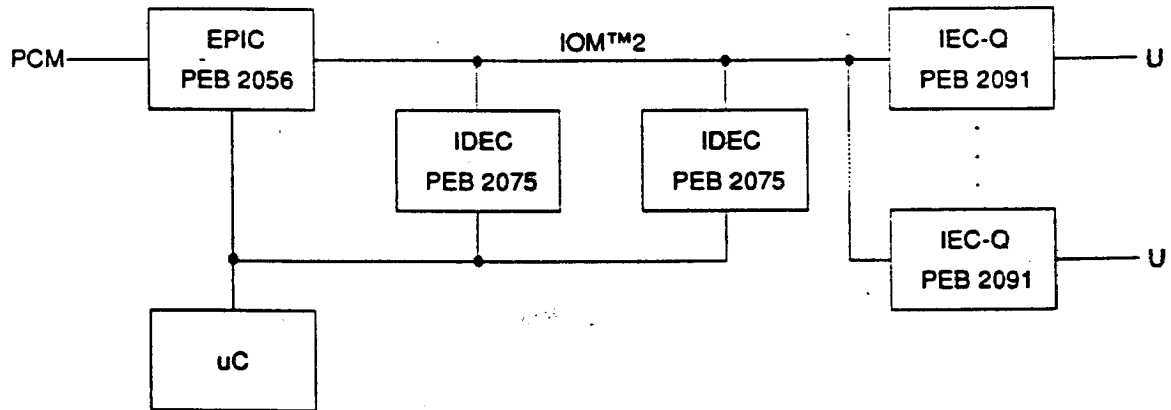
A LT configuration with up to 8 IEC-Q devices can be built with an EPIC and two IDECs. The EPIC controls the C/I channel, the B channel slot assignment and the MONITOR channel handling. The IDEC is a HDLC controller for four independent D channels.

### NT Application



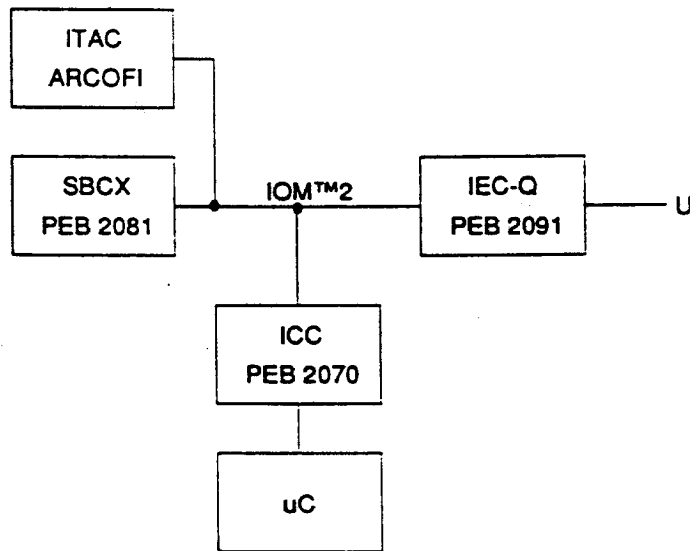
By using the SBCX ( four wire S/T bus interface ) a complete NT1 Network Termination can be built with only two devices. For a more complex and microcontrolled NT, the ICC is used to provide layer 1 maintenance functions.

## NT-PABX Application



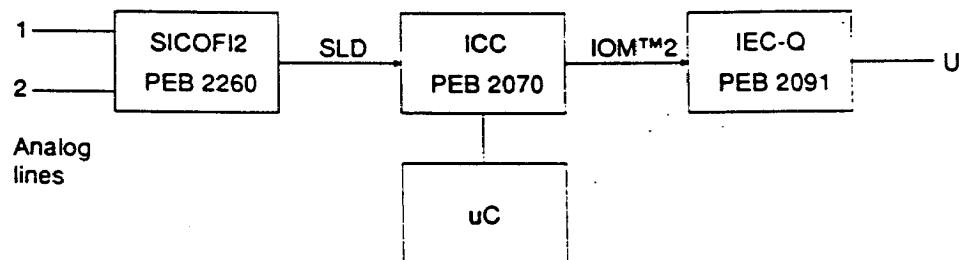
The basic timing is generated by the IEC-Q.

## TE mode



With Voice/Data modules such as ITAC Terminal Adapter Circuit or ARCOFI Audio Ringing Codec Filter, a complete TE configuration can be built in a cost effective manner. Three IOM™ channels are used, the IOM™ data clock is fixed at 1.536 MHz.

## DAML Digital Added Main Line (Pair Gain)



## 2.1 Operation Modes and Functions

MODE	BURST	LT	INPUT PIN				OUTPUT PIN Synchronized to U		Super- Frame- Marker	
			SLOT0	SLOT1	SLOT2	DCL	DCL	CLS		
NT	0	0	0	0	0	-	512 kHz	7.68 MHz	no	*)
NT	0	0	1	0	0	-	512 kHz	7.68 MHz	yes	*)
TE	0	0	0	1	0	-	1.536 MHz	7.68 MHz	no	*)
TE	0	0	1	1	0	-	1.536 MHz	7.68 MHz	yes	*)
PABX	1	0	slot assignment			512 kHz - 4.096 MHz	-	512 kHz		
LT	1	1	slot assignment			512 kHz - 4.096 MHz	-	-		

\*) note : 1 DCL period HIGH phase of FSC at superframe position.  
2 DCL period HIGH phase of FSC at normal frame position  
(see timing diagram).

Tab. 2.1 : modes of operation

Time slot no.	SLOT0	SLOT1	SLOT2	Bit no.	min. Freq. on DCL
0	0	0	0	0 .. 31	512 kHz
1	0	0	1	32 .. 63	1024 kHz
2	0	1	0	64 .. 95	1536 kHz
3	0	1	1	96 .. 127	2048 kHz
4	1	0	0	128 .. 159	2560 kHz
5	1	0	1	160 .. 191	3071 kHz
6	1	1	0	192 .. 223	3584 kHz
7	1	1	1	224 .. 255	4096 kHz

Tab 2.2 : slot assignment

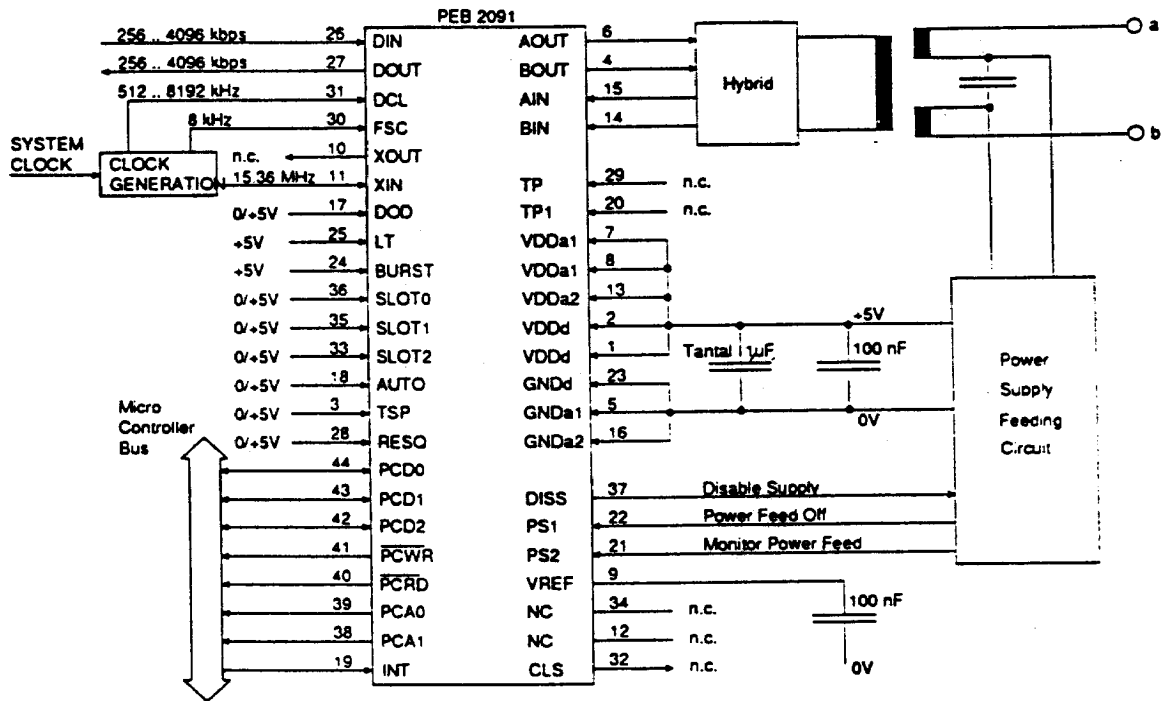
MODE	INPUT PIN AUTO
transparent	0
automatic	1

Tab. 2.3 : EOC mode

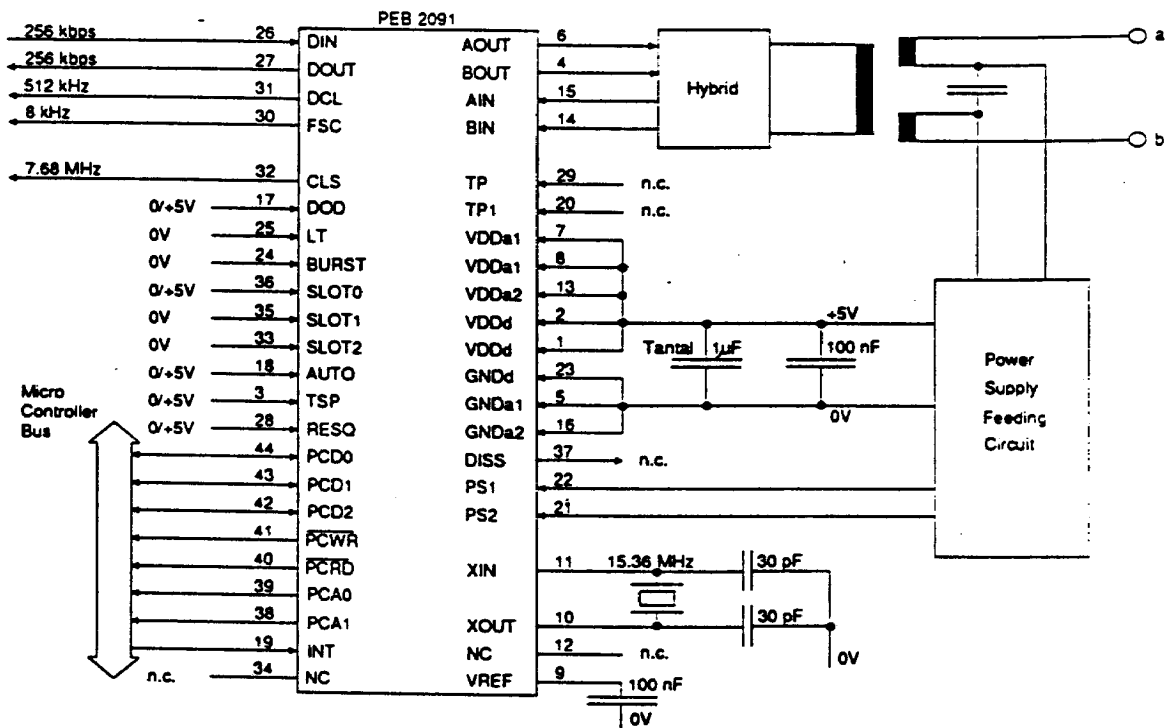
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## 2.2 Interfaces

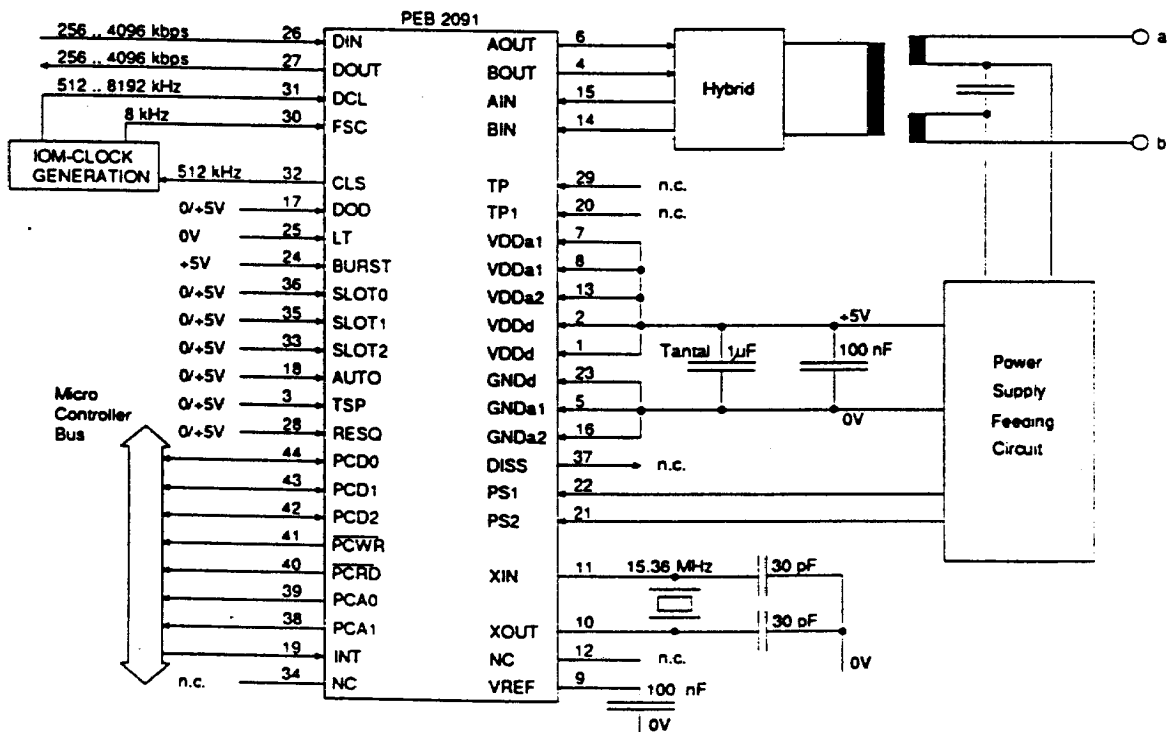
LT mode



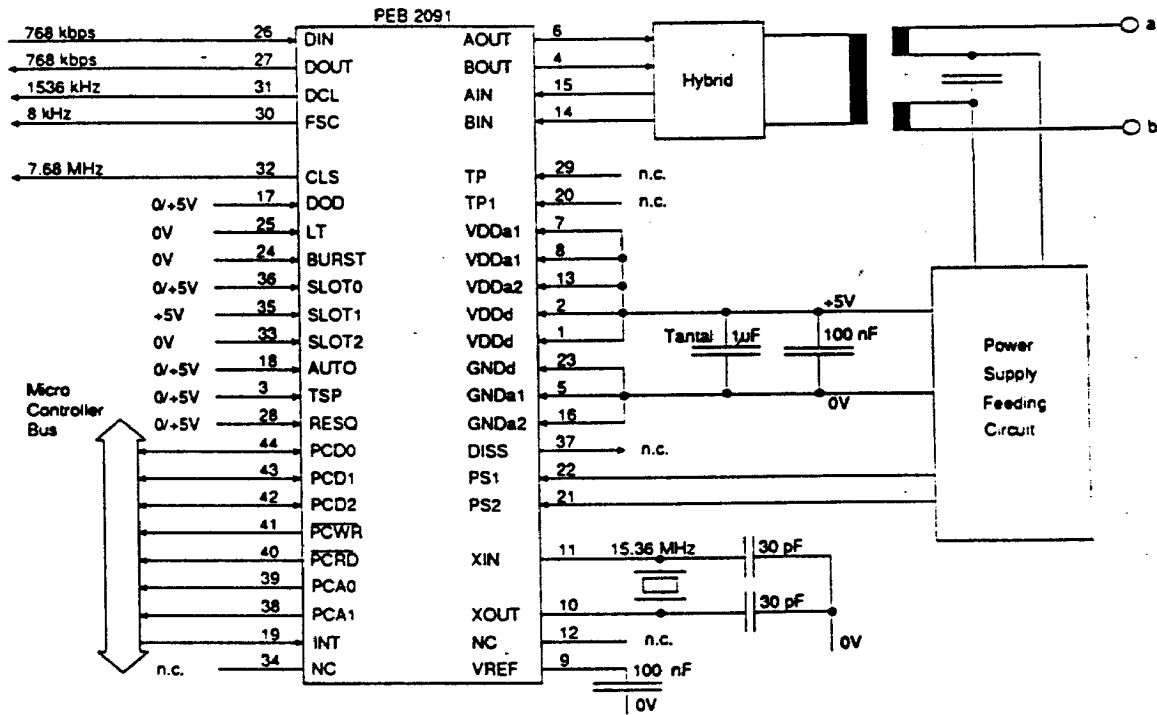
NT mode



NT-PABXmode



TE mode





### 3. Functional Description

The IEC-Q can be subdivided into three main blocks:

- LIU, Line Interface Unit
- SIU, System Interface Unit
- REC, Receiver

The Line Interface Unit (LIU) contains the crystal oscillator and all of the analog functions, such as the A/D converter in the receive path and the pulse-shaping D/A converter and line driver in the transmit path.

The System Interface Unit (SIU) performs the connection between the U and the IOM™ interface. The data channels (2B+D) are transferred after scrambling/descrambling and speed adaption to the appropriate frame. A complete activation and deactivation procedure is implemented, which is directly controlled by activation and deactivation indications from U or IOM™ interface. State transition of the procedure depends on the reached status of the receiver (adaption and synchronization) and timing functions to watch fault conditions. Two modes can be selected for maintenance functions. All ANSI specified EOC procedure handling and executing is performed in the automode. All bits are transferred transparent to the IOM™ interface without any internal processing in the transparent mode.

The Receiver block (REC) performs the filter algorithmic functions using digital signal processing techniques. Modules for echo cancellation, pre- and post-equalization, phase adaption and frame detection are implemented in a modular multi-processor concept.

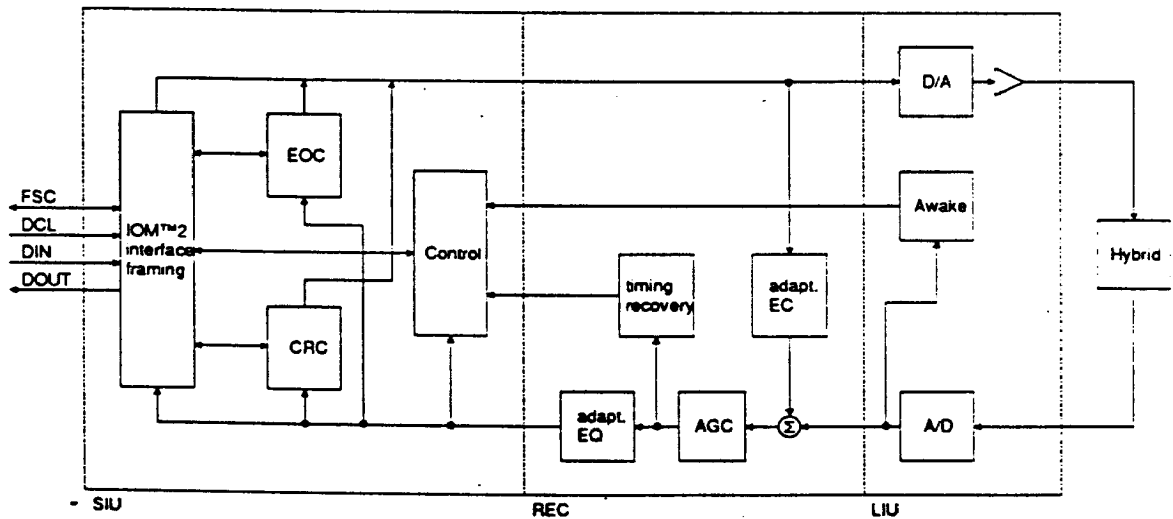
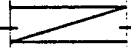


Fig. 3.1 : simplified block diagram of the IEC-Q

## 4. IEC-Q Interfaces

## 4.1 U Interface

		FRAMING	2B+D	Overhead Bits (M1-M6)						
		Quat Positions	1-9	10-117	118s	118m	119s	119m	120s	120m
		Bit Positions	1 - 18	19-234	235	236	237	238	239	240
Super Frame #	Basic Frame #	Sync Word	2B+D	M1	M2	M3	M4	M5	M6	
1	1	ISW	2B+D	eoc <sub>a1</sub>	eoc <sub>a2</sub>	eoc <sub>a3</sub>	act	act	1	1
	2	SW	2B+D	eoc <sub>dm</sub>	eoc <sub>i1</sub>	eoc <sub>i2</sub>	dea	ps1	1	febe
	3	SW	2B+D	eoc <sub>i3</sub>	eoc <sub>i4</sub>	eoc <sub>i5</sub>	1	ps2	crc <sub>1</sub>	crc <sub>2</sub>
	4	SW	2B+D	eoc <sub>i6</sub>	eoc <sub>i7</sub>	eoc <sub>i8</sub>	1	ntm	crc <sub>3</sub>	crc <sub>4</sub>
	5	SW	2B+D	eoc <sub>a1</sub>	eoc <sub>a2</sub>	eoc <sub>a3</sub>	1	cso	crc <sub>5</sub>	crc <sub>6</sub>
	6	SW	2B+D	eoc <sub>dm</sub>	eoc <sub>i1</sub>	eoc <sub>i2</sub>	1		crc <sub>7</sub>	crc <sub>8</sub>
	7	SW	2B+D	eoc <sub>i3</sub>	eoc <sub>i4</sub>	eoc <sub>i5</sub>	1		crc <sub>9</sub>	crc <sub>10</sub>
	8	SW	2B+D	eoc <sub>i6</sub>	eoc <sub>i7</sub>	eoc <sub>i8</sub>	1		crc <sub>11</sub>	crc <sub>12</sub>
2,3,....										

LT-to-NT direction  NT-to-LT direction

"1" = reserve=reserve bit for future standard; set=1  
 eoc=embedded operations channel  
 a=address bit  
 dm=data/message indicator  
 i=information (data/message)

act=activation bit  
 ps1,ps2=power status bits  
 ntm=Nt1 in Test Mode bit  
 crc=cyclic redundancy check covers 2B+D & M4  
 febe=far end block error bit  
 cso=cold start only  
 dea=deactivation

2B1Q Superframe Technique & Overhead Bit Assignments  
 (8x1.5 ms "Basic Frames"= 12 ms Superframe)

Tab. 4.1 : U frame structure

#### 4.1.1 U Interface Maintenance Channel

##### 4.1.1.1 Embedded Operation Channel (EOC)

The EOC protocol operates in a repetitive command/response mode with a triple last look and master function on the network side.

All messages are latched, i.e. they will be continually executed until an RTN (return to normal) message appears.

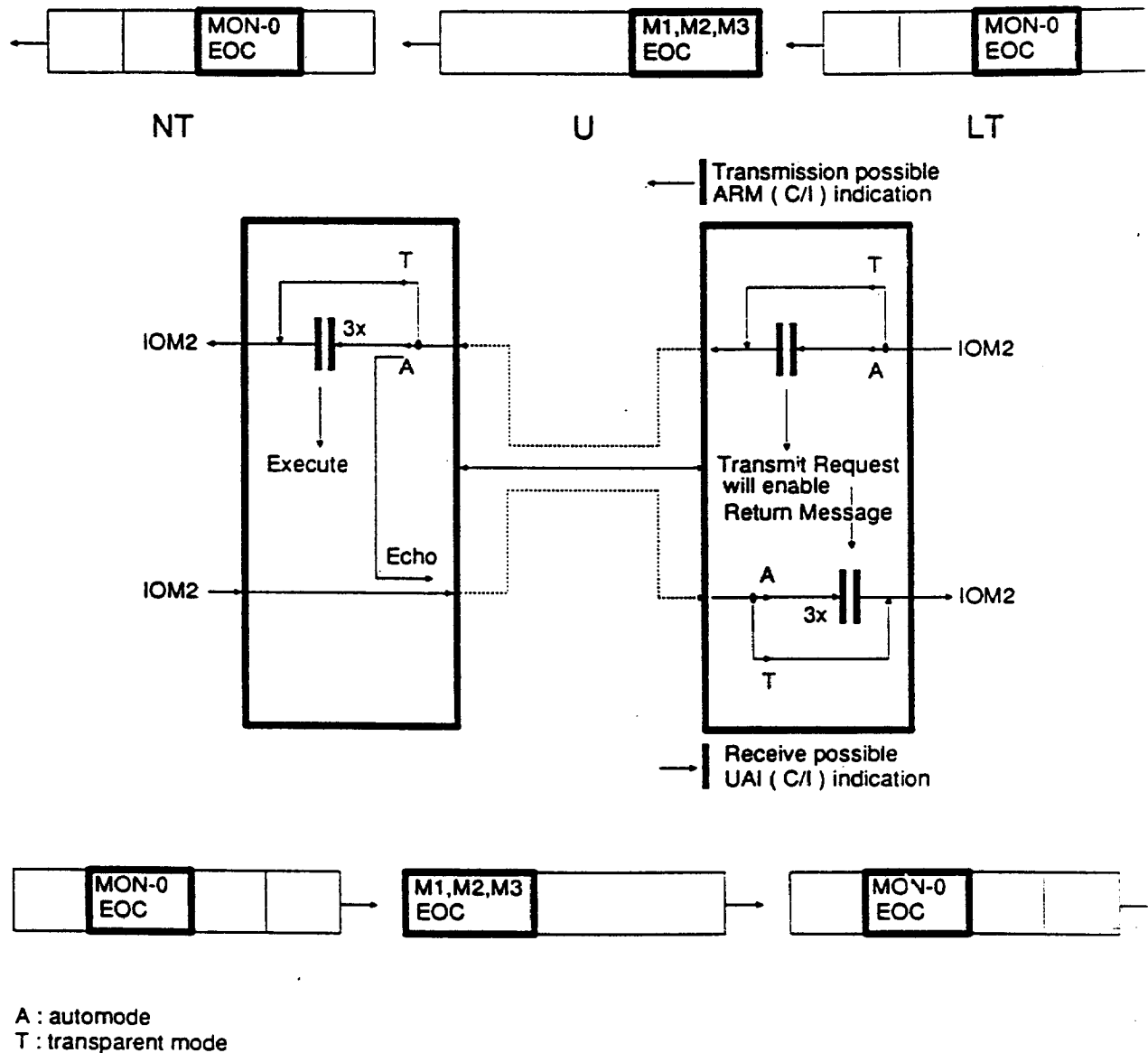


Fig. 4.1 : EOC procedure

## Frame and Functions

EOC																						
address field			data/ message indicator d/m	information								(o)rigin (d)estination		message								
a1	a2	a3		i1	i2	i3	i4	i5	i6	i7	i8	LT	NT									
0	0	0	1 0  1 1 1 1 1 1 1 1											NT address								
1	1	1												broadcast address								
														message data								
														LBBD								
														LB1								
														LB2								
														RCC								
														NCC								
														RTN								
														H								
											UTC											

Tab. 4.2 : frame and functions

RTN	Return to Normal	will release all outstanding EOC controlled operations; Reset of EOC processor to initial state.
UTC	Unable to Comply Ack	validates the receipt of an EOC message, but the EOC message is not in the menu of NT.
NCC	Notify of Corrupted CRC	
RCC	Request Corrupt CRC	
H	Hold State	
LBBD	Loopback B1, B2 and D	request within NT/SBCX.
LB1/2	Loopback Channel (B1 or B2)	request within NT/IEC-Q.

Only EOC frames with data/message indicator set to "1" (message) are able to evaluate; otherwise a UTC message will be replied.

## NT Automode

In the NT Automode configuration, every EOC message will be recognized and executed after receiving three identical consecutive EOC frames with correct NT address "000" or broadcast address "111". All received EOC frames are echoed back in the next transmitted EOC frame (0.75 ms frame delay) except:

- wrong address.  
in this case the HOLD state message with NT address will be transmitted until a correctly addressed message is received.
- message not executable.  
a UTC message is transferred back after the third non-executable identical received message.

For test purposes, all EOC frames are transmitted via the IOM™2 MONITOR channel, after the third correct reception.

**NT Transparent Mode**

For NT transparent mode, the received EOC frame will not be analyzed or executed but rather transmitted downstream to IOM™2 MONITOR channel. In the upstream direction, the last incoming EOC code from the IOM™2 MONITOR channel is used for transmission.

**LT Automode**

In the LT automode, EOC frames to be sent are taken from the IOM™2 MONITOR channel information. This will be continually transmitted until a new EOC frame is to be sent.

After POWER DOWN, RESET or during start procedure, an RTN (return to normal) message is transmitted.

Every new transmit request will enable the return message.

The return message upstream via IOM™2 is a single transmission of an accepted EOC frame.

Every EOC frame will be accepted only after first detecting 3 identical consecutive EOC frames and if the new EOC frame is different from the previously accepted one.

**LT Transparent Mode**

For LT transparent mode, the transmit procedure corresponds to the LT automode; in the receive direction, the IEC-Q is transparent to every EOC frame.

**4.1.1.2 CRC Process**

An error monitoring function is implemented covering the 2B+D and M4 data transmission of a U superframe by a Cyclic Redundancy Check (CRC).

The computed polynomial is:

$$G(u) = u^{12} + u^{11} + u^3 + u^2 + u + 1$$

(+ modulo 2 addition)

The generated check digits (CRC bits CRC1, CRC2, ..., CRC12) from the data are transmitted in the following U superframe after the data transmission (CRC1 most significant bit). The receiver will compute the CRC of the received 2B+D and M4 data and a comparison will be done with the received CRC bits generated by the transmitter.

A CRC error will be indicated to both sides of the U interface. As a NEBE (Near End Block Error) on that side where the error is detected, as a FEBE (Far End Block Error) on the opposite side.

The FEBE bit will be placed in the next available U superframe transmitted to the originator.

The IEC-Q contains two error counters clocked by the far end or near end error indication.

The maximum counter value is 255; a reset is performed either during activation of the U interface or after read-out. Both counter values can be read out via the MONITOR channel (MON-2) of the IOM™2 interface. In the NT mode, block error indications are issued additionally by a MON-1 message every time an error has occurred.

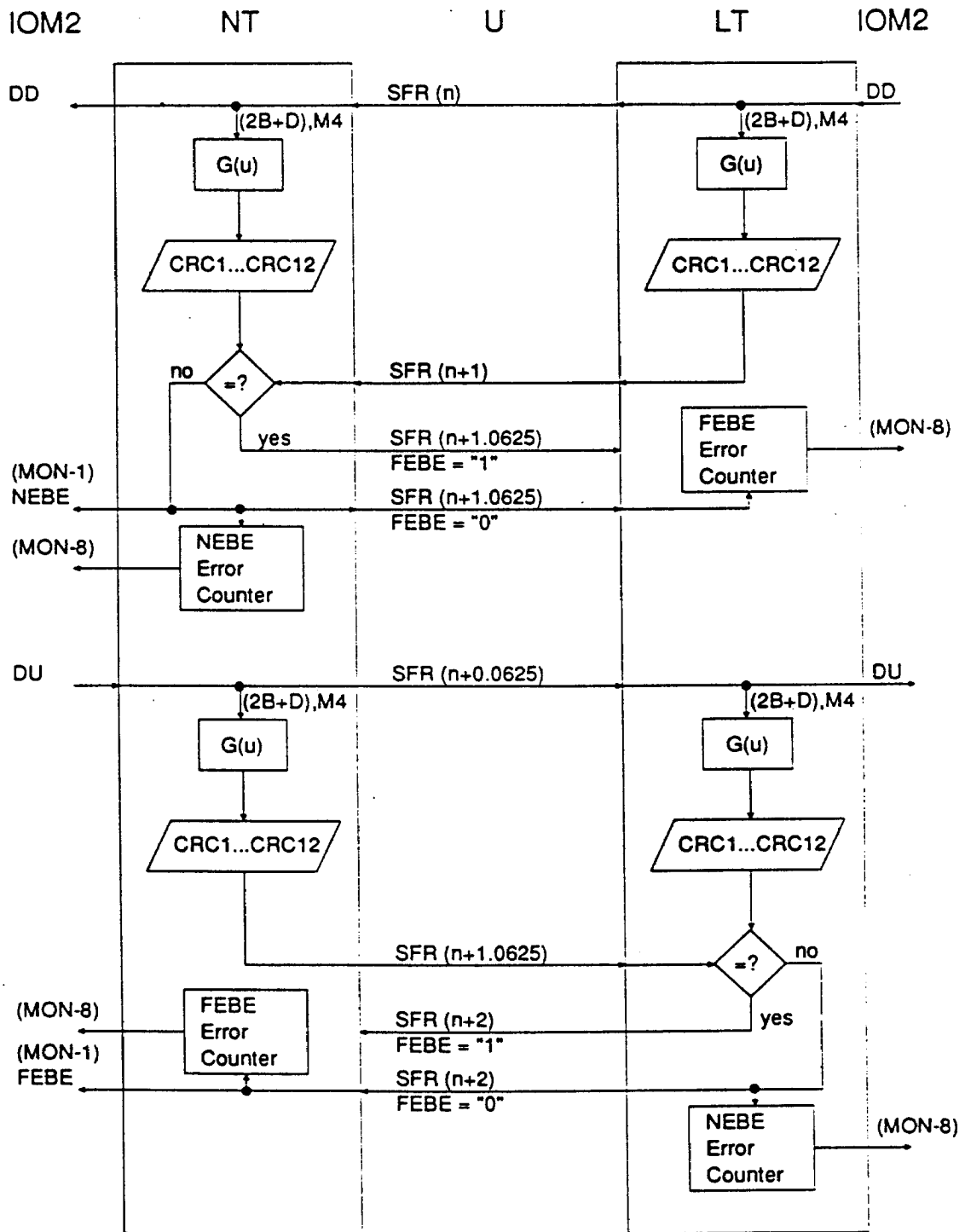


Fig. 4.2 : CRC process

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**Corrupted CRC (CCRC)**

Data fault conditions can be generated for testing of the CRC procedure by manipulating the CRC bits.

The transmission of a corrupted CRC (inverse data) can be either generated

LT Side: MON-8 command (CCRC)

NT Side: EOC command (RCC)

The "Notify of Corrupted CRC" (NCC) causes the received CRC bits to be corrupted. In both test modes the error counters in the addressed chip are stopped and error indications via IOM™2 interface are retained.

In the transparent mode the EOC messages will pass through the chip without execution. There is no suppression of error counter and error messages towards the IOM™ interface.

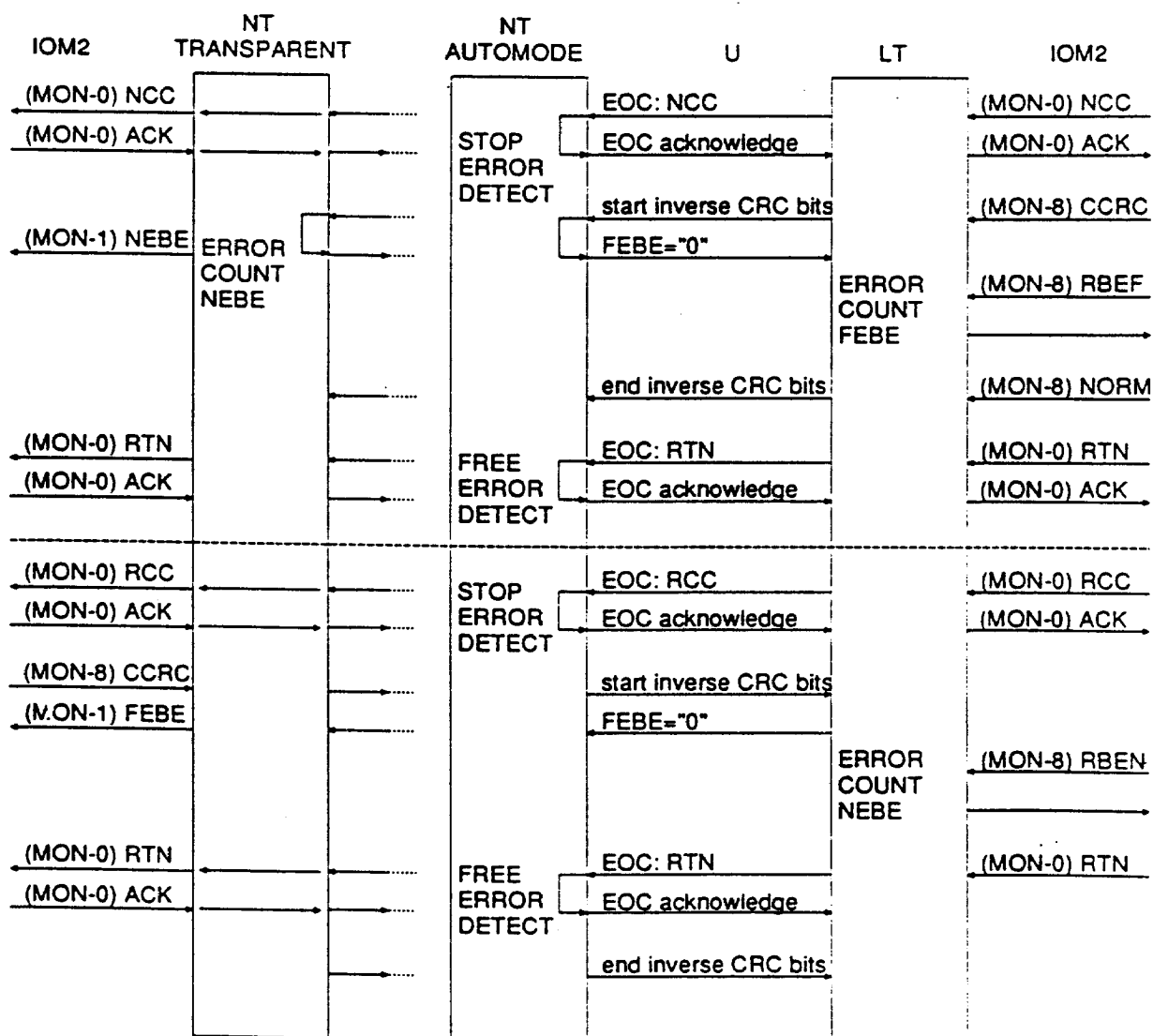


Fig. 4.3 : Corrupted CRC test

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## 4.2 IOM™2 Interface

The IOM™2 interface is viewed as a standard interface that interconnects different modules together in a terminal. The interface is synchronized by frame and data clock signals supplied by a master clock source. The definition of master or slave mode depends on whether the timing for the interface is received or supplied by the device.

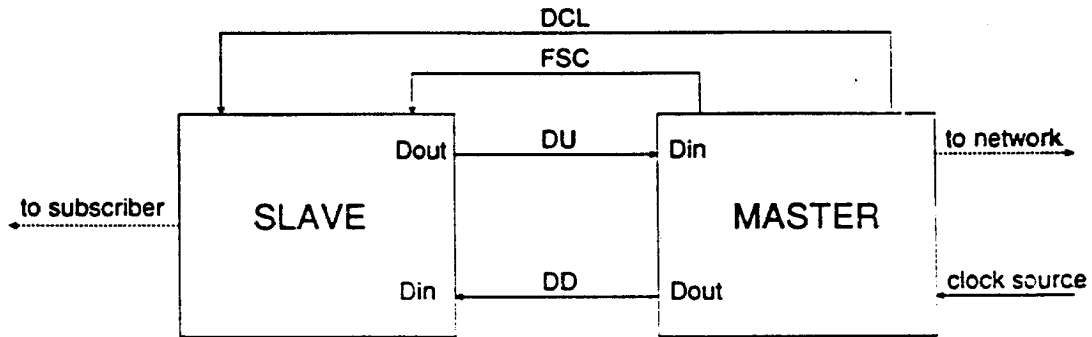


Fig. 4.4 : IOM™2 interface signals

The IOM™2 interface consists of four physical connections. Two lines for the transmission of data, one for each direction. The other two lines are for the frame and data clocks (see figure).

**DU** Data Upstream. Transmission of data from the subscriber side to the exchange side.

**DD** Data Downstream. Transmission of data from the exchange side to the subscriber side.

**DCL** Data Clock. Twice the data transmission frequency on DU and DD.

**FSC** Frame Synchronization Clock. Resets the bit counter at the start of each frame.

The downstream and upstream directions are always with respect to the exchange. From the device point of view, these connections can also be named Din and Dout, referring to the reception or transmission of data, respectively.



## The frame structure of IOM™2

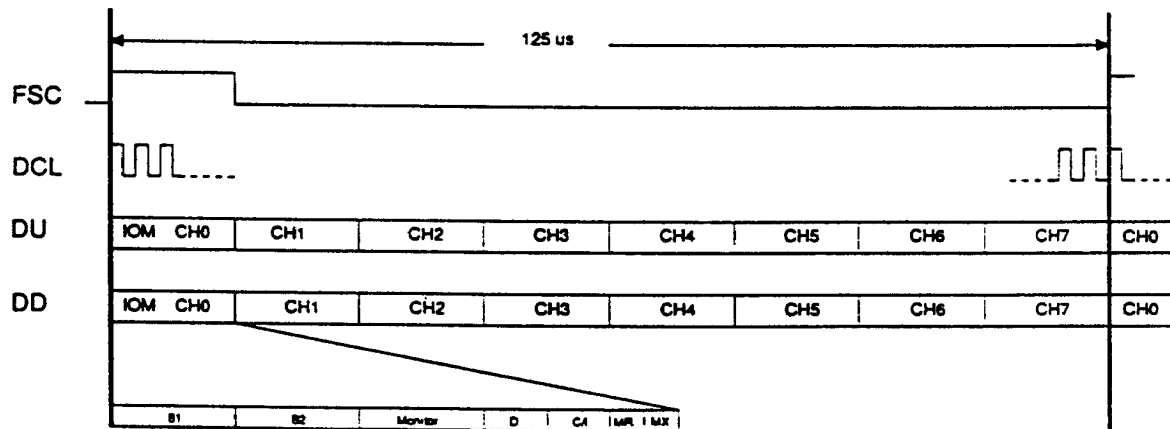
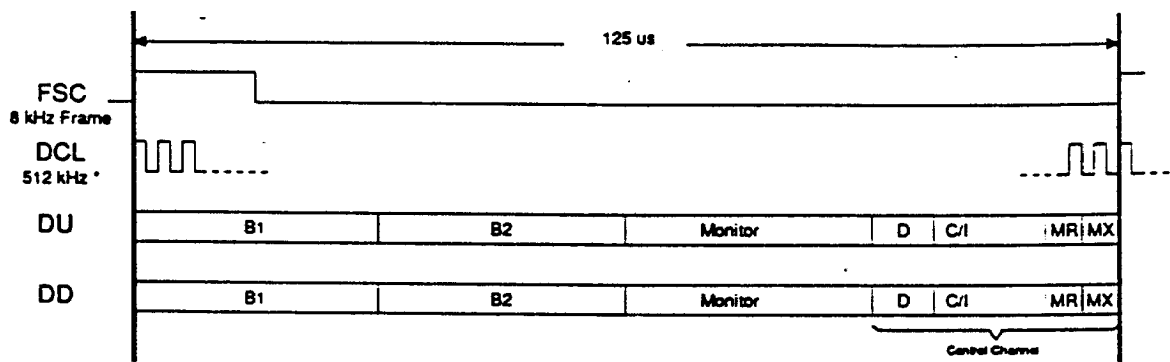


Fig. 4.5 : IOM™2 interface multiplexed frame structure (2.048 kbps)

- B1, B2: circuit switched voice/data.
- D: D channel for signaling and packet switched data.
- C/I: command/indication bits for control.
- MR, MX: monitor handshake bits

\* DCL is programmable for values from 512 kHz to 4.096 MHz.

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#### 4.2.1 IOM™2 Interface Maintenance Functions

##### 4.2.1.1 Control/Indication Channel

The Control/Indication channel (C/I channel) is used to control the operational status of the IEC-Q and to issue corresponding indications.

In general, commands (on DIN) have to be applied continuously as long as the required action is needed.

A command is validated by the IEC-Q if it has been detected in two subsequent IOM™ frames (double last look criterion).

Indications (on DOUT) are issued by the IEC-Q as long as no other indication has to be forwarded i.e. they are not strictly state-oriented.

Code	NT mode		LT mode	
	IN	OUT	IN	OUT
0000	TIM	DR	DR	-
0001	RES	-	RES	DEAC
0010	-	FJ	-	FJ
0011	-	-	LTD	HI
0100	EI1	EI1	RES1	RSY
0101	SSP	-	SSP	EI2
0110	DT	INT	DT	INT
0111	-	PU	-	UAI
1000	AR	AR	AR	AR
1001	-	-	-	ARM
1010	ARL	ARL	ARL	-
1011	-	-	-	EI3
1100	AI	AI	-	AI
1101	-	-	-	LSL
1110	-	AIL	-	-
1111	DI	DC	DC	DI

Tab. 4.3 : C/I channel codes

AI	Activation Indication.	HI	High Impedance (set by PFOFF).
AR	Activation Request.	INT	Interrupt (set by power controller).
ARL	Activation Request Local loop.	LTD	LT Disable (control of pin DISS).
ARM	Activation Request Maintenance bits.	LSL	Loss-of-Signal Level on U.
DC	Deactivation Confirmation.	UAI	U Activation Indication.
DR	Deactivation Request.	RES	Circuit Reset.
DEAC	Deactivation Accepted.	RES1	Receiver Reset.
DI	Deactivation Indication.	RSY	Loss of Synchronization.
DT	Data Through (test mode).	PU	Power Up.
EI1	Error Indication 1 (error on U).	SSP	Test mode (Send Single Pulses).
EI2	Error Indication 2 (error on S/T).	TIM	Timing required.
EI3	Error Indication 3 (timeout 15 s: error on U).	FJ	Frame Jump.

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#### 4.2.1.2 IOM™2 MONITOR Channel

The MONITOR (MON) channel is used for the transfer of messages and data related to maintenance functions. The MX and MR bits in the 4<sup>th</sup> octet of the IOM™ frame are used for flow control (active low).

##### 4.2.1.2.1 Transfer Procedure

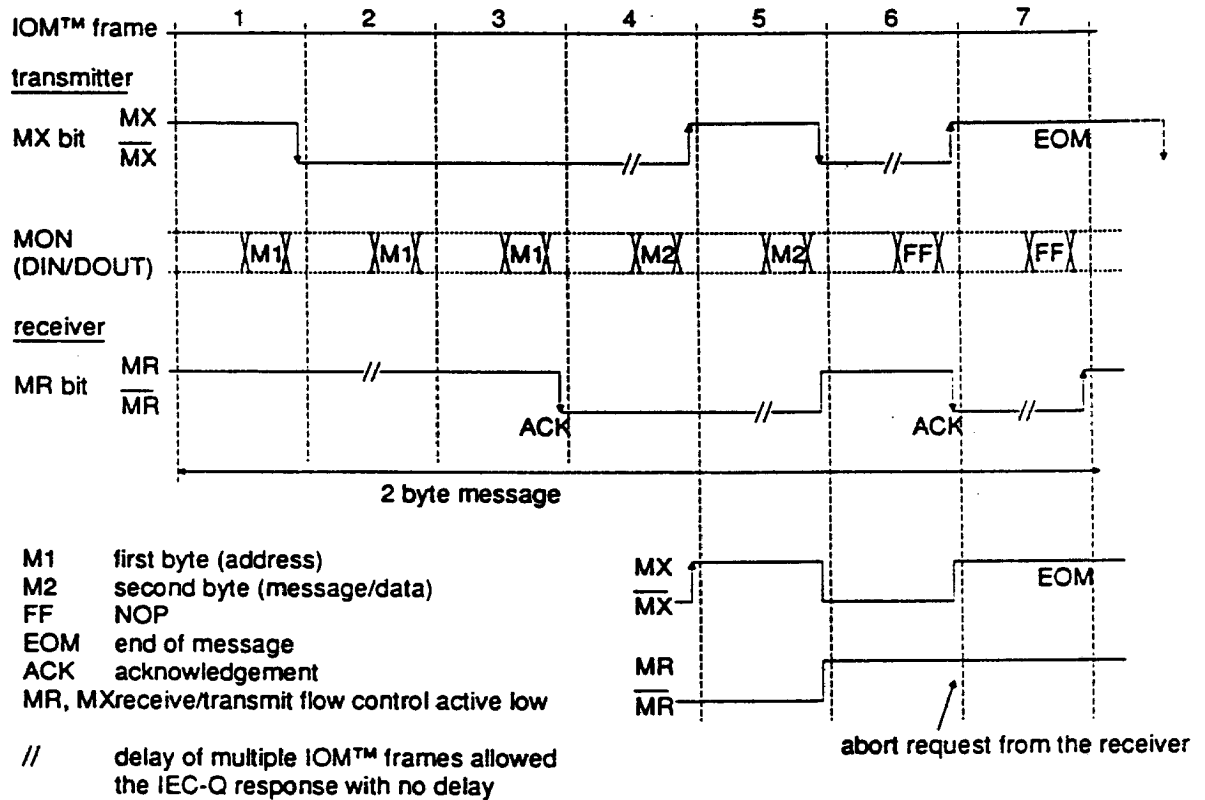


Fig. 4.6 : transfer procedure

The MON channel procedure allows a full duplex transmission. The MX bit is used to start or indicate the transmission of data on the MON channel. The receipt of data is acknowledged making use of the MR bit in the reverse direction.

The procedure allows the transmission of two-byte messages or data. The first byte contains the address and possibly data and the second byte a message or data.

The MON channel is in an idle condition when the MX bit is inactive in two or more consecutive frames. In this case, the MR bit in the reverse direction is inactive too. In the MON channel, binary "1s" are transmitted. The transmission of the first byte M1 is started by the transmitter with the transition of the MX bit from inactive to active in the same frame. This is allowed only if the MR bit in the reverse direction has been in the inactive state for at least two consecutive frames.

The receiver confirms the start of the transfer procedure by setting the MR bit active if the transmitted bytes are identical in the first two received frames. It acknowledges the receipt of byte M1 by keeping the MR bit in the active state for at least one more frame.

In the frame following the transition of the MR bit from inactive to active, the transmitter starts the transfer of the second byte M2 with the transition of the MX bit from active to inactive. The MX bit stays in the inactive state for only one frame if the receipt of byte M1 has been acknowledged by the receiver.

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In the next frame, the receiver sets the MR bit inactive and acknowledges the receipt of byte M2 by a transition of the MR bit from inactive to active one frame later.

The transmitter sets the MX bit inactive and keeps it in the inactive state for at least one more frame. The presence of the MX bit in the inactive state for two or more consecutive frames indicates the end of the message (EOM).

In the frame following the transition of the MX bit from active to inactive, the receiver sets the MR bit inactive. As it detects the EOM, it keeps the MR bit in the inactive state until a new message is received.

If the received bytes are not identical and no EOM is detected, the receiver sends no acknowledgement to the transmitter i.e. it sets the bit inactive and keeps it in this state until it has detected the response of the transmitter (MX bit inactive in at least two frames) and until a new transfer procedure is started. In general, after starting the receive procedure, the MR bit stays in the inactive state for at least two consecutive frames, the transmitter is requested to abort transmission (MX bit inactive) and to retransmit the entire message.

If an EOM is detected, the receiver sets the MR bit inactive i.e. no acknowledgement is issued and the MR bit is kept in this state until a new transfer procedure is started. The bit has to be set inactive at the latest one frame after the MX bit has been inactive two times. Furthermore, the receiver checks after the receipt of EOM if two bytes have been transferred. If this is not the case the whole message is disregarded by the receiver.

To allow the start of a new cycle of MON messages every 6 ms and to prevent a lock-up situation under failure conditions, the transmit procedure is reset to its idle state every 6 ms. If this happens when a transfer procedure is being performed, the transmitter of the IEC-Q sets the MX bit inactive two times to assure that the receiver enters the idle state too. If a transmit procedure is reset, the message is lost. To prevent this situation, the transmitter does not start a transfer procedure during a period of time corresponding to 16 IOM™ frames before the superframe indication (IOM™ frames 81..96) or 6 ms after (IOM™ frames 33..48). In this case, the receiver is requested to delay the receive procedure for not more than 4 IOM™ frames compared to the timing diagram in figure 4.6.

The receive procedure is also reset to its idle state every 6 ms. If this happens when a receive procedure is being performed, the message may be lost because the generation of an abort request can not be guaranteed. To prevent this situation, the receiver does not start a receive procedure during a period of time corresponding to 16 IOM™ frames before the superframe indication or 6 ms after. In this case the transmitter is requested to delay the transmit procedure for not more than 5 IOM™ frames compared to the timing diagram in figure 4.6.

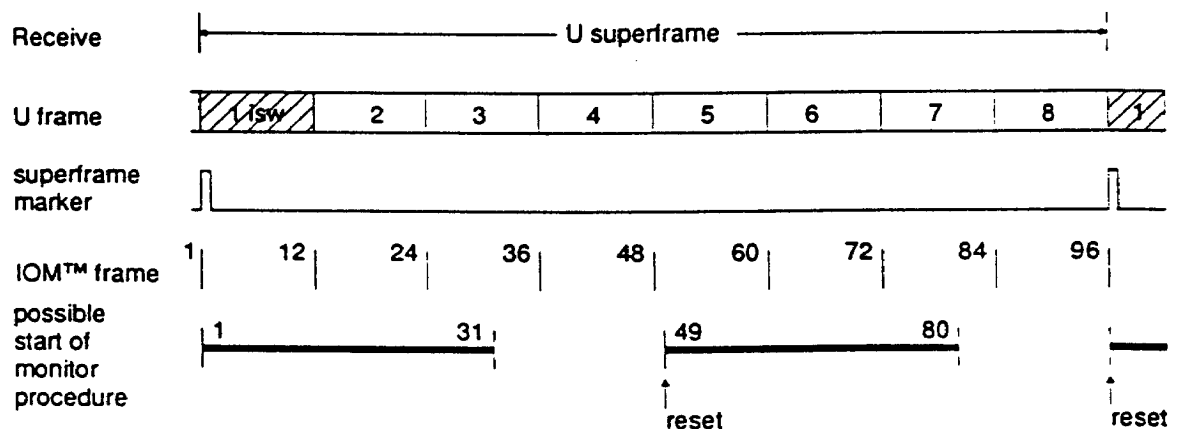


Fig. 4.7 : monitor access

#### 4.2.1.2.2 Message Structure



## MON-1

Automode and transparent mode

0 0 0 1	x x x x	s s s s	m m m m
1		S/Q code	M bits

## Notation:

U upstream (TE -> LT)  
D downstream (LT -> TE)  
x don't care

S/Q code	NT		LT	
	D	U	D	U
0000	STP FEBE NEBE FNBE	ST		
0001				
0010				
0100				
1000				
1100				
1111		NORM		

M bits				
1xx0		NTM		
1111		NORM		

## Messages:

FEBE far end block error.  
FNBE far and near end block error.  
NEBE near end block error.  
NORM return to normal.  
NTM NT test mode.  
ST self test request NT.  
STP self test pass.

The MON-1 structure applies to the NT mode only and is used for indications corresponding to specific bits in the maintenance channel of the U interface and for S/Q channel related messages.

Indications related to the Q channel issued by the SBCX are transferred over the MON channel every time a change has been detected in the Q channel (latching). Block error indications (FEBE, NEBE and FNBE) are issued by the IEC-Q every time an error has occurred (non-latching); the response to a self-test request (STP) is non-latching too.

All indications received by the IEC-Q during one superframe (12 ms) are passed over the MON channel in one block making use of one 2-byte message.

Note: Indications issued by the SBCX may be received with a different timing i.e. every 5 ms for instance.

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**MON-2**

Automode and transparent mode

0 0 1 0	$d_{11}d_{10}d_9d_8$	$d_7d_6d_5d_4d_3d_2d_1d_0$
2	M bits	M bits

The MON-2 structure is used in both NT and the LT modes to transfer all the overhead bits except EOC and CRC. This corresponds to 12 bits passed in the same order as defined on the U interface and starting (first bit after the address bit) with the act bit:

U Super-frame position	NT -> LT		LT -> NT		
	position	control	position	control	
M41	act	IEC-Q	act	IEC-Q	$d_{11}$
M51	1	MON-2	1	MON-2	$d_{10}$
M61	1	MON-2	1	MON-2	$d_9$
M42	ps1	pin	dea	IEC-Q	$d_8$
M52	1	MON-2	1	MON-2	$d_7$
M62	febe	IEC-Q	febe	IEC-Q	$d_6$
M43	ps2	pin	1	MON-2	$d_5$
M44	ntm	MON-1	1	MON-2	$d_4$
M45	cso	IEC-Q*	1	MON-2	$d_3$
M46	1	MON-2	1	MON-2	$d_2$
M47	1	MON-2	1	MON-2	$d_1$
M48	1	MON-2	1	MON-2	$d_0$

note: \* : set to "0"

Mxy : Mx in frame y

In the transmit direction (on DIN), only the undefined bits marked with binary "1" may be controlled by making use of a MON-2 message. They are set to binary "1" after leaving a Power Down state. The transfer mode is latched i.e. the U bit transmits a given bit polarity as long as it is not changed by a new MON-2 message. No further processing is performed by the IEC-Q.

The bits act, dea, febe and cso are always controlled by the IEC-Q itself. The ntm bit is controlled by the S chip making use of a MON-1 message. The bits ps1 and ps2 are defined by pins.

In the receive direction (on DOUT), a MON-2 message defining all 12 bits is issued every time a change on at least one bit has been detected but not more often than once per superframe (12 ms interval). This is valid for all bits except the febe bit. In the LT mode, single block errors are not indicated autonomously, but may be read by making use of a local command (RBEN, RBEF). In the NT mode, single block errors are indicated by making use of a MON-1 message.

## MON-8

Automode and transparent mode

1 0 0 0	r 0 0 0	c c c c c c c c
8	reg.ad.	local command/ message/data

Notation:

U upstream (TE -> LT)  
D downstream (LT -> TE)  
1 binary 1  
0 binary 0  
a...a address controller interface to pin PCA  
d...d data controller interface to pin PCD

r	code c	NT		LT	
		D	U	D	U
0	1111 0000		CCRC 1)	CCRC	
0	1111 0100		LB1 1)		
0	1111 0010		LB2 1)		
0	1111 0001		LBB D 3)		
0	1111 1111		NORM 1)	NORM	
0	1111 1011		RBEN	RBEN	
0	1111 1010		RBEF	RBEF	
0	1111 1000			RPFC	
0	011d ddaa		WCI 2)	WCI 2)	
0	010* *aa		RCI 2)	RCI 2)	
0	ddd* ....	ACI 2)			ACI 2)
0	0000 0000		RID	RID	
	.... ....	AID			AID

Note:

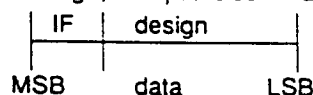
- 1) These codes are only used in the transparent mode.
- 2) see controller interface description.
- 3) This code is used in the transparent mode or after receipt of EOC (LBB D) command.

Commands:

CCRC corrupt crc  
LB1 loopback channel B1 request (within NT/IEC-Q)  
LB2 loopback channel B2 request (within NT/IEC-Q)  
LBB D loopback B1, B2 and D channel request (within NT/IEC-Q)  
NORM return to normal  
RBEF read far end block error counter  
RBEN read near end block error counter  
WCI write controller interface  
RCI read controller interface  
ACI answer controller interface  
RID read identification  
RPFC read power feed current value

The MON-8 structure is used for local functions.

Commands (on DIN) concerning loopback and CRC may be passed at any time and need to be transferred only once. They are latched, i.e. they are valid as long as they are not disabled explicitly by a "NORM" message, except the commands requesting the transfer of internal data which are non-latching



IF = "00" (U interface)  
design = "000000" (Siemens design)

AID Answer identification

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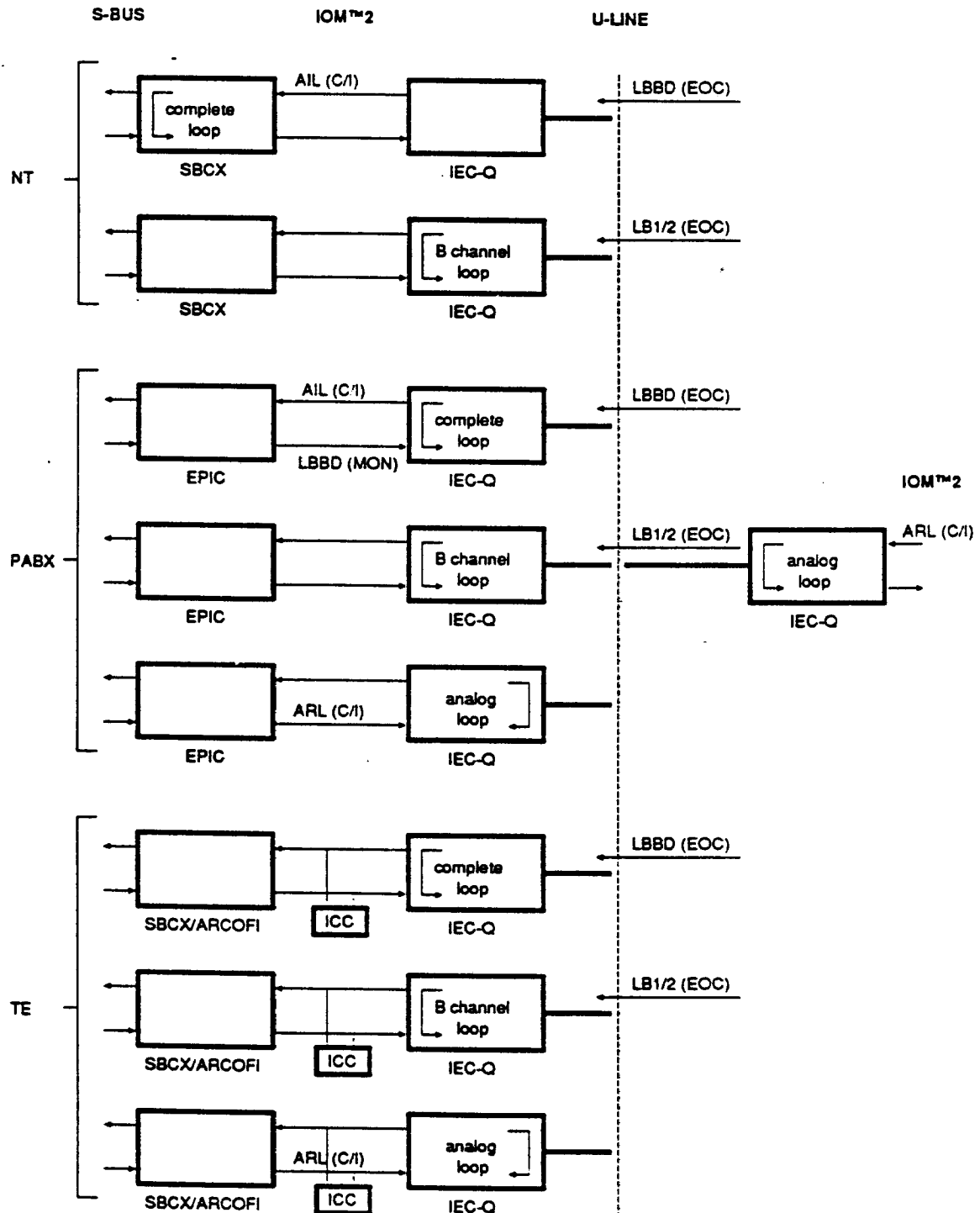


Fig. 4.8 : test loops closed by the IEC-Q or under its remote control

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### 4.3 Test Loops

For the test of the line cards, several test loops are provided which can be controlled from the exchange. In the complete loop, all channels (2B+D) shall be transmitted back towards the transmitting station without modification. The data from the other end of the line is ignored. There are separate loops for single channels called individual B channel loopbacks. The individual B channel loopback can provide per-channel maintenance capabilities without totally disrupting service to the customer. All loops are transparent loops; that means all bits toward the loop are passed onward as well as looped back. Nevertheless, the NT receives this signal and synchronizes on it.

#### Switching an Analog Loop in the IEC-Q

The analog loop is closed in the IEC-Q as near to the U interface as possible. Using internal switches, the signal from the line driver is fed back to the input of the ADC with an attenuation of approx. 12 dB. The line driver is still connected to the output pins and transmitting data. The input signal from the hybrid is ignored in this mode.

The analog loop mode is controlled via the IOM™2 C/I channel.

In an analog loop, the transmit path is set to the LT mode and the receive path is set to the NT mode independently of the polarity of the LT pin.

#### Switching the complete loop and the individual B channel loopback

The individual B channel loopbacks are always closed in the IEC-Q. The complete loop can be closed in the IEC-Q NT-PABX and NT-TE modes. With internal switches, the corresponding user data at DOUT (2B+D or B1 or B2) are directly fed back into DIN. The control input (Monitor- and C/I channel as well as MX and MR bit) is still read from the IOM™2 interface. Although these loops are closed by command from the exchange, the IEC-Q can still be deactivated by RES and SSP C/I channel commands from the layer 2 device.

In the NT, the activation of an analog loop leads to the deactivation of all services initiated by the exchange. While the analog loop is activated, the NT is not available for services i.e. a complete or an individual B channel loopback can't be closed and a required CCRC shall not be carried out.

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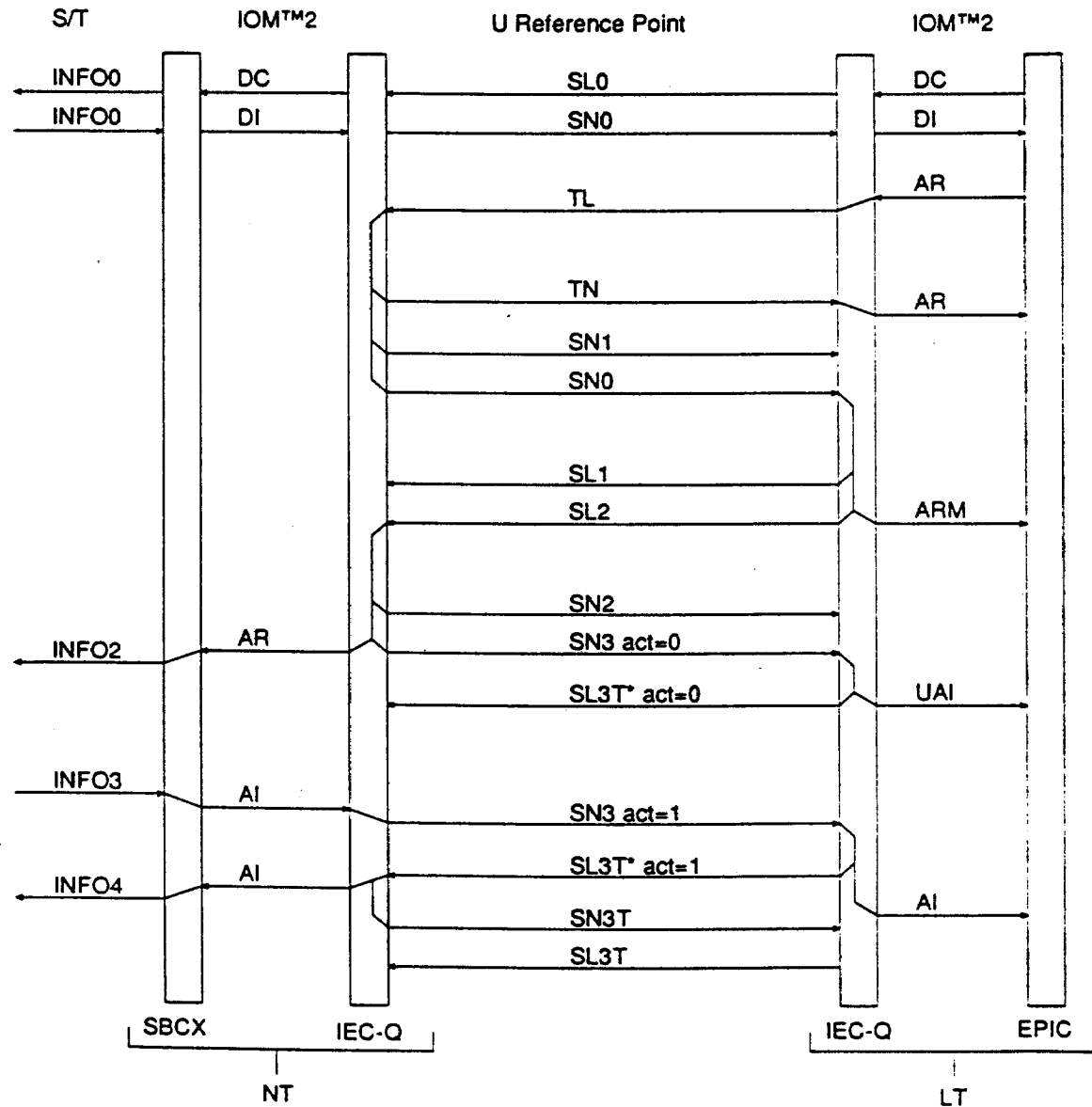
note: for transparent mode operation the EOC loop request is performed over the IOM<sup>TM</sup>2 interface NT upstream by MON-8 message.

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## 5. Activation and Deactivation Procedures

Activation can be initiated by either the LT or the NT side.

Deactivation is always initiated from the LT side.



\*) note: SL3 is generated by exchange at this time

Fig. 5.1 : Activation from LT

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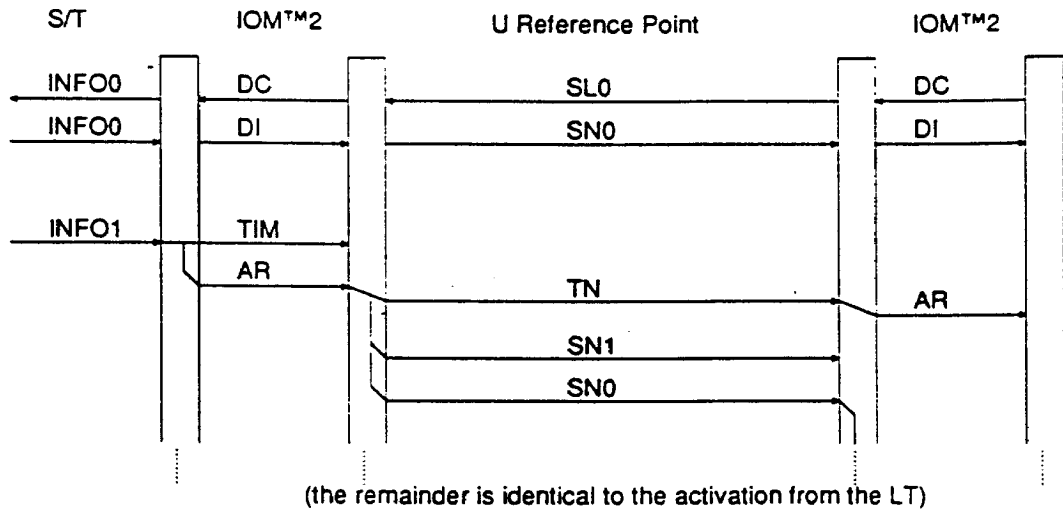


Fig. 5.2 : Activation from NT

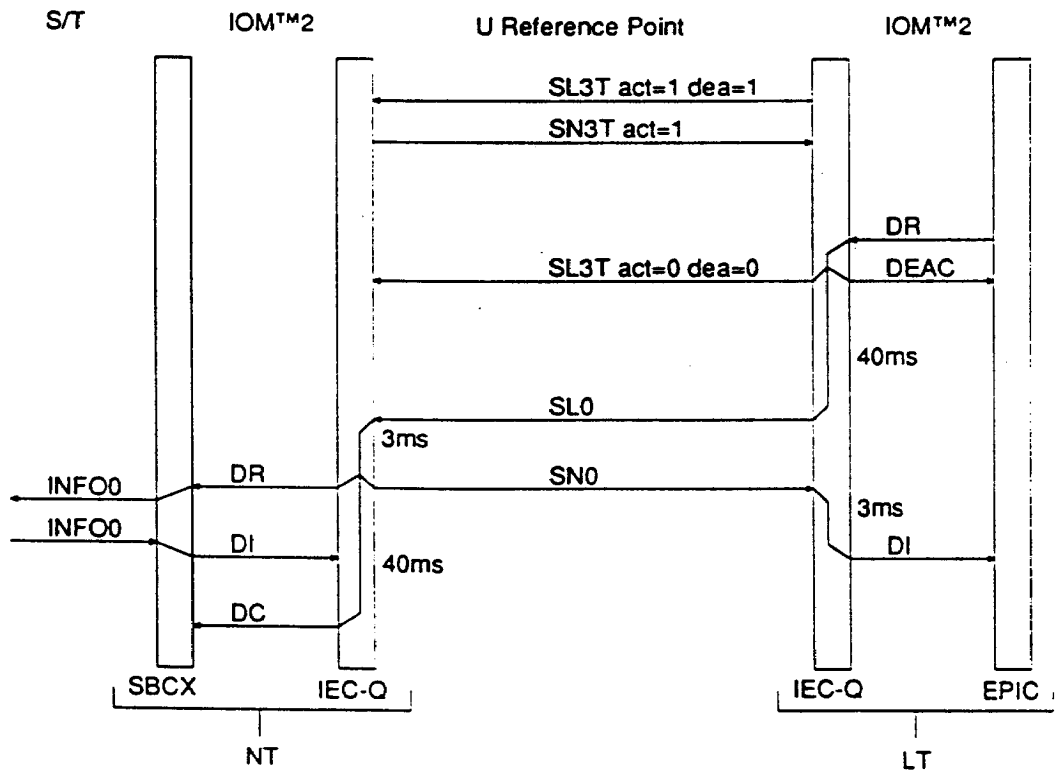


Fig. 5.3 : Deactivation procedure

signal	synch word (SW)	super frame (ISW)	2B+D	M
TN	+ - 3	+ - 3	+ - 3	+ - 3
SN0	no signal	no signal	no signal	no signal
SN1	present	absent	1	1
SN2	present	absent	1	1
SN3	present	present	1	normal
SN3T	present	present	normal	normal
TL	+ - 3	+ - 3	+ - 3	+ - 3
SL0	no signal	no signal	no signal	no signal
SL1	present	absent	1	1
SL2	present	present	0	normal
SL3*)	present	present	0	normal
SL3T	present	present	normal	normal

\*) SL3 must be generated by exchange

TL/TN alternate  $\pm 3$  for 10 kHz tone.

SNx signal from NT to LT.

SLx signal from LT to NT.

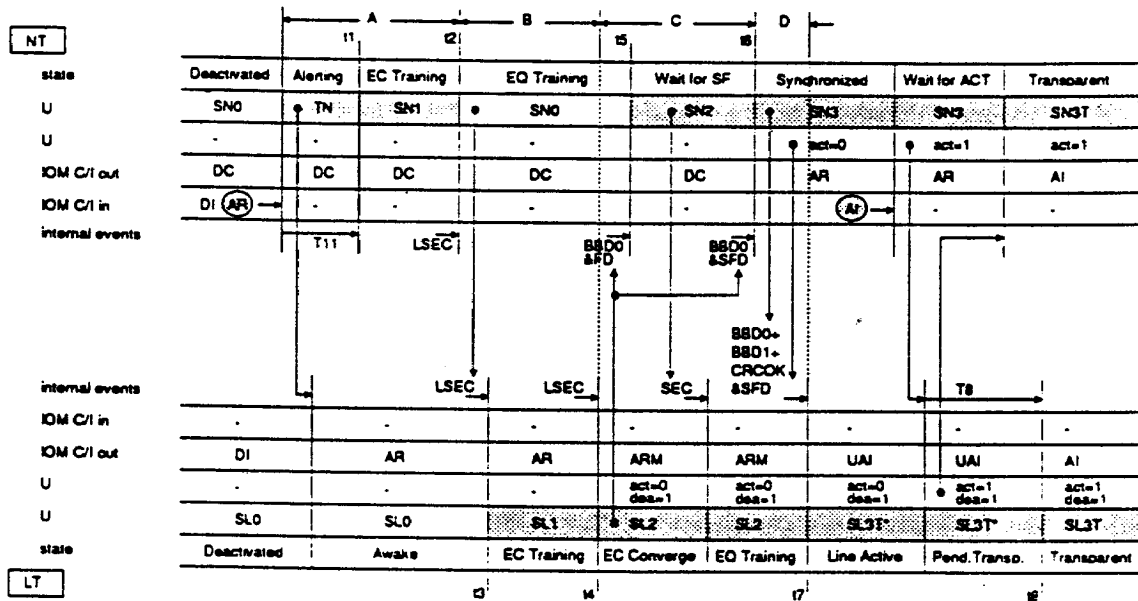


Fig. 5.4 : activation from NT

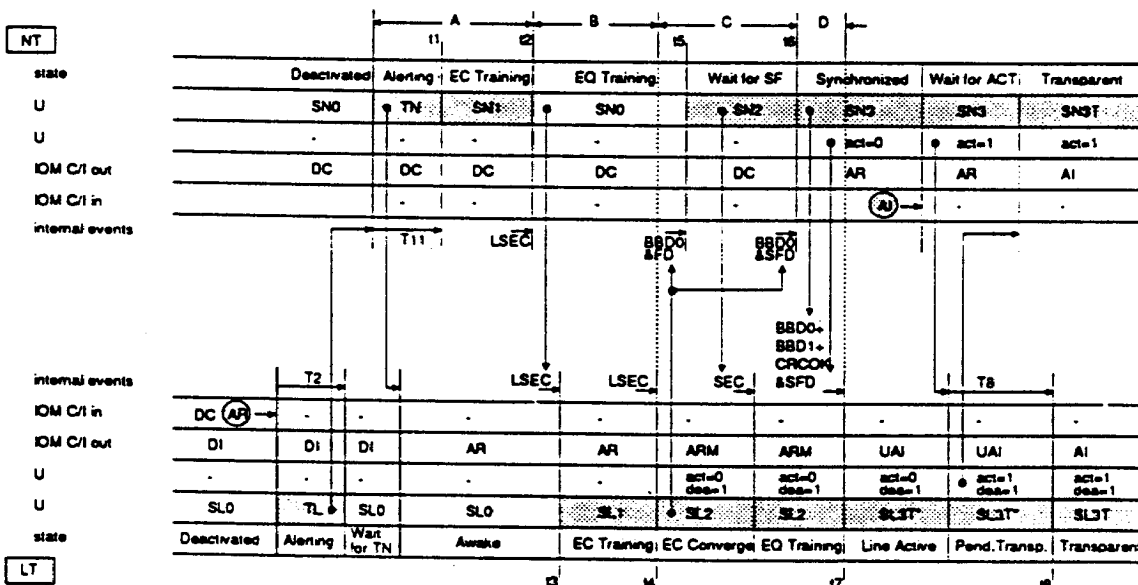


Fig. 5.5 : activation from LT

$$t2 - t3 \leq 480 \text{ ms}$$

$$A + C \leq 5 \text{ s cold start}$$

$$A + C \leq 150 \text{ ms warm start}$$

$$B + D \leq 10 \text{ s cold start}$$

$$B + D \leq 150 \text{ ms warm start}$$

2

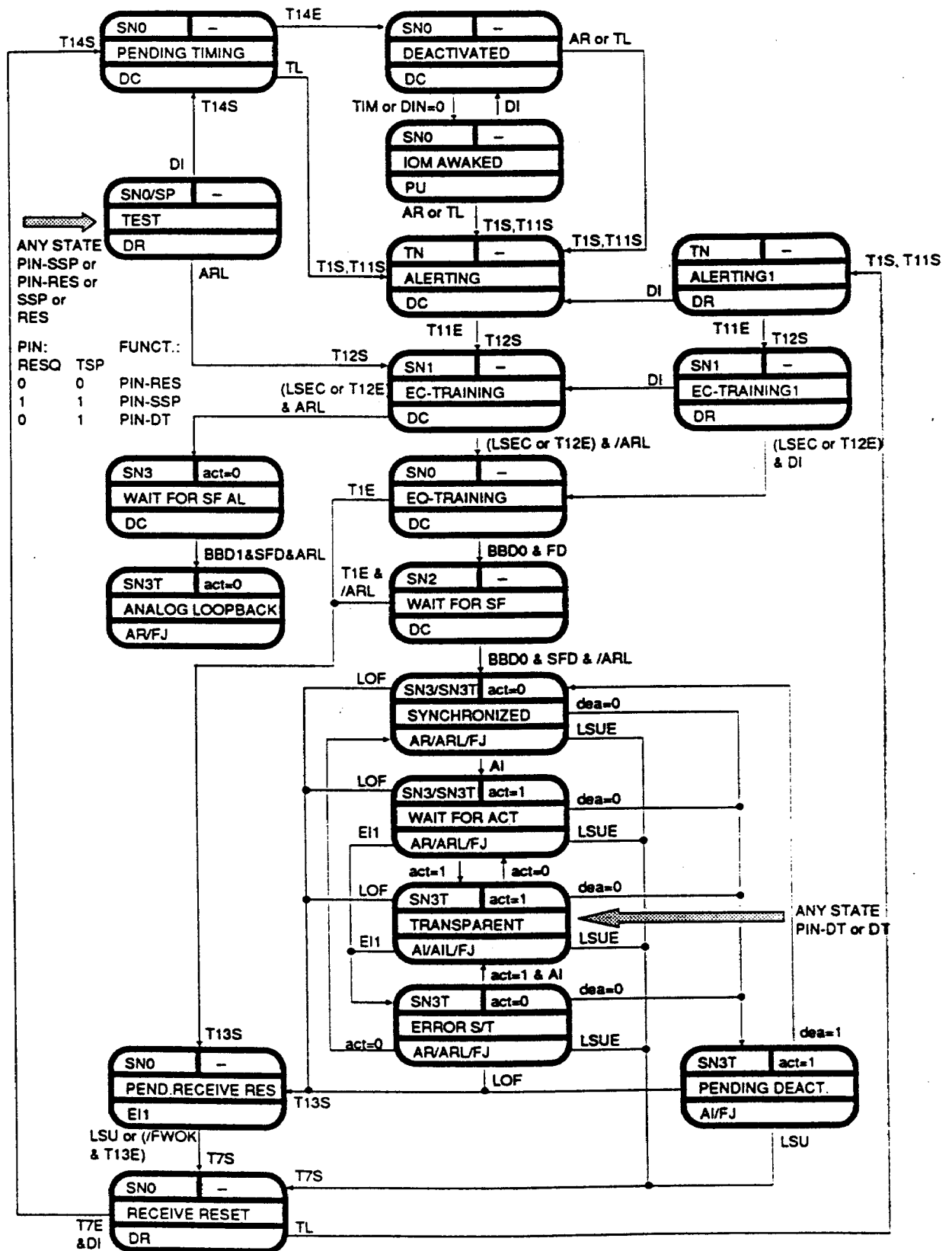
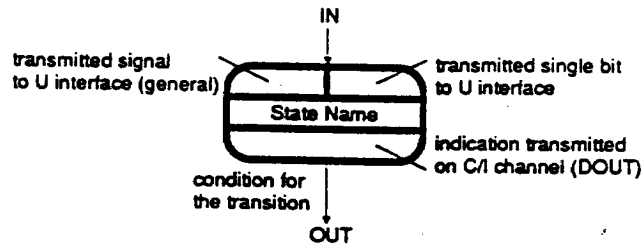


Fig. 5.6 : state transition diagram NT, NT-PABX modes



## Explanation for NT State Diagram



The following commands or events are used for the transition:

1.) C/I channel (on DIN)

AI Activation Indication

The SBCX issues this indication to announce that the receiver is synchronized:  
The IEC-Q informs the network side by setting the act bit to "1".

AR Activation Request

INFO1 has been received by the SBCX (NT mode only, not relevant in NT-PABX mode) and the IEC-Q is requested to start the activation process by sending the wake-up signal TN.

ARL Activation Request Local Loopback

The IEC-Q is requested to operate an analog loopback (close to the U interface) and to begin the start-up sequence by sending SN1 (without starting timer T1).  
This command may be issued only after the IEC-Q has been reset by making use of the C/I channel code RES or the pin reset RESQ. This assures that the EC and EQ coefficient-updating algorithms converge correctly.  
The ARL command has to be issued continuously as long as the loopback is required.

DI Deactivation Indication

This indication is used during a deactivation procedure to inform the IEC-Q that timing signals are not needed any more and that the IEC-Q may enter the deactivated (power-down) state. The DI indication has to be issued by the SBCX continuously until the IEC-Q has answered with the DC code.

DIN=0 Binary "0" polarity on DIN

In the NT mode, this asynchronous signal requests the IEC-Q when staying in the deactivated state to enter the power-up state and to provide timing signals on the IOM™ interface. Hereafter, binary "0s" in the C/I channel (code TIM "0000" or any other code different from DI "1111" maintain the IOM™ interface activated.

DT Data Through

This unconditional command is used for test purposes only and forces the IEC-Q into a state equivalent to the transparent state. The far-end transceiver is assumed to be in the same condition.

EI1 Error Indication 1

The SBCX indicates an error condition on its receive side (loss of frame alignment or loss of incoming signal).  
The IEC-Q informs the network side by setting the act bit to "0" thus indicating that transparency has been lost.

RES Reset

Unconditional command which resets the whole chip; especially the EC and EQ coefficients are set to zero.  
For cold start, the reset code should be applied for a period of time of at least 8 IOM™ frames (1 ms).

**SSP Send Single Pulses**

Unconditional command which requests the transmission of single pulses on the U interface.

**TIM Timing**

In the NT mode the IEC-Q is requested to continue providing timing signals and not to leave the power up-state.

In the NT-PABX mode the IEC-Q is requested to enter the power-up state or not to leave it.

**2.) Pins**

**Pin-Res** Pin-Reset; corresponds to pin RESQ.

The functionality of this pin is the same as for the C/I code RES.

**Pin-SSP** Pin-Send Single Pulses; corresponds to pin TSP.

The functionality of this pin is the same as for the C/I code SSP.

**Pin-DT** Pin-Data Through; this function is activated when both pins RESQ and TSP are active (RESQ="0" and TSP="1").

The functionality is the same as for the C/I code DT.

**3.) Events related to the U Interface**

**act=0/1** act bit received from network side.

- act=1 requests the IEC-Q to achieve transparency of the transmission in both directions. As transparency in receive direction (U interface to IOM™) is already performed when the receiver is synchronized, the receipt of act=1 establishes transparency in transmit direction (IOM™ to U interface) too.

In the case of loopbacks however, transparency in both directions of transmission is performed when the receiver is synchronized.

-act=0 indicates that the network side has lost transparency.

**dea=0/1** dea bit received from the network side.

- dea=0 informs the IEC-Q that a deactivation procedure has been started by the network side.

- dea=1 reflects the case when dea=0 was detected by mistake due to for instance transmission errors and allows the IEC-Q to recover from this situation.

**LOF** Loss of Framing on the U interface (576 msec).

**LSEC** Loss of Signal level behind the Echo Canceler.

Internal signal which indicates that the echo canceler has converged.

**LSU** Loss of Signal level on the U interface.

This signal indicates that a loss of signal level of a duration of 3 ms has been detected on the U interface. This short response time is relevant in all cases where the NT waits for a response (no signal level) from the network side i.e. after a deactivation has been announced (receipt of dea=0), after the NT has lost framing and after timer T1 has elapsed.

**LSUE** Loss of Signal level on the U interface (Error condition).

This signal indicates that a loss of signal level of a duration of 588 ms has been detected on the U interface. This long response time (see also LSU) is valid in all cases where the NT is not prepared to lose signal level i.e. the LT has stopped transmission because of loss of framing, an unsuccessful activation or the transmission line is interrupted.

**SFD** Superframe Detected.

**FD** Frame Detected.

**TL** Tone (wake-up signal) received from the LT.

The IEC-Q is requested to start the activation process.

**BBD0/1** Binary "0s" or "1s" detected in the B and D channels.  
 This internal signal indicates that for a period of time of 6-12 ms, a continuous stream of binary "0s" or "1s" (analog loopback) has been detected. It is used as a criterion for receiver synchronization (SL2 from the network side or SN3 in the case of an analog loopback detected correctly).

#### 4.) Timers

The start of timers is indicated by TxS, the expiration by TxE.

The following timers are used:

	(ms)		(state)
T1	15000	activation control	
T11	9	TN transmit	alerting
T12	5500	supervisor EC converge	EC training
T13	15000	frame synchronization	pending receive reset
T7	40	hold time	receive reset
T14	0.5	hold time	pending timing

The following indications or signals are transmitted:

#### 1.) C/I channel (on DOUT)

- AI** Activation Indication  
 The IEC-Q has established transparency of transmission in the direction IOM™ to U interface.  
 In the NT mode, the SBCX is requested to send INFO4 and to achieve transparency of transmission in the direction IOM™ to S/T interface.  
 In the NT-PABX mode, the AI code signals that the IEC-Q is "ready for sending".
- AIL** Activation Indication Loopback  
 The IEC-Q has detected act=1 while loopback 2 is still established.  
 In the NT mode, the SBCX is requested to send INFO4 (if a transparent loopback 2 is to be implemented) and to keep loopback 2 established.  
 In the NT-PABX mode, the AIL code indicates that act=1 has been detected and that loopback 2 is still established within the IEC-Q.
- AR** Activation Request  
 The U receiver has synchronized on the incoming signal.  
 In the NT mode, the SBCX is requested to start the activation procedure on the S/T interface by sending INFO2.  
 In the NT-PABX mode, the AR code on DOUT has to be answered by the AI code on DIN.
- ARL** Activation Request Loopback  
 The IEC-Q has detected a loopback 2 command in the EOC channel and has established transparency of transmission in the direction IOM™ to U interface.  
 In the NT mode, the SBCX is requested to send INFO 2 (if a transparent loopback 2 is to be implemented) and to operate loopback 2.  
 In the NT-PABX mode, the ARL code indicates that loopback 2 is in operation within the IEC-Q.
- DC** Deactivation Confirmation  
 Idle code on the IOM™ interface. Normally the IEC-Q stays in the power-down mode, but an activation procedure may have been started from the network side as well.

**DR DeactivationRequest**

The IEC-Q has detected a deactivation request command from the network side or stays in a test mode.

In the NT mode, the SBCX is requested to start the deactivation procedure on the S/T interface by sending INFO0.

In the NT-PABX mode, the DR code on DOUT has to be answered by the DI code on DIN.

**EI1 Error Indication 1**

The IEC-Q has entered a failure condition (loss of framing on the U interface or expiration of timer T1).

**FJ Frame Jump**

This indication is relevant only in the NT-PABX mode and signals that either a data buffer overflow/underflow has been detected or a phase jump of one of the IOM™ timing signals DCL or FSC has occurred.

The FJ code is issued for a period of 1.5 ms.

**2.) Signals transmitted on the U Interface**

The signals SNx, TN and SP transmitted on the U interface are defined in section 5.

The following states are used:

**Alerting**

The wake-up signal TN is transmitted for a period of T11 either in response to a received wake-up signal TL or to start an activation procedure on the network side.

**Alerting IOM Awaked**

This state is entered when a wake-up tone was received in the receive reset state and the deactivation procedure on the user side was not yet finished.

The transmission of wake-up tone TN is started.

**Analog Loopback**

Upon detection of binary "1s" for a period of 6-12 ms and of the superframe indication, the analog loopback state is entered and transparency is achieved in both directions of transmission. This state can be left making use of any unconditional command. However, only the C/I channel code RES or pin RESQ only should be used. This assures that the EC and EQ coefficients are set to zero and that for a subsequent normal activation procedure the receiver updating algorithms converge correctly.

**Deactivated (full reset)**

This state corresponds to the power-down or low power consumption mode i.e. no timing signals are delivered on the IOM™ interface and no signal is sent on the U interface.

The IEC-Q waits for a wake-up signal TL from the network side or a wake-up signal (DIN=0) from the user side to start an activation procedure.

In the NT-PABX mode (where timing signals are delivered from the PABX side) the C/I channel codes AR and TIM are valid too.

**EC Training**

The signal SN1 is transmitted on the U interface to allow the NT receiver to update the EC coefficients. The automatic gain control (AGC), the timing recovery and the EQ updating algorithm are disabled. The EC training state is left when the EC has converged (LSEC) or when timer T12 has elapsed.

**EC Training 1**

This state is entered if the transmission of signal SN1 has to be started and the deactivation procedure on the user side is not yet finished.

**EQ Training**

The receiver waits for signal SL1 or SL2 to be able to update the AGC, to recover the timing phase, to detect the synchword (SWD) and to update the EQ coefficients.

The EQ training state is left upon detection of binary "0s" in the B and D channels for a period of 6-12 ms corresponding to the detection of SL2.

**Error S/T**

Loss of framing or loss of incoming signal has been detected on the S/T interface (EI1).  
The network side is informed by setting the act bit to "0" (loss of transparency on the user side).  
The following codes are issued on the C/I channel:

- normal activation or single channel loopback: AR
- loopback 2: ARL

**IOM Awaked**

Timing signals are delivered on the IOM™ interface. The IEC-Q enters the deactivated state again upon detection of the C/I channel code DI (idle code).

**Pending Deactivation**

The IEC-Q waits for the receive signal level to be turned off (LSU) to enter the receiver reset state and start the deactivation procedure.

**Pending Receive Reset**

This state is entered upon detection of loss of framing on the U interface or expiration of timer T1. This failure condition is signalled to the network side by turning off the transmit level (SN0). The IEC-Q then waits for a response (no signal level LSU) from the network side to enter the receive reset state.

**Pending Timing**

In the NT mode this state assures that the C/I channel code DC is issued four times before the timing signals on the IOM™ interface are turned off.

**ReceiveReset**

This state is entered upon detection of a deactivation request from the network side, after a failure condition on the U interface (loss of signal level LSUE) or through the pending reset state upon expiration of timer T1 or loss of framing.

No signal is transmitted on the U interface, especially no wake-up signal TN, and the SBCX is requested to start the deactivation procedure on the user side (DR).

Timer T7 assures that no activation procedure is started from the user side for a minimum period of time of T7.

The state is left only after completion of the deactivation procedure on the user side (receipt of the C/I channel code DI), unless a wake-up tone is received from the network side.

**Synchronized**

When the IEC-Q has reached this state, it informs the network side by sending the superframe indication (inverted synchword) and the user side by issuing the C/I channel codes AR or ARL. The loopback commands decoded by the EOC processor control the output of indications and transmit signals:

- normal activation SN3 and AR
- single channel loopback: SN3T and AR
- loopback 2: SN3T and ARL

The IEC-Q waits for the receipt of the C/I channel code AI to enter the wait for act state.

**Test**

This testmode is entered when the unconditional commands RES, SSP, Pin-RES or Pin-SSP are used. It is left when both pins RESQ and TSP are inactive and the C/I channel codes DI or ARL are received.

The following signals are transmitted on the U interface:

- no signal level (SN0) when the C/I channel code RES is applied or pin RESQ is activated.
- single pulses (SP) when the C/I channel code SSP is applied or pin TSP is activated.

**Transparent**

This state is entered upon the detection of act=1 received from the network side and corresponds to the fully active state. In the case of a normal activation in both directions of transmission.

The user side is informed by the following codes:

- normal activation or single channel loopback: AI
- loopback 2: AIL

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**Wait for Act**

Upon the receipt of AI, the act bit is set to "1" and the NT waits for a response (act=1) from the network side.

The output of indications and transmit signals is as defined for the synchronized state.

**Wait for Superframe**

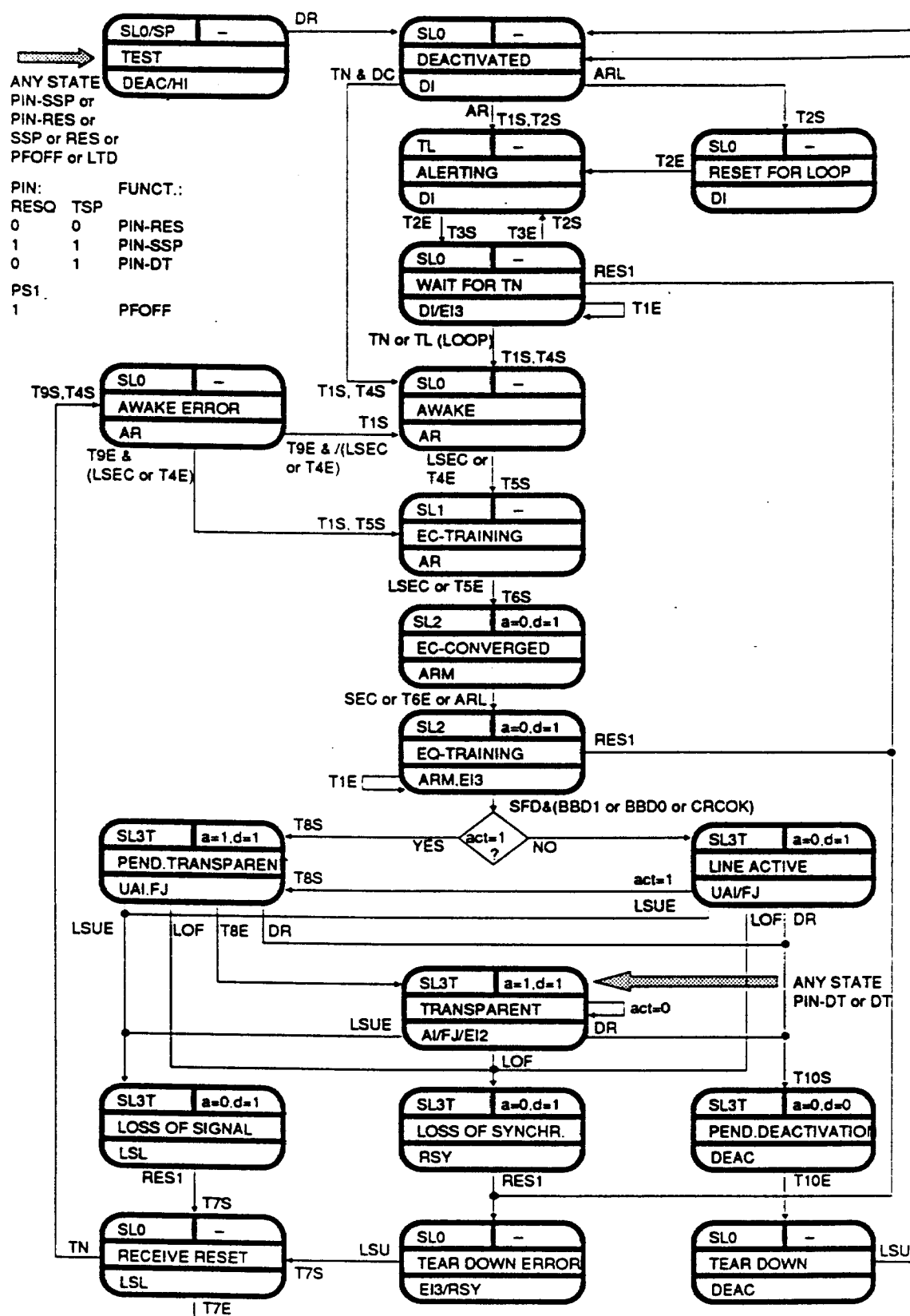
Upon detection of SL2, the signal SN2 is sent on the U interface and the receiver waits for detection of the superframe indication. Timer T1 is then stopped and the synchronized state is entered.

**Wait for Superframe Analog Loopback**

This state is entered in the case of an analog loopback and allows the receiver to update the AGC, to recover the timing phase and to update the EQ coefficients.

Signal SN3 is sent instead of signal SN2 in the wait for SF state.

*JB*



**Fig. 5.7 : state transition diagram LT mode**

**Explanation for LT state diagram**

The following commands or events are used for the transition:

**1.) C/I channel (on DIN)**

**AR Activation Request**

The IEC-Q is requested to enter the power-up state and to start an activation procedure by sending the wake-up signal TL.

**ARL Activation Request Local Loopback**

The IEC-Q is requested to operate an analog loopback (close to the U interface) and to start the start-up sequence by sending the wake-up tone TL. This command may be issued only after the IEC-Q has been set to the deactivated state (C/I channel code DI issued on DOUT) and has to be issued continuously as long as loopback is requested.

**DR Deactivation Request**

This command requests the IEC-Q to start a deactivation procedure by setting the dea bit to "0" and to cease transmission afterwards.

The DR code is not an unconditional command and the IEC-Q reacts on it only in the states line active, pending transparent and transparent i.e. when the C/I channel codes UAI, AI, FJ or EI2 are issued on DOUT.

**DT Data Through**

This unconditional command is used for test purposes only and forces the IEC-Q into the transparent state. The far-end transceiver is assumed to be in the same condition.

**LTD LTDDisable**

This is an unconditional command which requests the IEC-Q to switch off the remote-power-feed circuit for the subscriber line by activating the pin DISS.

**RES Reset**

Unconditional command which resets the whole chip; for cold start the reset code should be applied for a period of at least 8 IOM™ frames (1 ms).

**RES1 Reset1**

The reset 1 command resets all receiver functions, especially the EC and EQ coefficients and the AGC are set to zero. The RES1 code should be used when the IEC-Q has entered a failure condition (expiry of timer T1, loss of framing or loss of signal level) indicated by the C/I channel code EI1 on DOUT.

This command starts a deactivation procedure on the U interface, besides resetting the receiver.

**SSP Send Single Pulses**

Unconditional command which requests the transmission of single pulses on the U interface.

**2.) Pins**

**Pin-RES** Pin-Reset; corresponds to pin RESQ.

The functionality of this pin is the same as for the C/I code RES.

**Pin-SSP** Pin-Send Single Pulses; corresponds to pin TSP.

The functionality of this pin is the same as for the C/I code SSP.

**Pin-DT** Pin-Data Through;

RESQ and TSP are active (RESQ="0" and TSP="1"). The functionality is the same as for the C/I code DT.

**PFOFF** Power Feed Off; corresponds to pin PS1.

This pin indicates that the remote-power-feed circuit for the subscriber line has been turned off. The IEC-Q is requested to forward this indication making use of the C/I channel code HI.



## 3.) Events related to the U interface

act=0/1	<p>act bit received from the user side.</p> <ul style="list-style-type: none"> <li>- act=1 signals that the NT has detected INFO3 on the S/T interface and indicates that the whole basic access is synchronized in both directions of transmission. The network side is requested to provide transparency of transmission in both directions and to respond with setting the act bit to "1". In the case of loopbacks (loopback 2 or single channel loopback in the NT) however, transparency is required even when the NT is not sending act=1.</li> </ul> <p>Transparency is achieved in the following manner:</p> <ul style="list-style-type: none"> <li>- The IEC-Q performs transparency in both directions of transmission after the receiver has achieved synchronization (state EQ training is left) independently of the status of the received act bit.</li> <li>- The status "ready for sending" is reached when the state transparent is entered i.e. when the C/I channel indication AI is issued. This is valid in the case of a normal activation procedure for call control. In the case of loopbacks (loopback 2 or single channel loopback in the NT and analog loopback in the LT) however, the status "ready for sending" is reached when the state line active is entered i.e. when the C/I channel indication UAI is issued. Until the status "ready for sending" is reached, binary "0s" have to be passed in the B and D channels on DIN.</li> <li>- act=0 indicates the loss of transparency on the user side (loss of framing or loss of signal level on the S/T interface). The IEC-Q informs the network side by issuing the C/I channel indication EI2, but performs no state change or other actions.</li> </ul>
CRCOK	<p>Cyclic Redundancy Check OK.</p> <p>This input is used as a criterion that the receiver has acquired frame synchronization and converged both its EC and EQ coefficients.</p>
LOF	Loss of Framing on the U interface (576 msec).
LSEC	<p>Loss of Signal Level behind the Echo Canceler.</p> <p>In the awake state, this input is used as indication that the NT has ceased the transmission of signal SN1. In the EC training state, this input is used as an internal signal indicating that the EC in the LT has converged.</p>
LSU	<p>Loss of Signal Level on the U interface.</p> <p>This signal indicates that a loss of signal level of a duration of 3 ms has been detected on the U interface. This short response time is relevant in all cases where the LT waits for a response (no signal level) from the user side i.e. after a deactivation procedure has been started or after loss of framing in the LT.</p>
LSUE	<p>Loss of Signal Level on the U interface (error condition).</p> <p>This signal indicates that a loss of signal level of a duration of 492 ms has been detected on the U interface. This long response time (see also LSU) is valid in all cases where the LT is not prepared to lose signal level i.e. the NT has stopped transmission because of losing framing or because of an unsuccessful activation or the transmission line is interrupted.</p>
SEC	<p>Signal Level behind the echo canceler.</p> <p>This signal indicates that a signal level corresponding to SN2 from the NT has been detected on the U interface.</p>
SFD	Superframe Detected.
TN	<p>Tone (wake-up signal) received from the NT.</p> <p>When staying in the deactivated state, the IEC-Q is requested to start an activation procedure and to inform the network side making use of the C/I channel code AR. When staying in the wait for awake acknowledge state, the signal TN sent by the NT acknowledges the receipt of a wake-up signal TL from the LT. When an analog loopback is operated, the wake-up signal TL sent by the LT transmitter is detected by the LT receiver.</p>

//

**BBD0/1** Binary "0s" or "1s" detected in the B and D channels.  
 This internal signal indicates that for a period of time of 6-12 ms a continuous stream of binary "0s" or "1s" has been detected. It is used as a criterion that the receiver has acquired frame synchronization and converged both its EC and EQ coefficients.  
 BBD1 corresponds to the signals SN2 or SN3 in the case of a normal activation and BBD0 corresponds to the internally received signal SL2 in the case of an analog loopback or possibly a loopback 2 in the NT.

#### 4.) Timers

	(ms)		(state)
T1	15000	supervisor for start-up	
T2	3	TL transmission	alerting
		receiver reset	reset for loop
T3	40	re-transmission of TL	wait for TN
T4	6000	supervisor SN0 detect	awake
T5	300	supervisor EC converge	EC training
T6	6000	supervisor SN2 detect	EC converge
T8	24	delay time for AI indication	pend.transparent
T7	40	hold time	receive reset
T9	40	hold time	awake error
T10	40	dea=0 transmisssion	pend.deactivation

The following Indications or signals are transmitted:

##### 1.) C/I channel (on DOUT)

**AI** Activation Indication  
 This indication signals that act=1 has been received and that timer T8 has elapsed.  
 This indication is not issued in the case of an analog loopback; it may be issued in the case of loopback 2 or a single channel loopback in the NT.

**AR** Activation Request  
 The AR code signals that a wake-up signal has been received and that a start-up procedure is being performed; receiver synchronization has not yet been achieved.

**DEAC** Deactivation  
 This indication is issued in response to a DR code or in the test state.

**DI** Deactivation Indication  
 Idle code on the IOM™ interface. Normally the IEC-Q stays in the deactivated state, unless an activation procedure was started by the network side.

**EI2** Error Indication 2  
 The NT receiver on the S/T interface has detected a loss of signal level or has lost framing (receipt of act=0).

**EI3** Error Indication 3  
 This indication is issued when the IEC-Q has entered the failure condition; unsuccessful activation (expiration of timer T1).

**LSL** Loss of Signal Level  
 The IEC-Q has entered a failure condition after loss of signal level (LSUE).

**RDY** Resynchronization indication after a loss of framing (LOF).  
 For EI3, LSL and RDY indication the network side should react by applying the C/I channel code RES1, to allow the IEC-Q to enter the receive reset state and to reset the receiver functions.

4/2

- FJ** Frame Jump  
This indication signals that either a data buffer overflow/underflow has been detected or a phase jump of one of the IOM™ timing signals DCL or FSC has occurred. The FJ code is issued for a period of 1.5 ms.
- HI** High Impedance  
PFOFF is activated which means that the remote-power-feed circuit for the subscriber line is turned off.
- UAI** U Activation Indication  
The UAI code signals that the line system is synchronized in both directions of transmission (see also the input act=1).
- ARM** Activation Request Maintenance  
Transmission of maintenance bits is possible.

## 2.) Signals transmitted on the U interface

The signals SLx, TL and SP transmitted on the U interface are defined in section 5.

The polarity of the overhead bits act and dea is indicated as follows:

a=0/1 corresponds to act bit set to binary "0/1".

d=0/1 corresponds to dea bit set to binary "0/1".

The following states are used:

### Alerting

The wake-up signal TL is transmitted for a period of time of T2 in response to an activation request from the network side (AR or ARL).

In the case of an analog loopback, the signal TL is forwarded internally to the wake-up signal detector and stored.

### Awake

This state is entered upon the receipt of a wake-up or an acknowledge signal TN from the NT.

In the case of an activation started by the network side, timer T1 is restarted when the awake state is entered.

### Awake Error

This state is equivalent to the awake state, but is entered only when a wake-up signal is received while in the receive reset state. As the receive reset state was entered upon the application of the C/I channel code RES1, the awake error state assures that a minimum amount of time elapses between the application of the RES1 code and the entrance into a state (EQ training) in which the IEC-Q again reacts on the RES1 code.

The network side is requested to stop issuing the command RES1 within T9 after the receipt of the C/I channel code AR on DOUT and to replace it by another command such as the idle code DC for instance.

### Deactivated (full reset)

This state corresponds to the power-down or low power consumption mode (the receiver and parts of the interface are forced into a power-down mode; functions related to the IOM™ interface and the wake-up signal detector are still active); no signal is sent on the U interface.

The IEC-Q waits for a wake-up signal TN from the user side or an activation request (AR or ARL) from the network side to start an activation procedure.

### EC Converged

Upon convergence of the EC coefficients, the IEC-Q starts the transmission of signal SL2 and waits for the receipt of signal SN2 from the NT (SEC). If no signal is detected within T6 however, the start-up procedure is continued. In the case of an analog loopback, this state is left immediately because the EC compensates for the looped back transmit signal.

HB

**EC Training**

The signal SL1 is transmitted on the U interface to allow the LT receiver to update its EC coefficients. The EC training state is left when the EC has converged (LSEC) or when timer T5 has elapsed. Timer T5 allows the start-up procedure to proceed even if LSEC, because of a high noise level on the U interface for instance, could not be detected.

**EQ Training**

The EQ training is left after the receiver synchronization has been achieved and the superframe indication detected (SFD). Upon expiration of timer T1 the C/I channel indication EI3 is issued.

**Line Active**

In this state, the IEC-Q performs transparency of the transmission in both directions. The line system is synchronized and the maintenance channel is operational.

The IEC-Q stays in the line active state

- during a normal activation procedure for call control or when a single channel loopback is performed in the NT no INFO3 signal is received on the S/T interface i.e. all TE's are unplugged or

- when an analog loopback is established or

- possibly when a loopback 2 is established in the NT and the SBCX monitors INFO3 on the S/T interface and no INFO3 is received.

In the case of normal activation for call control, binary "0s" have to be applied to the B and D channels on the IOM™ interface. After the C/I channel indication UAI has been issued, the layer 2 receiver should be fully operational to prevent the first layer 2 message issued by the user side, upon the receipt of the AI code in the TE, to be lost.

**Loss of Signal**

This state is entered upon the detection of a failure condition i.e. loss of receive signal (LSUE). The act bit is set to "0" and the C/I channel indication LSL is issued. The IEC-Q waits for the C/I channel command RES1 to enter the receive reset state.

**Loss of Synchronization**

This state is entered upon the detection of a failure condition i.e. loss of framing by the LT receiver (LOF).

The act bit is set to "0" and the C/I channel indication RSY is issued. The IEC-Q waits for the C/I channel command RES1 to enter the tear down error state and subsequently the receive reset state.

**Pending Deactivation**

This is a transient state entered after the receipt of a DR code. The dea bit is set to "0". Timer T10 assures that the dea bit is set to "0" in at least three subsequent superframes before the transmit level is turned off.

**Pending Transparent**

This is a transient state entered upon the detection of act=1 and left by T8. The act bit is set to "1". The purpose of this state is to issue the C/I channel indication AI (corresponding to "ready for sending") T8 only after the act bit has been set to "1" by the LT transceiver. This assures that under normal operating conditions the AI indication is issued first on the TE side and only afterwards on the network side and that normally the layer 2 receiver in the TE is already operational when the first layer 2 message is issued by the network side.

**ReceiveReset**

The receive reset state assures that for a period of T7 no signal, especially no wake-up signal TL, is sent on the U interface i.e. no activation procedure is started from the network side. However, a wake-up signal TN from the user side is acknowledged.

**Tear Down**

In this state, transmission ceases in order to deactivate the basic access and the IEC-Q waits for a response (no signal level, LSU) from the user side.

**Tear Down Error**

This state is entered after loss of framing was detected. Transmission ceases in order to deactivate the basic access and the IEC-Q waits for a response (no signal level, LSU) from the user side. -

EI3 indication is transmitted after a transition forced by RES1 from the wait for TN or EQ training states. In the case of transition from the loss of synchronization state RSY is sent.

**Test**

This testmode is entered when the unconditional commands RES, SSP, LTD, Pin-RES, Pin-SSP or PFOFF are used. It is left when the pins RESQ, TSP and PS1 are inactive and the C/I channel code DR is received.

The output signals are as follows:

- when the C/I channel code RES is applied or when the pin RESQ is activated:

SL0 and DEAC

- when the C/I channel code SSP is applied or when the pin TSP is activated:

single pulses (SP) and DEAC

- when the C/I channel code LTD is applied:

SL0 and DEAC; furthermore, the pin DISS is activated

- when the pin PS1 is activated:

SL0 and HI

In this state the IEC-Q does not react to the receipt of a wake-up signal TN.

**Transparent**

This state corresponds to the fully active state in the case of a normal activation for call control.

It may be entered in the case of a loopback 2 or a single channel loopback in the NT.

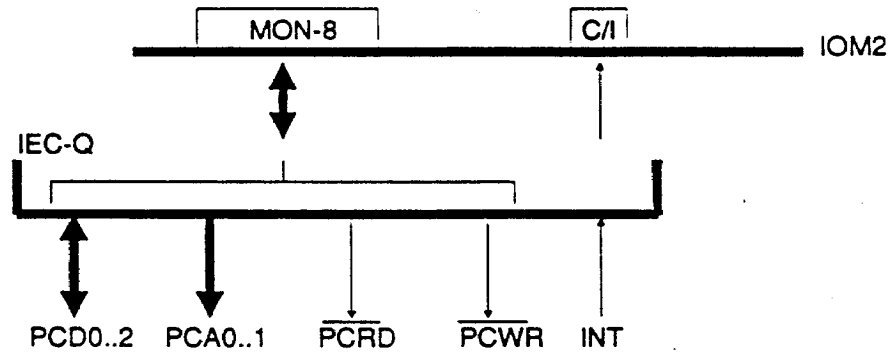
The network side is informed that the status "ready for sending" is reached (indication AI). If the user side loses transparency (receipt of art=0), the network side is informed by making use of the C/I channel indication EI2, but no state change is performed.

**Wait for Awake Acknowledge**

The IEC-Q waits for a response (tone TN from the NT or tone TL in the case of an analog loopback) to the transmission of wake-up signal TL. If no response is received within T3, the state is left for retransmission of a wake-up tone TL. This procedure is repeated until the detection of tone TN or until the expiration of timer T1. In this case the C/I channel indication EI3 is issued, but no state change is performed.

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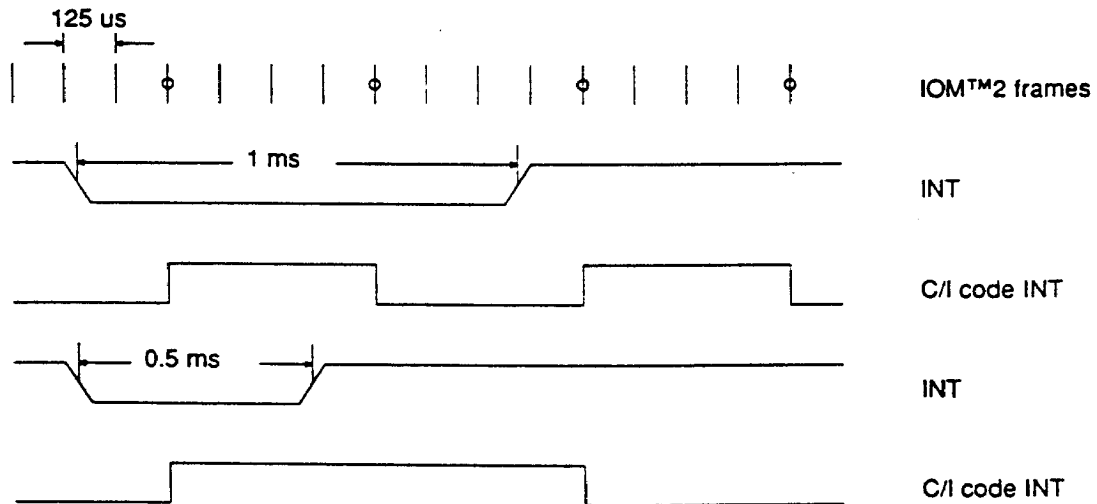
## 6. Controller interface



A controller interface is implemented to handle control functions via the IOM™2 interface to connect circuits without direct access to a micro processor. A typical application is the direct connection of the IEPC power controller.

### INT

For every change at the input pin (INT) the IEC-Q will transmit a C/I channel code "0110" (INT) in four subsequent IOM™ frames. The input condition of the interrupt pin is sampled every 4 IOM™2 frames.



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PCA0..1, PCD0..2,  $\overline{PCWR}$   $\overline{PCRD}$ 

Communication is performed by using the local MONITOR message (MON-8) of the IOM™2 interface. The following 2-byte messages are adapted to the IEPC power controller status register read and write operations, but can be used in general too.

MON-8	WCI	Write Controller Interface
1 0 0 0 0 0 0 0		0 1 1 D0 D1 D2 A0 A1
MON-8	RCI	Read Controller Interface
1 0 0 0 0 0 0 0		0 1 0 - - - A0 A1
MON-8	ACI	Answer Controller Interface
1 0 0 0 0 0 0 0		D0 D1 D2 - - - - -

After the receipt of the MONITOR message, the IEC-Q will set the address/data bits and generate the read and write pulse.

The address bits are latching, the output is stable until a overwrite by a new dedicated MON-8 message appears.

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## 7. Analog Line Port

The analog part of the IEC-Q consists of three main building blocks:

- the analog-to-digital converter in the receive path
- the digital-to-analog converter and
- the output buffer in the transmit path

Furthermore, it contains some special functions. These are:

- the analog test loop
- the range function (attenuation of the input signal)
- the level detect function (starting activation of the IEC-Q)

### 7.1 Analog-to-Digital Converter (ADC)

The ADC was specially developed for this application. It is a sigma-delta modulator of second order using a clock rate of 15.36 MHz. This means a ratio clock frequency/baseband width of 192. The output signal is converted to a standard digital word in a special digital filter. At the output of this digital filter a resolution and linearity of 65 dB or approximately 11 bit is achieved. The input signal to this ADC can be attenuated by 6 dB, activating the range function. The ADC can be internally tied to the output of the transmitter activating the loop function.

#### Input signal range

The peak input signal, measured between AIN and BIN, must be below 4 V peak-to-peak. The maximum SNR is achieved with 1.3 Vpp (range inactive) or 2.6 Vpp (range active) input signal voltage.

#### Input Impedance

The input impedance, measured between AIN and BIN, is at least 50 k.

### 7.2 Special functions

#### Range function

For short lines, the input signal to the ADC is automatically attenuated by  $6 \text{ dB} \pm 1 \text{ dB}$  in order to lower the high receive signal.

#### Loop function

An external loop command in the C/I channel activates an internal analog test loop from the output pins to the input pins of the IEC-Q. The signal is attenuated by approximately 12 dB within this loop.

#### Level detect

The level detect circuit evaluates the differential signal between AIN and BIN. The differential threshold level is between 4 and 30 mV. The DC level (common mode level) may be between 0 and 3 V. Level detect is not affected by the loop and range setting.

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### 7.3 Digital-to-Analog Converter (DAC)

The shape of the output pulse is formed in a special DAC. The DAC was specially optimized for excellent matching between positive and negative pulses and high linearity. It uses a fully differential switched-capacitor approach. The staircase-like output signal of the DAC drives the output buffers. The shape of the DAC output signal is shown below, with the peak amplitude normalized to one. This signal is fed to the output through a switched-capacitor lowpass and a RC lowpass of first order with a corner frequency of  $1\text{ MHz} \pm 50\%$ .

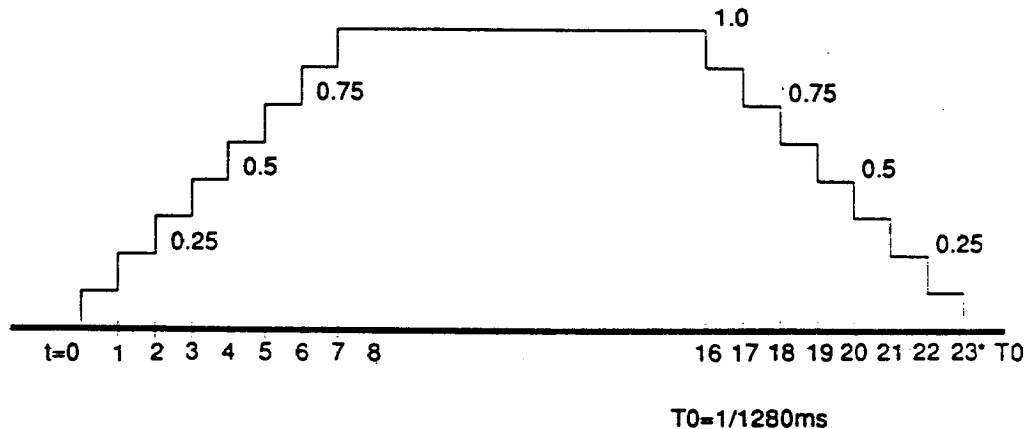


Fig. 7.1 : DAC output for a single pulse

The duration of each output pulse is 11 steps, with  $t = 1/640\text{ ms}$  per step. On the other hand, the pulse rate is 80 kHz or one pulse per 8 steps. Thus, subsequent pulses are overlapping for a duration of 3 steps.

#### Symbol rate

The symbol rate is  $80\text{ kbaud} \pm 1\text{ ppm}$  and applies to synchronous symbol transmission with a clock generated by LT circuits.

#### Output stage

The output stage consists of two identical buffers, operated in a differential mode. This concept allows an output voltage swing of 6.4 V peak-to-peak at the output pins of the IEC-Q. The buffers are optimized for:

- high output swing
- high linearity
- low quiescent current to minimize power consumption.

The output jitter produced by the transmitter (with jitter free input signals) is below 0.02 UIpp measured with a highpass filter of 30 Hz cutoff frequency. Without the filter, the output jitter is below 0.1 UIpp.

#### Pulse shape

The pulse mask for a single positive pulse measured between AOUT and BOUT with a load of  $98\ \Omega$  is given in the following figure.

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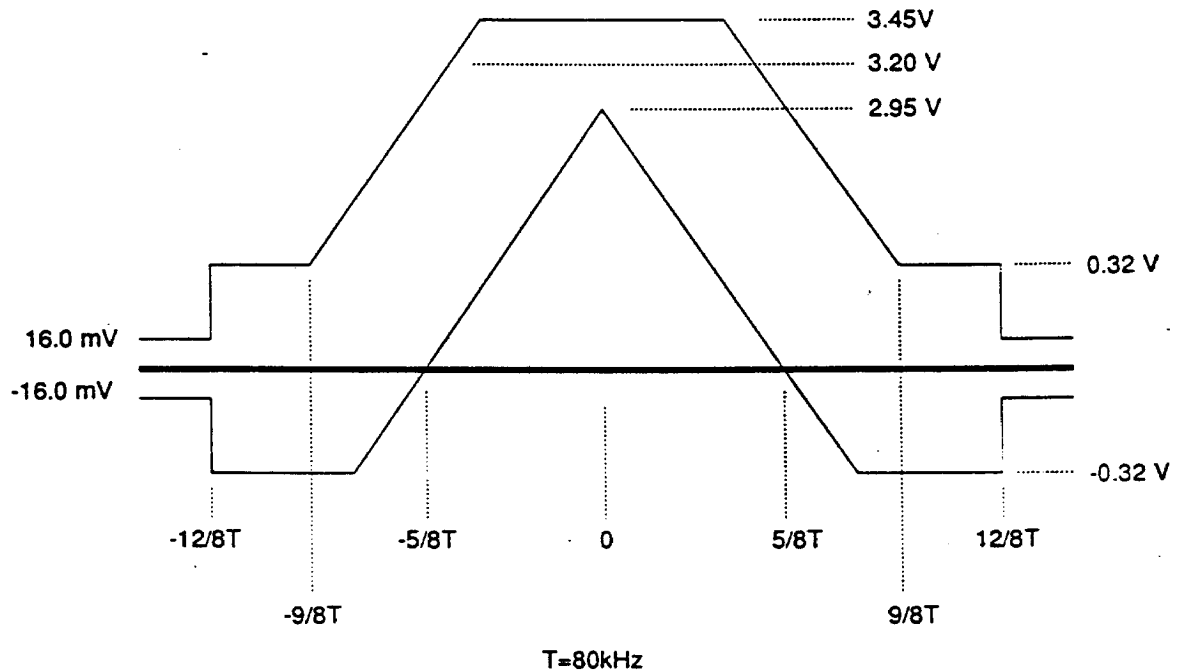
**Signal amplitude**

Fig. 7.2 : pulse mask for a single positive pulse

The peak-to-peak voltage of a single positive pulse measured between AOUT and BOUT and terminated with  $98 \Omega$  is  $3.2 \text{ V} \pm 4.5\%$ .

**Offset voltage**

The offset voltage, measured under the same conditions as above, is less than 2 % of the peak amplitude.

**Signal stability**

The signal amplitude measured over a period of one minute varies less than 1 %.

**Output impedance**

The output impedance measured between AOUT and BOUT is below  $4 \Omega$  in power-up and below  $12 \Omega$  in power-down mode. The required impedance of  $135 \Omega \pm 5\%$  seen from the line side of the transformer is established by putting two resistors of  $24 \Omega \pm 0.1\%$  each in the hybrid.

**Load**

The load is given by the hybrid, the transformer and the subscriber line. The transformer ratio should be 1:1.65 (circuit/line side) and the total inductivity seen from the line side between 10 and 15 mH.

**Noise and distortion level**

The sum of noise and total harmonic distortion, weighted with a low pass filter 0 to 80 kHz, is at least 65dB below the signal for an evenly distributed but otherwise random sequence of +3, +1 and -1, -3.

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## 7.4 Specified Data for Analog Function

parameter	min.	typ	max.	units
receive path:				
signal/(noise+dest.)	60	65		dB
DC-level at AD-output	0.45	0.5	0.55	
threshold of level detect	4		30	mV
transmit path:				
signal/(noise+dest.)	65	70		dB
output DC-level	2.05	2.375	2.6	V
offset between AOUT/BOU			35.5	mV
signal amplitude	3.05	3.2	3.35	V
output impedance between AOUT/BOU				
power-up		2	4	Ohm
power-down		6	12	Ohm

( TA = 70 degree centigrade, VDD = 4.75 V )

Tab. 7.1 : specified data of analog functions

## 7.5 Clock generation

### NT modes:

The master clock is derived from a built in crystal oscillator. The crystal is connected to the pins XIN and XOUT. The maximum capacitive load at XIN is 40 pF each.

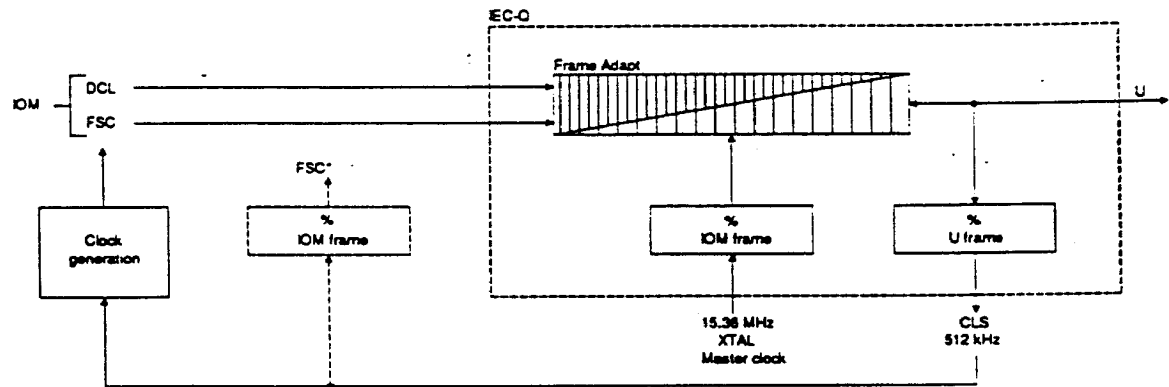
### Master clock:

Nominal frequency: 15.36MHz  
Overall tolerance:  $\pm 100$  ppm

A crystal (serial resonance) is connected which meets the following specification:

Nominal frequency: 15.36MHz  
Overall tolerance:  $\pm 60$  ppm  
Load capacitance: 20 pF  
Resonance resistance: 20  $\Omega$   
Shunt capacitance: 7 pF

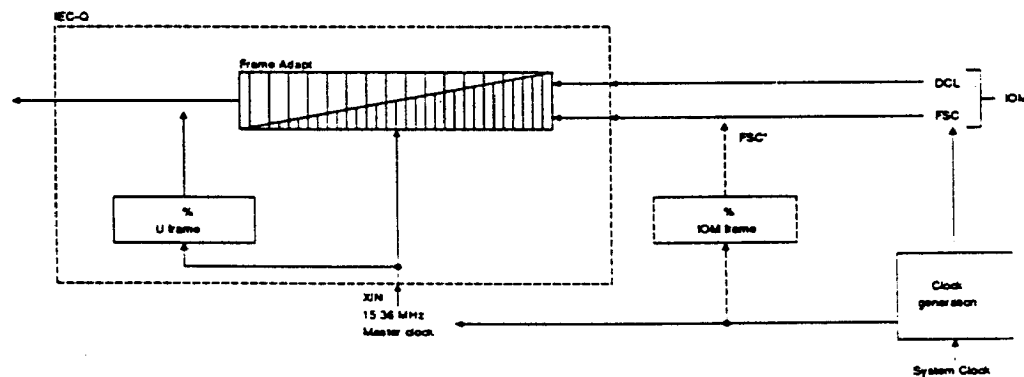
## NT-PABXmode:



Max. difference of phase deviation of FSC and fictitious FSC\* :  $\pm 18\mu s$

## LT modes:

In the LT modes, the timing signals are derived from the system clock via an external phase locked loop. The master clock is fed to pin XIN.



## Master clock:

Nominal frequency:

15.36MHz

Duty ratio:

$0.5 \pm 5\%$

Rise and fall times:

$< 10 \text{ ns}$

Max. low freq. phase wander within 1 period:

$\pm 0.85 \text{ ps}$

Jitter (peak-to-peak):

see following figure 7.3

Max. difference of phase deviation of FSC and fictitious FSC\*:

$\pm 18\mu s$

Start of activation, phase difference:

0

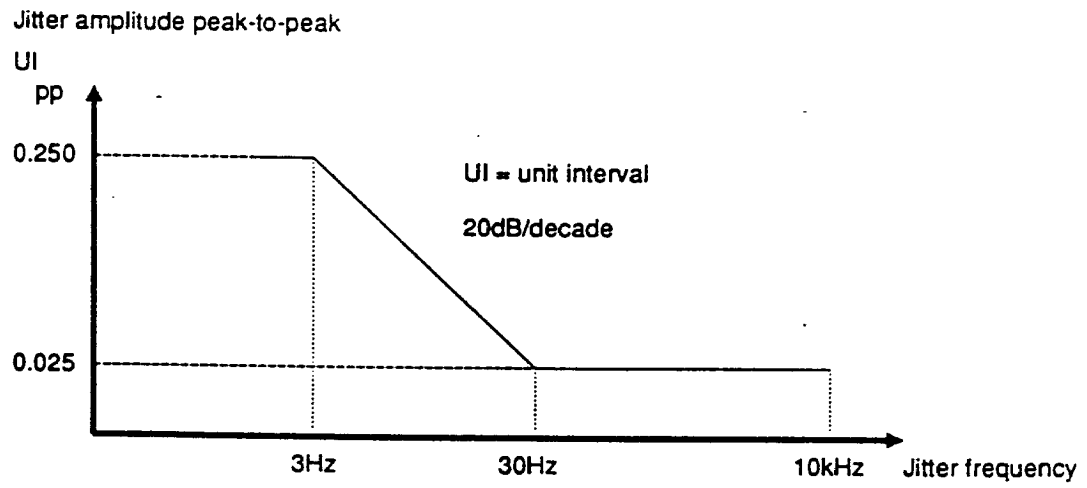


Fig. 7.3: Range of sinusoidal input jitter

## 8. Electrical Characteristics

Unless otherwise specified, the static and dynamic characteristic limits apply over a supply voltage range of 4.75 to 5.25 Volts.

### 8.1 Static characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{IH}$	High Level Input Voltage		3.5		$V_{DD} + 0.3$	V
$V_{IL}$	Low Level Input Voltage				1.0	V
$I_{IL}$	Low Level Input Leakage current	$V_{in} = DGND$	-10			$\mu A$
$I_{IH}$	High Level Input Leakage current all inputs except AIN, BIN, XIN, XOUT, VREF	$V_{in} = DVDD$			10	$\mu A$
$V_{OH1}$	High Level Output Voltage all outputs except DOUT	$I_{OH1} = 0.4 \text{ mA}$	4.0			V
$V_{OH2}$	High Level Output Voltage DOUT	$I_{OH2} = 6 \text{ mA}$	4.0			V
$V_{OL1}$	Low Level Output Voltage all outputs except DOUT	$I_{OL1} = 2 \text{ mA}$			0.33	V
$V_{OL2}$	Low Level Output Voltage DOUT	$I_{OL2} = 7 \text{ mA}$			0.5	V
$C_{IN}$	Input Capacitance DIN, PS1, PS2, DCL, FSC (input), DOUT (open)				10	pF

Tab. 8.1 : static characteristics

#### Power Consumption

All measurements with random 2B+D data in active states, +5 V, 0 to +75 °C.

Symbol	Parameter	Min	Typ	Max	Unit	Comments
	135 Ohm line load		340		mW	power up mode
			50		mW	power down LT/NT-PABX mode
			45		mW	power down NT/TE mode

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## 8.2 Dynamic Characteristics

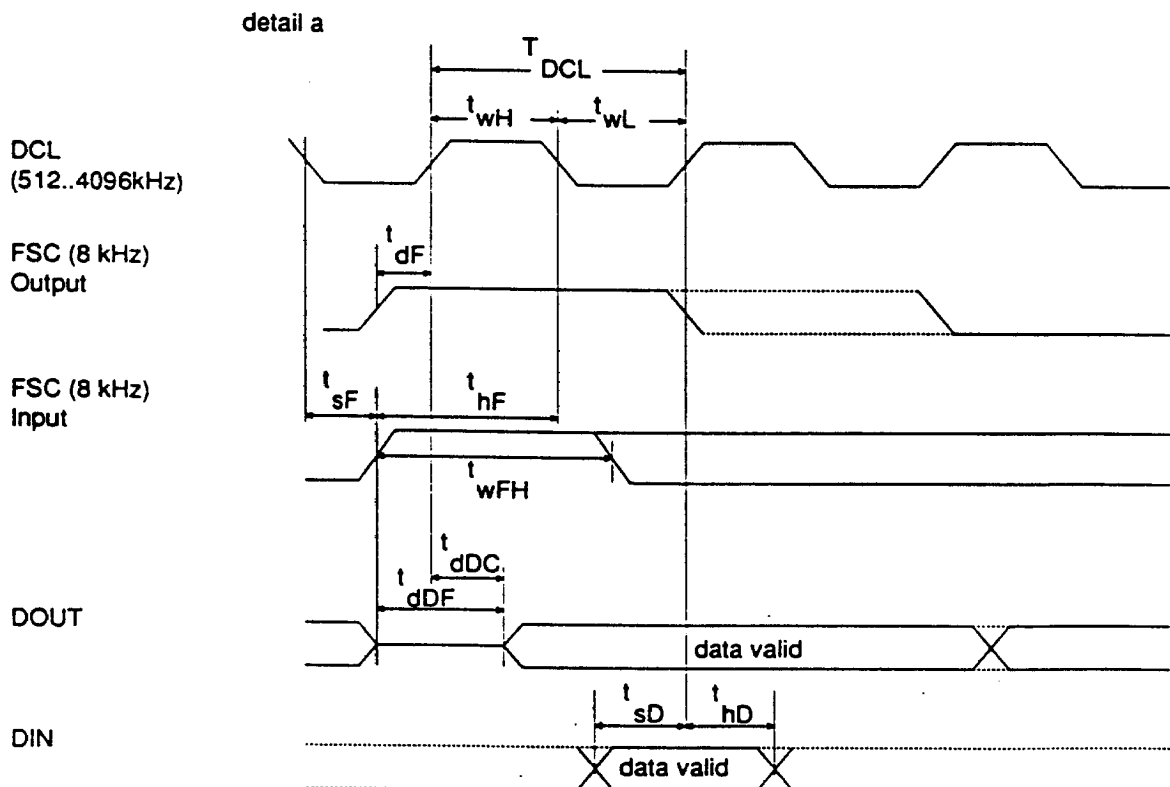
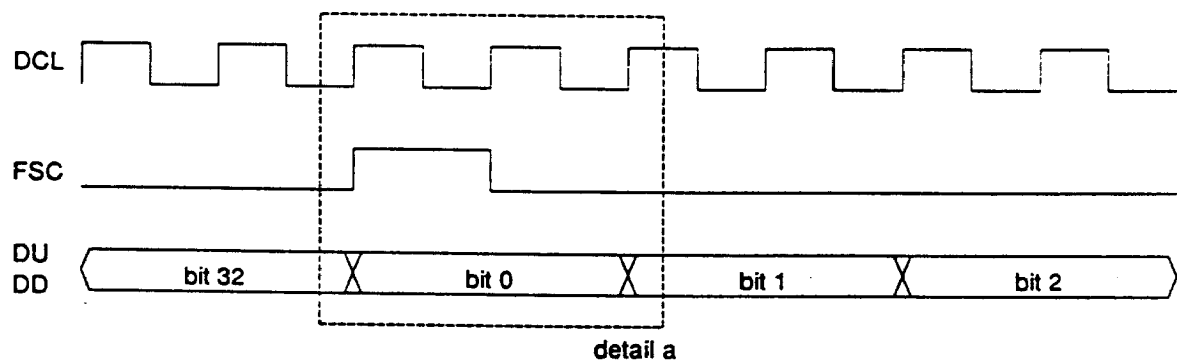
### 8.2.1 IOM™2 Interface Timing

Data is transmitted in both directions (DU and DD) at half the data clock rate. The transmitter synchronizes the information to the rising edge.

The data clock (DCL) is a square wave signal with a duty cycle ratio of typically 1:1. The frequency is variable and can be set for values ranging from 512 kHz to 4.096 MHz.

The frame clock (FSC) is an 8 kHz signal for synchronizing data transmission on DU and DD. The rising edge of this signal gives the time reference for the first bit transmitted in the first IOM™2 channel. In the master mode (NT) the output of FSC will mark the position of the superframe by either a single HIGH phase of a DCL period, or a two time HIGH phase of a DCL period is transmitted.

For power saving reasons, the IOM™2 interface can be switched into a "power-down" state. In this case, the idle state of the data lines are high, while those of the clock lines are low.



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parameter	signal	abbr.	min.	max.	units
data clock	DCL	tr, tf		60	ns
clock period	DCL	TDCL	200		ns
pulse width	DCL	twH, twL	53		ns
frame sync.	FSC	tr, tf		60	ns
frame setup	FSC	tsF	30		ns
frame hold	FSC	thF	30		ns
frame width high	FSC	twFH	100		ns
frame width low	FSC	twFL	2*TDCL		ns
data delay/frame	DOUT	tdDF		150 1)	ns
data setup	DIN	tsD	20		ns
data hold	DIN	thD	50		ns

Tab. 8.3 : dynamic input characteristics

parameter	signal	abbr.	test condition	min.	typ	max.	units
data clock	DCL	tr, tf	CL=25pF			30	ns
clock period 2)	DCL	TDCL	CL=25pF	1875	1953	2035	ns
pulse width 2)	DCL	twH, twL		880	977	1075	ns
clock period 3)	DCL	TDCL	CL=25pF	565	651	735	ns
pulse width 3)	DCL	twH, twL		230	325	420	ns
frame width high superframe	FSC	twFH	CL=25pF		TDCL		
frame width high normal frame	FSC	twFH	CL=25pF		2*TDCL		
frame sync.	FSC	tr, tf	CL=25pF			30	ns
frame delay	FSC	tdF	CL=25pF	160	130	100	ns
data out	DOUT	tf	C=150pF (R=1kOhm to VDD DOD pin high) or RESQ pin low			200	ns
data out	DOUT	tr, tf	C=150pF DOD pin low RESQ pin high			150	ns
data delay/clock	DOUT	tdDC	CL=150pF			100	ns
data setup	DIN	tsD		twH+20			ns
data hold	DIN	thD		50			ns

1) condition CL=150pF    2) 256 kbps    3) 768 kbps

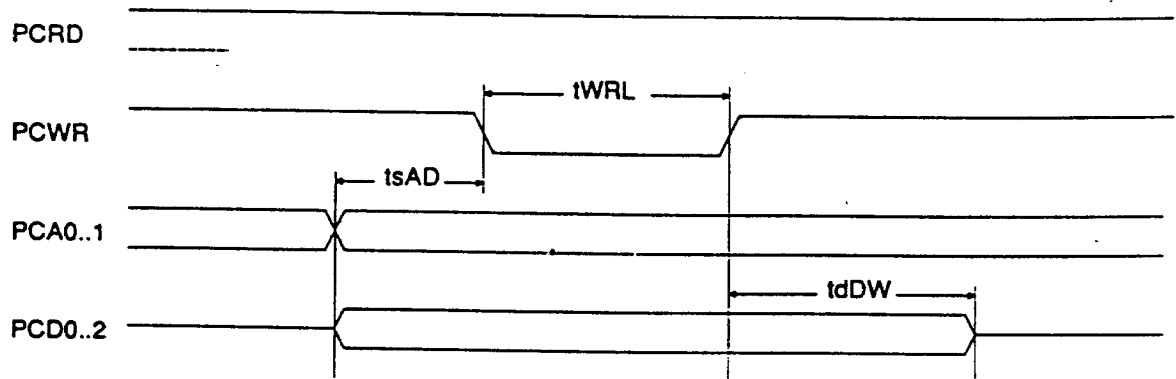
Tab. 8.2 : dynamic output characteristics

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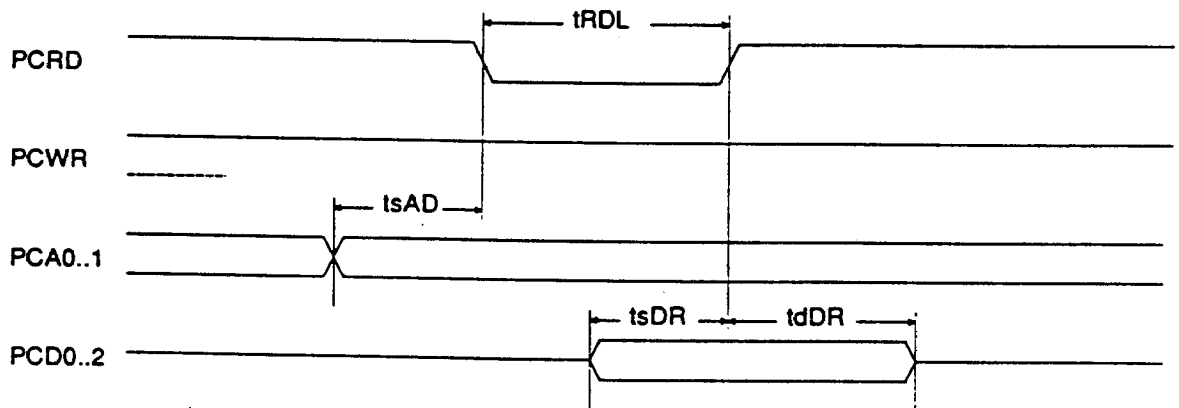


## 8.2.2 Controller Interface Timing

## WRITE access



## READ access



## Interrupt

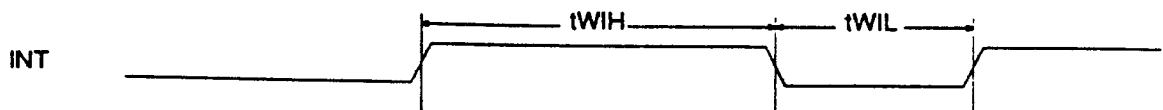


Fig. 8.1 : controller interface timing

parameter	signal	abbr.	min.	typ	max.	units
write clock	PCWR	tr, tf			30	ns
write width	PCWR	tWRL		4*TDCL		
address setup	PCA0..1	tsAD		2*TDCL		
data delay write	PCD0..2	tdDW		2*TDCL		
data delay read	PCD0..2	tdDR	130			ns
setup data read	PCD0..2	tsDR	130			ns
read clock	PCRD	tr, tf			30	
read width	PCRD	tRDL		4*TDCL		
interrupt length	INT	tWIH	0.5			ms
		tWIL	0.5			ms

all test condition : CL = 25 pF

Tab. 8.4 : dynamic characteristics of controller interface

### 8.3 Power supply

Supply voltages

$$VDDd = + 5V \pm 0.25V$$

$$VDDa1 = + 5V \pm 0.25V$$

$$VDDa2 = + 5V \pm 0.25V$$

Maximum ripple on VDDa1 and VDDa2 max. 50mV peak-to-peak

### 8.4 Maximum ratings

Maximum ratings are those parameter limits above which permanent damage to the integrated circuits may occur. It is not implied, that more than one of these conditions can be applied simultaneously.

Maximum positive supply voltage:

$$VDD = + 5V$$

Maximum voltage applied to any input:

$$-0.3V \leq V_{in} \leq VDDd + 0.3V$$

Maximum voltage applied line port:

$$-0.3V \leq V_{in} \leq VDDa + 0.3V$$

Max. voltage between GNDa1 (GNDa2) and GNDd:

$$\pm 250mV$$

## 9. IEC-Q PEB 2091 Pin Definitions and Functions

PIN	Symbol		Function
7,8	VDDa1		5 V $\pm$ 5 % analog supply voltage.
13	VDDa2		5 V $\pm$ 5 % analog supply voltage.
5	GNDa1		0 V analog.
16	GNDa2		0 V analog.
1,2	VDDd		5 V $\pm$ 5 % digital supply voltage.
23	GNDd		0 V digital.
11	XIN	I	In all NT modes, crystal connection. In all LT modes, 15.36 MHz clock input synchronized to IOM™ clocks.
10	XOUT	O	In all NT modes, crystal connection. In all LT modes, to be left open.
15	AIN	I	Received line signal to hybrid.
14	BIN	I	Received line signal to hybrid.
6	AOUT	O	Transmitted line signal to hybrid.
4	BOUT	O	Transmitted line signal to hybrid.
9	VREF	O	VREF pin to buffer internally generated voltage with capacitor 100 nF vs GNDa.
31	DCL	I/O	IOM™2 device clock.
30	FSC	I/O	IOM™2 frame clock.
26	DIN	I	IOM™2 data input synchronous to DCL.
25	LT	I	LT mode. (HIGH input = LT mode) (LOW input = NT mode)
24	BURST	I	NT-, NT-TE mode. (LOW) LT-, NT-PABX mode. (HIGH)
36	SLOT0	I	256 kbit/s modes select. Allocation of time slot for BURST mode.
35	SLOT1	I	256 kbit/s modes select. Allocation of time slot for BURST mode.
33	SLOT2	I	256 kbit/s modes select. Allocation of time slot for BURST mode.
32	CLS	O	TE/NT: 7.68 MHz clock out sync to line signal. NT-PABX: 512 kHz clock out sync to line signal.

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Pin	Symbol		Function
21	PS1-	I	NT: Power Status (primary). LT: PFOFF, Power Feed Off must be clamped to LOW if not used.
22	PS2	I	NT: Power Status (secondary). LT: Monitor Power Feed (active HIGH). Serial data of Power Feed Current.
18	AUTO	I	Auto-/transparent mode selection of EOC (automode=HIGH).
3	TSP	I	Test Single Pulses. Transmit of alternating $\pm 3$ quaternary symbols. 1.5 ms cycle Must be clamped to LOW if not used.
28	RESQ	I	Power On Reset (active LOW) must be low at least 300 $\mu$ s. The clock on the DCL pin has to be applied during RESET in the LT mode and in the NT-PABX mode. Clamp to HIGH if not used.
27	DOUT	O	IOM <sup>TM</sup> 2 Data Output synchronous to DCL (tristate or open drain).
37	DISS	O	Dissable supply (active HIGH).
19	INT	I	Controller interface interrupt must be clamped to LOW during normal operation.
20	TP1	I	Test Pin (digital loop, do not connect; internal pull-down).
29	TP	I	Test Pin (do not connect; internal pull-down).
44	PCD0	I/O	Power Controller interface data bus (MSB, do not connect if not used; internal pull-up).
43	PCD1	I/O	Power Controller interface data bus (do not connect if not used; internal pull-up).
42	PCD2	I/O	Power Controller interface data bus (LSB, do not connect if not used; internal pull-up).
41	$\overline{\text{PCRD}}$	O	Power Controller interface read request (active LOW).
40	$\overline{\text{PCWR}}$	O	Power Controller interface write request (active LOW).
39	PCA0	O	Power Controller interface address bus.
38	PCA1	O	Power Controller interface address bus.
17	DOD	I	DOUT Open Drain (HIGH); tristate driver at DOUT (LOW).
12,34	n.c.	-	not connected. for reason of compatibility do not connect externaly.

note:

Pin 44, 43, 42, 41, 40, 39, 38, 17 are switched as test pins (I/O) during test condition.

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for DOD = "1" : DOUT open drain output (external pull-up)

for DOD = "0" : DOUT:

	binary equivalent DOUT	DOUT in SLOT position	DOUT in /SLOT position
RESQ = "0"	"0":	low	internal pullup
	"1":	internal pullup	internal pullup
RESQ = "1"	"0":	low	high Z
	"1":	high	high Z

RESQ	TSP	mode
0	0	RESET
0	1	Data Through
1	0	normal
1	1	Test Single Pulses

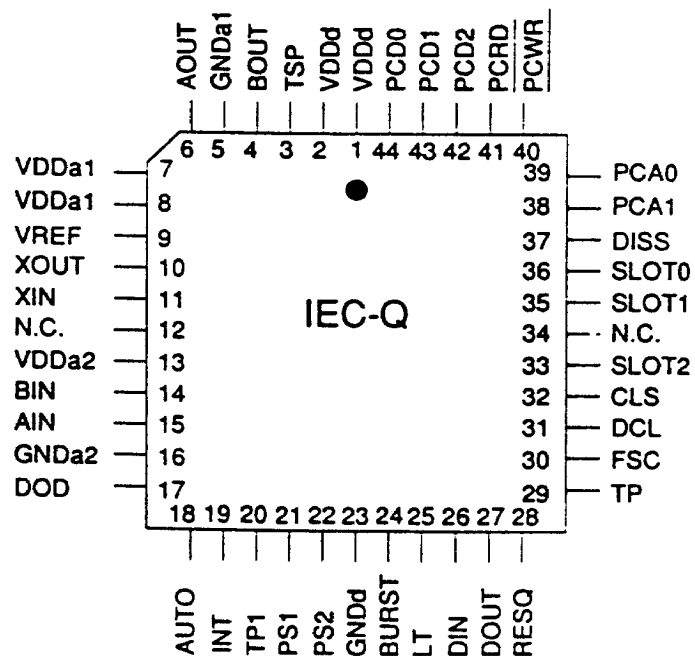


Fig. 9.1 : 2091 pin configuration (top view)

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