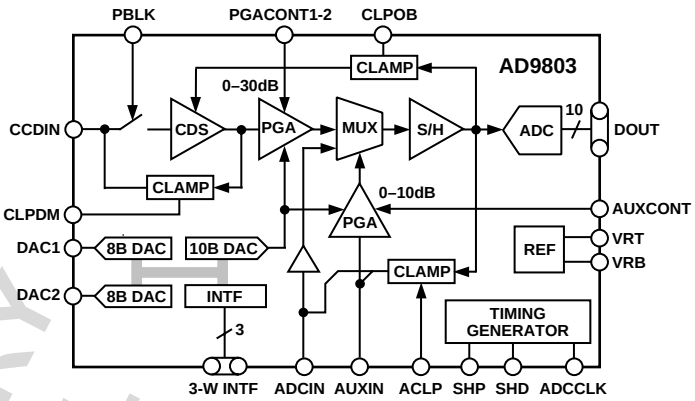
CCD Signal Processor for Electronic Cameras

Preliminary Technical Data — AD9803

FEATURES

3-Wire Serial I/F for Digital Control
21 MHz Correlated Double Sampler
Low Noise PGA with 0 dB–30 dB Range
Analog Pre-Blanking Function
AUX Input with Input Clamp and PGA
10-Bit 27 MSPS A/D Converter
Direct ADC Input with Input Clamp
Internal Voltage Reference
Two Auxiliary 8-Bit DACs
+3 V Single Supply Operation
Low Power CMOS: 190 mW
48-Lead LQFP Package

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD9803 is a complete CCD and video signal processor developed for electronic cameras. It is well suited for video camera and still-camera applications.

The 21 MHz CCD signal processing chain consists of a CDS, low noise PGA, and 10-bit ADC. Required clamping circuitry and a voltage reference are also provided. The AUX input features a wideband PGA and input clamp, and operates up to 27 MHz.

The AD9803 operates from a 3 V supply with a power consumption of 190 mW. The AD9803 is packaged in a space saving 48-lead LQFP and is specified over an operating temperature range of –20°C to +75°C.

REV. PrA

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AD9803–SPECIFICATIONS

GENERAL SPECIFICATIONS

Parameter	Min	Typ	Max	Units
TEMPERATURE RANGE				
Operating	–20		70	°C
Storage	–65		150	°C
POWER SUPPLY VOLTAGE				
Analog	2.7	3.3	3.6	V
Digital	2.7	3.3	3.6	V
Digital Driver	2.7	3.3	3.6	V
POWER CONSUMPTION				
(Power-Down Modes Selected Through Serial I/F)				
Normal Operation (D-Reg 00)		(Specified Under Each Mode of Operation)		
Standby Mode (D-Reg 01)		30		mW
Reference Standby (D-Reg 10 or STBY Pin Hi)		10		mW
Shutdown Mode (D-Reg 11)		10		mW
MAXIMUM CLOCK RATE		(Specified Under Each Mode of Operation)		
S/H AMPLIFIER				
Gain		0		dB
Clock Rate			27	MHz
A/D CONVERTER				
Resolution	10			Bits
Differential Nonlinearity				
0–255 Code		±0.5	±0.8	LSBs
256–1023 Code		±0.5	±1.0	LSBs
No Missing Codes		GUARANTEED		
Full-Scale Input Range		1.0		V p-p
Clock Rate			27	MHz
REFERENCE				
Reference Top Voltage		1.75		V
Reference Bottom Voltage		1.25		V

Specifications subject to change without notice.

DIGITAL SPECIFICATIONS

Parameter	Symbol	Min	Typ	Max	Units
LOGIC INPUTS					
High Level Input Voltage	V_{IH}	2.1			V
Low Level Input Voltage	V_{IL}			0.6	V
High Level Input Current	I_{IH}		10		µA
Low Level Input Current	I_{IL}		10		µA
Input Capacitance	C_{IN}		10		pF
LOGIC OUTPUTS					
High Level Output Voltage	V_{OH}	2.1			V
Low Level Output Voltage	V_{OL}			0.6	V
High Level Output Current	I_{OH}		50		µA
Low Level Output Current	I_{OL}		50		µA

Specifications subject to change without notice.

CCD-MODE SPECIFICATIONS

Parameter	Min	Typ	Max	Units
POWER CONSUMPTION		190		mW
MAXIMUM CLOCK RATE	21			MHz
CDS				
Gain		0		dB
Allowable CCD Reset Transient[1]		500		mV
Max Input Range Before Saturation[1]	1000			mV p-p
PGA				
Max Input Range	1000			mV p-p
Max Output Range	1000			mV p-p
Digital Gain Control				
Gain Control Resolution		10 (Fixed)		Bits
Gain (Selected Through Serial I/F)				
Gain(0) Gain(100)		0		dB
Gain(1023) Gain(820)		30		dB
Analog Gain Control				
PGACONT1 = 0.3 V, PGACONT2 = 1.5 V		0		dB
PGACONT1 = 2.4 V, PGACONT2 = 1.5 V		30		dB
PGACONT1 Gain Slope		14.3		dB/V
PGACONT2 Gain Slope		0.89		dB/V
BLACK-LEVEL CLAMP				
Clamp Level (Selected by the Serial I/F)				
CLP(0) (E-Reg 00)		32		LSB
CLP(1) (E-Reg 01)		48		LSB
CLP(2) (E-Reg 10)		64		LSB
CLP(3) (E-Reg 11)		16		LSB
TIMING SPECIFICATIONS[3]				
Pipeline Delay				
Even-Odd Offset Correction Disabled		5		Cycles
Even-Odd Offset Correction Enabled		7		Cycles
Internal Clock Delay[4] (t_{ID})	3			ns
Inhibited Clock Period ($t_{INIHIBIT}$)	15			ns
Output Delay (t_{OD})			20	ns
Output Hold Time (t_{HOLD})	2			ns
ADCCLK, SHP, SHD, Clock Period	47			ns
ADCCLK Hi-Level, Or Low-Level	20			ns
SHP, SHD Minimum Pulsewidth[5]	10			ns
SHP Rising Edge to SHD Rising Edge	20			ns

NOTES

[1]Input Range is defined as the peak-to-peak difference between the CCD's reference and data levels

[3]20 pF loading; timing shown in Figure 1.

[4]Internal aperture delay for actual sampling edge.

Specifications subject to change without notice.

AD9803–SPECIFICATIONS

AUX-MODE SPECIFICATIONS

Parameter	Min	Typ	Max	Units
POWER CONSUMPTION		100		mW
MAXIMUM CLOCK RATE	27			MHz
PGA				
Max Input Range	700			mV p-p
Max Output Range	1000			mV p-p
Digital Gain Control				
Gain Control Resolution		8		Bits
Gain (Selected by the Serial I/F)				
Gain(0)		0		dB
Gain(255)		10		dB
Analog Gain Control				
AUXCONT = 0.3 V		0		dB
AUXCONT = 2.4 V		10		dB
AUXCONT Gain Slope		4.167		dB/V
AUXCONT Stable Range	0.3		2.7	V
ACTIVE CLAMP (CLAMP ON)				
Clamp Level (Selectable by the Serial I/F)				
CLP(0) (E-Reg 00)		32		LSB
CLP(1) (E-Reg 01)		48		LSB
CLP(2) (E-Reg 10)		64		LSB
CLP(3) (E-Reg 11)		16		LSB
TIMING SPECIFICATIONS[1]				
Pipeline Delay		4 (Fixed)		Cycles
Internal Clock Delay (T_{ID})			5	ns
Output Delay (T_{OD})			20	ns
Output Hold Time (T_{HOLD})	2			ns

NOTES
[1]20 pF loading; timing shown in Figure 2.
Specifications subject to change without notice.

ADC-MODE SPECIFICATIONS

Parameter	Min	Typ	Max	Units
POWER CONSUMPTION		100		mW
MAXIMUM CLOCK RATE	27			MHz
ACTIVE CLAMP (Same as AUX-MODE)				
TIMING SPECIFICATIONS (Same as AUX-MODE)				

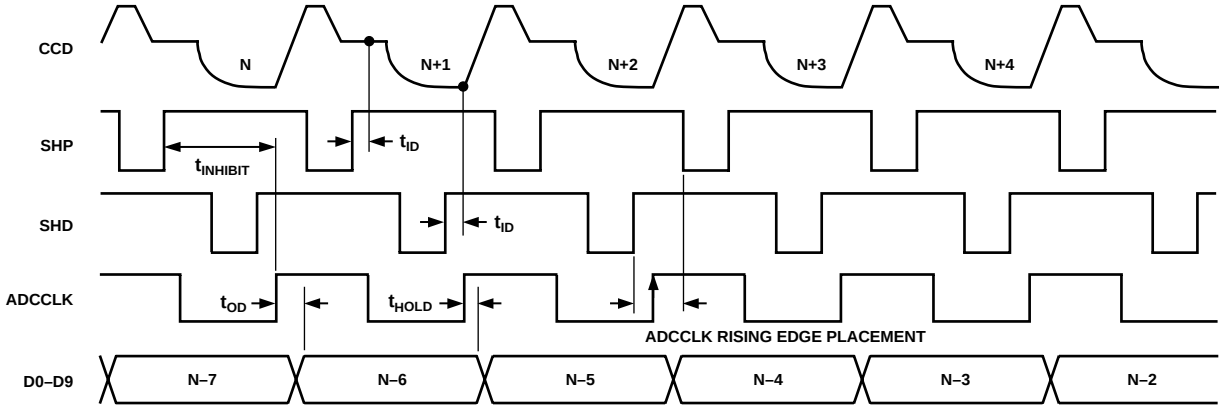
Specifications subject to change without notice.

DAC SPECIFICATIONS (DAC1 and DAC2)

Parameter	Min	Typ	Max	Units
RESOLUTION		8 (Fixed)		Bits
MIN OUTPUT			0.15	V
MAX OUTPUT	VDD–0.15			V
MAX CURRENT LOAD	1			mA
MAX CAPACITIVE LOAD	500			pF

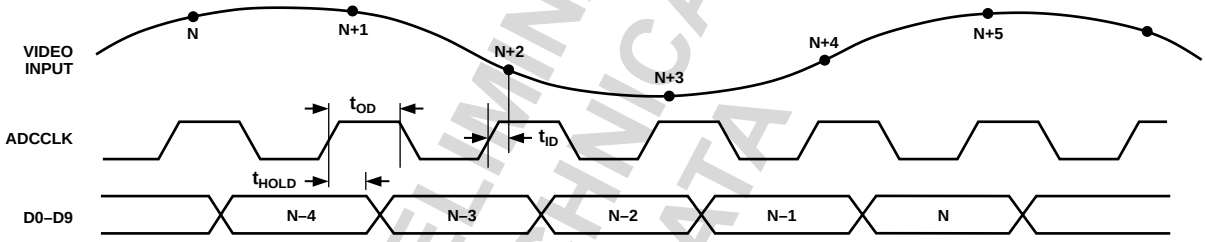
Specifications subject to change without notice.

TIMING SPECIFICATIONS



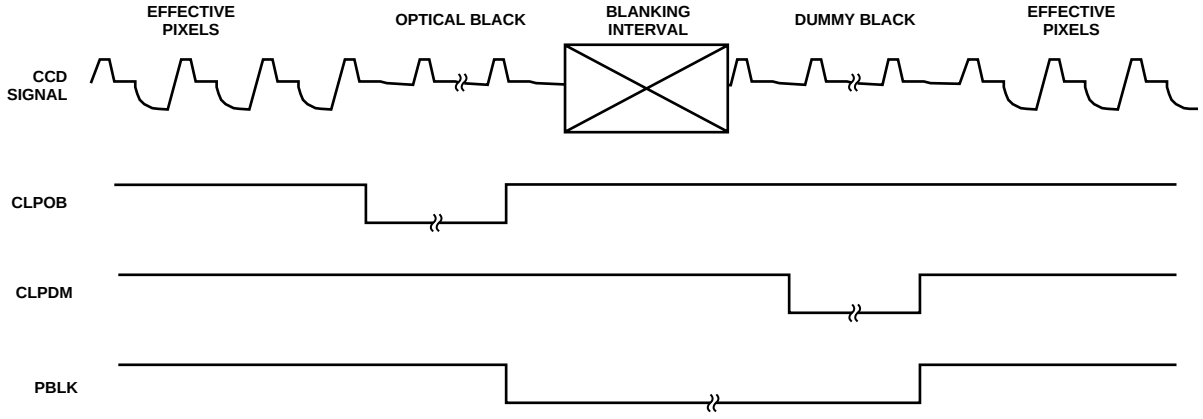
NOTES:
1. SHP AND SHD SHOULD BE OPTIMALLY ALIGNED WITH THE CCD SIGNAL. SAMPLES ARE TAKEN AT THE *RISING* EDGES.
2. ADCCLK RISING EDGE MUST OCCUR AT LEAST 15ns AFTER THE RISING EDGE OF SHP ($t_{INHIBIT}$).
3. RECOMMENDED PLACEMENT FOR ADCCLK RISING EDGE IS BETWEEN THE RISING EDGE OF SHD AND FALLING EDGE OF SHP.
4. OUTPUT LATENCY (7 CYCLES) SHOWN WITH EVEN-ODD OFFSET CORRECTION ENABLED.
5. ACTIVE LOW CLOCK PULSE MODE IS SHOWN.

Figure 1. CCD-MODE Timing



NOTE:
EXAMPLE OF OUTPUT DATA LATCHED BY ADCCLK RISING EDGE.

Figure 2. AUX-MODE and ADC-MODE Timing

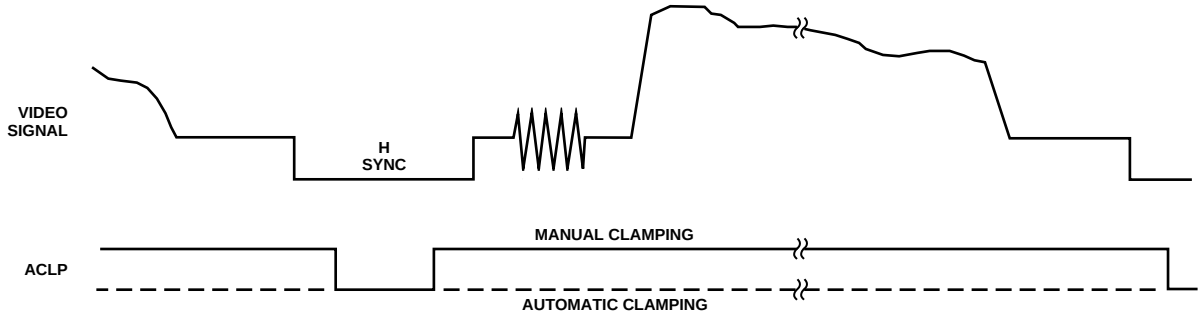


NOTES:
1. CLPOB PULSEWIDTH SHOULD BE A MINIMUM OF 10 OB PIXELS WIDE, 20 OB PIXELS ARE RECOMMENDED.
2. CLPDM PULSEWIDTH SHOULD BE AT LEAST 1 µs WIDE.
3. PBLK IS NOT REQUIRED, BUT RECOMMENDED IF THE CCD SIGNAL AMPLITUDE EXCEEDS 1V p-p.
4. CLPOB AND CLPDM OVERWRITE PBLK.
5. ACTIVE LOW CLAMP PULSE MODE IS SHOWN.

Figure 3. CCD-MODE Clamp Timing

Figure 4. AUX-MODE Clamp Timing

TIMING SPECIFICATIONS (CONTINUED)



NOTE: ACLP can be used two different ways. To control the exact time of the clamp, an active low pulse is used to specify the clamp interval. Alternatively, ACLP may be tied to ground. In this configuration, the clamp circuitry will sense the most negative portion of the signal and use this level to set the clamp voltage. For the video waveform in Figure 4, the SYNC level will be clamped to the black level specified in the E-Register. Active low clamp pulse mode is shown.

ABSOLUTE MAXIMUM RATINGS*

Parameter	With Respect To	Min	Max	Units
ADVDD	ADVSS, SUBST	–0.3	6.5	V
ACVDD	ACVSS, SUBST	–0.3	6.5	V
DVDD	DVSS	–0.3	6.5	V
DRVDD	DRVSS	–0.3	6.5	V
CLOCK INPUTS	DVSS	–0.3	DVDD + 0.3	V
PGACONT1, PGACONT2	SUBST	–0.3	ACVDD + 0.3	V
PIN, DIN	SUBST	–0.3	ACVDD + 0.3	V
DOUT	DRVSS	–0.3	DRVDD + 0.3	V
VRT, VRB	SUBST	–0.3	ADVDD + 0.3	V
CCDBYP1, CCDBYP2	SUBST	–0.3	ACVDD + 0.3	V
DAC1, DAC2	SUBST	–0.3	ADVDD + 0.3	V
DRVSS, DVSS, ACVSS, ADVSS	SUBST	–0.3	+0.3	V
Junction Temperature			+150	°C
Storage Temperature		–65	+150	°C
Lead Temperature (10 sec)			+300	°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

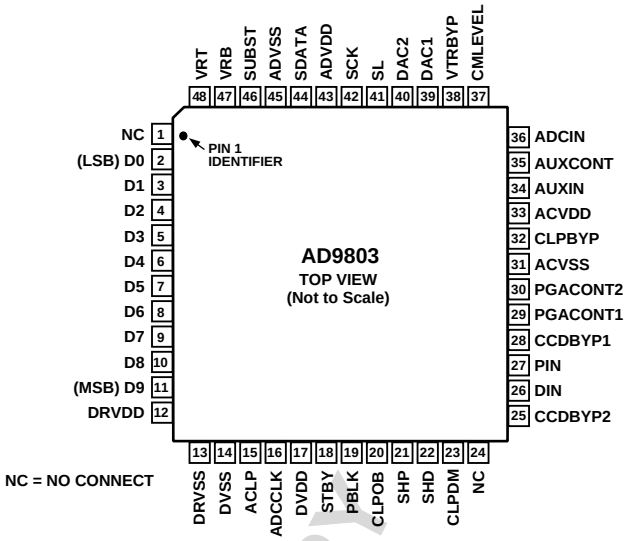
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9803JST	0°C to +70°C	48-Lead Plastic Thin Quad Flatpack	ST-48

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9803 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin #	Pin Name	Type	Description
1	NC		No Connect (Should be Left Floating or Tied to Ground)
2–11	D0–D9	DO	Digital Data Outputs
12	DRVDD	P	Digital Driver Supply (3 V)
13	DRVSS	P	Digital Driver Ground
14	DVSS	P	Digital Ground
15	ACLP	P	AUX-MODE/ADC-MODE Clamp
16	ADCCLK	DI	ADC Sample Clock Input
17	DVDD	P	Digital Supply (3 V)
18	STBY	DI	Power-Down Mode (Active Hi/Internal Pull-Down)
19	PBLK	DI	Pixel Blanking
20	CLPOB	DI	Black Level Restore Clamp
21	SHP	DI	CCD Reference Sample Clock Input
22	SHD	DI	CCD Data Sample Clock Input
23	CLPDM	DI	Input Clamp
24	NC		No Connect (Should Be Left Floating or Tied to Ground)
25	CCDBYP2	AO	CDS Ground Bypass (0.1 µF to Ground)
26	DIN	AI	CDS Negative Input (Tie to Pin 27 and AC-Couple to CCD Input Signal)
27	PIN	AI	CDS Positive Input (See Above)
28	CCDBYP1	AO	CDS Ground Bypass (0.1 µF to Ground)
29	PGACONT1	AI	PGA Coarse Gain Analog Control
30	PGACONT2	AI	PGA Fine Gain Analog Control
31	ACVSS	P	Analog Ground
32	CLPBYP	AO	Bias Bypass (0.1 µF to Ground)
33	ACVDD	P	Analog Supply (3 V)
34	AUXIN	AI	AUX-MODE Input
35	AUXCONT	AI	AUX-MODE PGA Gain Analog Control
36	ADCIN	AI	ADC-MODE Input
37	CMLEVEL	AO	Common-Mode Level (0.1 µF to Ground)
38	VTRBYP	AO	Bias Bypass (0.1 µF to Ground)
39	DAC1	AO	DAC1 Output
40	DAC2	AO	DAC2 Output
41	SL	DI	Serial I/F Load Signal
42	SCK	DI	Serial I/F Clock
43	ADVDD	P	Analog Supply (3 V)
44	SDATA	DI	Serial I/F Input Data
45	ADVSS	P	Analog Ground
46	SUBST	P	Analog Ground
47	VRB	AO	Bottom Reference (0.1 µF to Ground and 1 µF to VRT)
48	VRT	AO	Top Reference (0.1 µF to Ground)

NOTE
Type: AI = Analog Input, AO = Analog Output, DI = Digital Input, DO = Digital Output, P = Power.

SDATA / SELECT	A2	A1	A0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
MODES	0	0	1	a1	a0	b1	b0	c1	c0	d1	d0	e1	e0
				OPERATION MODES		OUTPUT MODES		CLOCK MODES		POWER DOWN MODES		CLAMP LEVEL	
PGA	0	1	0	f9	f8	f7	f6	f5	f4	f3	f2	f1	f0
				PGA GAIN LEVEL SELECTION									
DAC1	0	1	1			g7	g6	g5	g4	g3	g2	g1	g0
						DAC1 INPUT							
DAC2	1	0	0			h7	h6	h5	h4	h3	h2	h1	h0
						DAC2 INPUT							
MODES2	1	1	1							j0	k0	0	m0
										OPERATION AND POWER DOWN MODES			

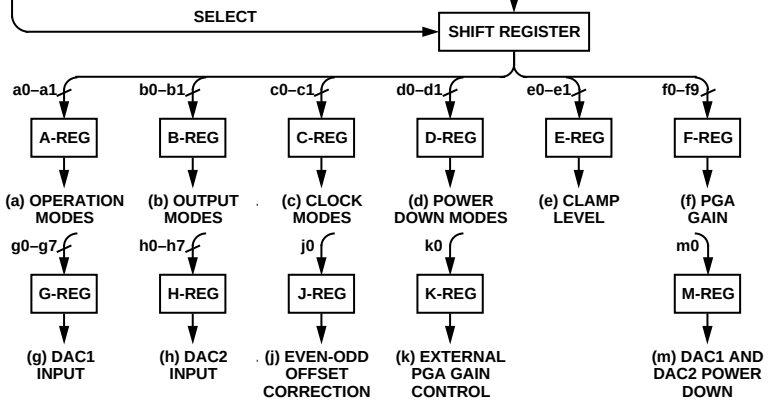


Figure 33. Internal Register Map

REGISTER DESCRIPTION

(a) A-REGISTER: Modes of Operation

a1	a0	Modes
0	0	ADC-MODE
0	1	AUX-MODE
1	0	CCD-MODE
1	1	CCD-MODE

(b) B-REGISTER: Output Modes

b1	b0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	Normal									
0	1	0	1	0	1	0	1	0	1	0	1
1	0	1	0	1	0	1	0	1	0	1	0
1	1	High Impedance									

(c) C-REGISTER: Clock Modes

c1	c0	SHP-SHD Clock Pulses	Clamp Active Pulses
0	0	Active Low	Active Low
0	1	Active Low	Active High
1	0	Active High	Active Low
1	1	Active High	Active High

(d) D-REGISTER: Power-Down Modes

Modes	d1	d0	Description
Normal	0	0	Normal Operation
Power-Down 1	0	1	Stand-By Mode (Fast Recovery)
Power-Down 2	1	0	Reference Stand-By (Same Mode as STBY Pin 18)
Power-Down 3	1	1	Total Shut-Down

(e) E-REGISTER: Clamp Level Selection

	e1	e0	Clamp Level
CLP(0)	0	0	32 LSBs
CLP(1)	0	1	48 LSBs
CLP(2)	1	0	64 LSBs
CLP(3)	1	1	16 LSBs

(f) F-REGISTER: PGA Gain Selection

	f9	f8	f7	f6	f5	f4	f3	f2	f1	f0	CCD-Gain
Gain(0)	0	0	0	0	0	0	0	0	0	0	0.00 dB
Gain(1)	0	0	0	0	0	0	0	0	0	1	0.03 dB
. . .											. . .
Gain(1022)	1	1	1	1	1	1	1	1	1	0	29.97 dB
Gain(1023)	1	1	1	1	1	1	1	1	1	1	30.0 dB

(f) F-REGISTER: PGA Gain Selection

	f9	f8	f7	f6	f5	f4	f3	f2	AUX-Gain
Gain(0)	0	0	0	0	0	0	0	0	0.00 dB
Gain(1)	0	0	0	0	0	0	0	1	0.04 dB
. . .									. . .
Gain(254)	1	1	1	1	1	1	1	0	9.96 dB
Gain(255)	1	1	1	1	1	1	1	1	10.00 dB

(g) G-REGISTER: DAC1 Input

	g7	g6	g5	g4	g3	g2	g1	g0	DAC1 Output*
Code(0)	0	0	0	0	0	0	0	0	0 V
Code(1)	0	0	0	0	0	0	0	1	0.012 V
. . .									. . .
Code(254)	1	1	1	1	1	1	1	0	2.988 V
Code(255)	1	1	1	1	1	1	1	1	3.0 V

(h) H-REGISTER: DAC2 Input

	h7	h6	h5	h4	h3	h2	h1	h0	DAC2 Output*
Code(0)	0	0	0	0	0	0	0	0	0 V
Code(1)	0	0	0	0	0	0	0	1	0.012 V
. . .									. . .
Code(254)	1	1	1	1	1	1	1	0	2.988 V
Code(255)	1	1	1	1	1	1	1	1	3.0 V

(j) J-REGISTER: Even-Odd Offset Correction

j0	Even-Odd Offset Correction
0	Offset Correction In Use
1	Offset Correction Not Used

(k) K-REGISTER: External PGA Gain Control

k0	PGA Gain Control
0	External Voltage Control Through AUXCONT or PGACONT1 and PGACONT2
1	Internal 10-Bit DAC Control of PGA Gain

(m) M-REGISTER: DAC1 & DAC2 pdn

m0	Power Down of 28-Bit DACs
0	8-Bit DACs Powered-Down
1	8-Bit DACs Operational

*VDD = 3 V

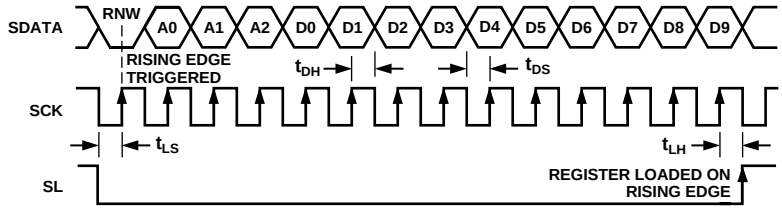


Figure 34. Serial WRITE Operation

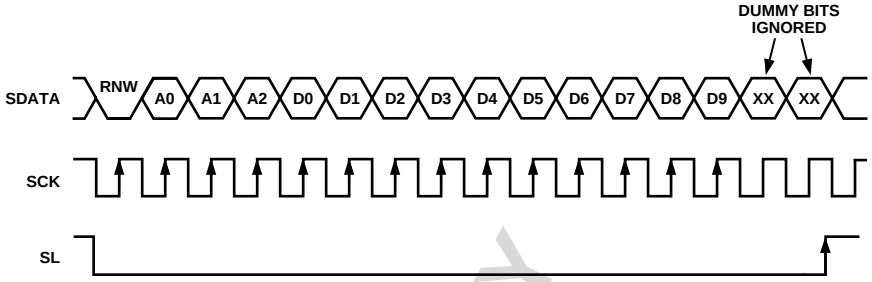


Figure 35. 16-Bit Serial WRITE Operation

NOTE**:** With the exception of a write to the PGA register during AUX-mode, all data writes must be 10 bits. During an AUX-mode write to the PGA register, only 8 bits of data are required. If more than 14 SCK rising edges are applied during a write operation, additional SCK pulses will be ignored (see Figure 35). All reads must be 10 bits to receive valid register contents. All registers default to 0s on power-up, except for the A-register, which defaults to 11. Thus, on power-up, the AD9803 defaults to CCD mode. During the power-up phase, it is recommended that SL be HIGH and SCK be LOW to prevent accidental register write operations. SDATA may be unknown. The RNW bit ("Read/Not Write") must be LOW for all write operations to the serial interface, and HIGH when reading back from the serial interface registers.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

48-Lead Plastic Thin Quad Flatpack (TQFP)
(ST-48)