Programmable high-speed decoder logic (48 × 73 × 22)

PHD48N22–7

DESCRIPTION

The PHD48N22-7 is an ultra fast Programmable High-speed Decoder featuring a 7.5ns maximum propagation delay. The architecture has been optimized using Philips Semiconductors state-of-the-art bipolar oxide isolation process coupled with titanium-tungsten fuses to achieve superior speed in any design.

The PHD48N22–7 is a two level logic element comprised of 36 fixed inputs, 73 AND gates, 10 outputs, and 12 bidirectional I/Os. This gives the device the ability to have as many as 48 inputs. Individual 3-State control of all outputs is also provided.

The device is field-programmable, enabling the user to quickly generate custom patterns using standard programming equipment. Proprietary designs can be protected by programming the security fuse.

The SLICE and SNAP software packages from Philips Components–Philips Semiconductors support easy design entry for the PHD48N22–7 as well as other PLD devices.

Order codes are listed below.

FEATURES

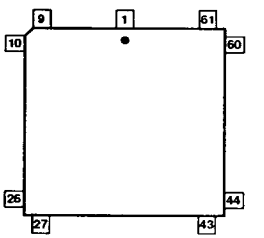
- Ideal for high speed system decoding
- Super high speed at 7.5ns t_{PD}
- 36 dedicated inputs
- 22 outputs
  - 12 bidirectional I/O
  - 10 dedicated outputs
- Security fuse to prevent duplication of proprietary designs.
- Individual 3-State control of all outputs
- Field-programmable on industry standard programmers
- Available in 68-Pin Plastic Leaded Chip Carrier (PLCC)

APPLICATIONS

- High speed memory decoders
- High speed code detectors
- Random logic
- Peripheral selectors
- Machine state decoders

PIN CONFIGURATION

A Package



A = Plastic Leaded Chip Carrier

Pin	Function	Pin	Function
1	I0	35	I29
2	I1	36	I30
3	I2	37	I31
4	V_{CC3}	38	V_{CC4}
5	I3	39	I32
6	I4	40	I33
7	I5	41	I34
8	I6	42	I35
9	I7	43	B0
10	I8	44	B1
11	I9	45	B2
12	I10	46	B3
13	I11	47	B4
14	GND5	48	GND6
15	GND1	49	GND2
16	I12	50	B5
17	I13	51	B6
18	I14	52	B7
19	I15	53	O0
20	I16	54	O1
21	V_{CC2}	55	V_{CC1}
22	I17	56	O2
23	I18	57	O3
24	I19	58	O4
25	I20	59	O5
26	I21	60	O6
27	I22	61	O7
28	I23	62	O8
29	I24	63	O9
30	I25	64	OR0
31	I26	65	OR1
32	GND3	66	GND4
33	I27	67	OR2
34	I28	68	OR3

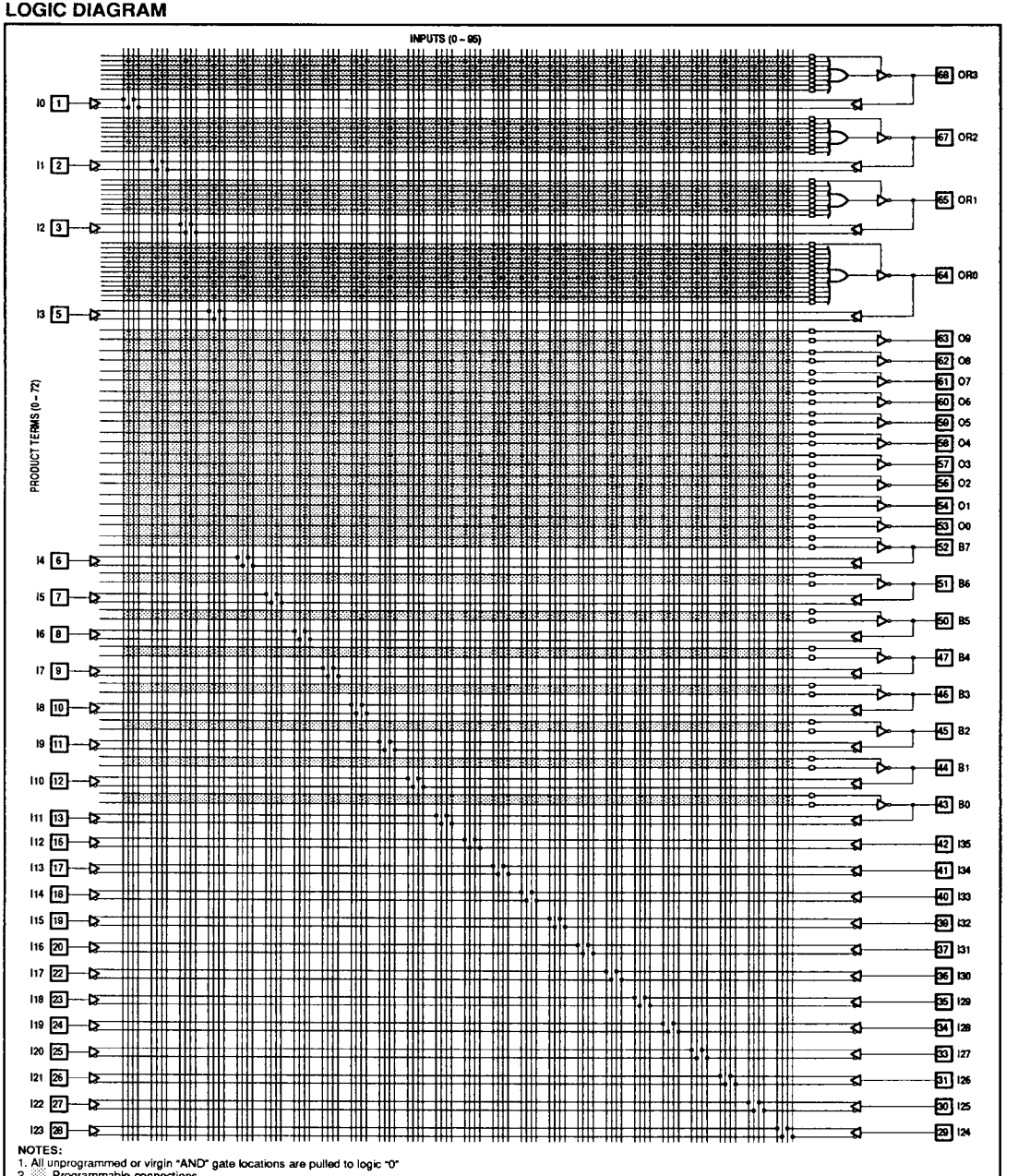
ORDERING INFORMATION

DESCRIPTION	ORDER CODE	DRAWING NUMBER
68-Pin Plastic Leaded Chip Carrier	PHD48N22–7A	0398E

Programmable high-speed decoder logic (48 × 73 × 22)

PHD48N22–7

LOGIC DIAGRAM

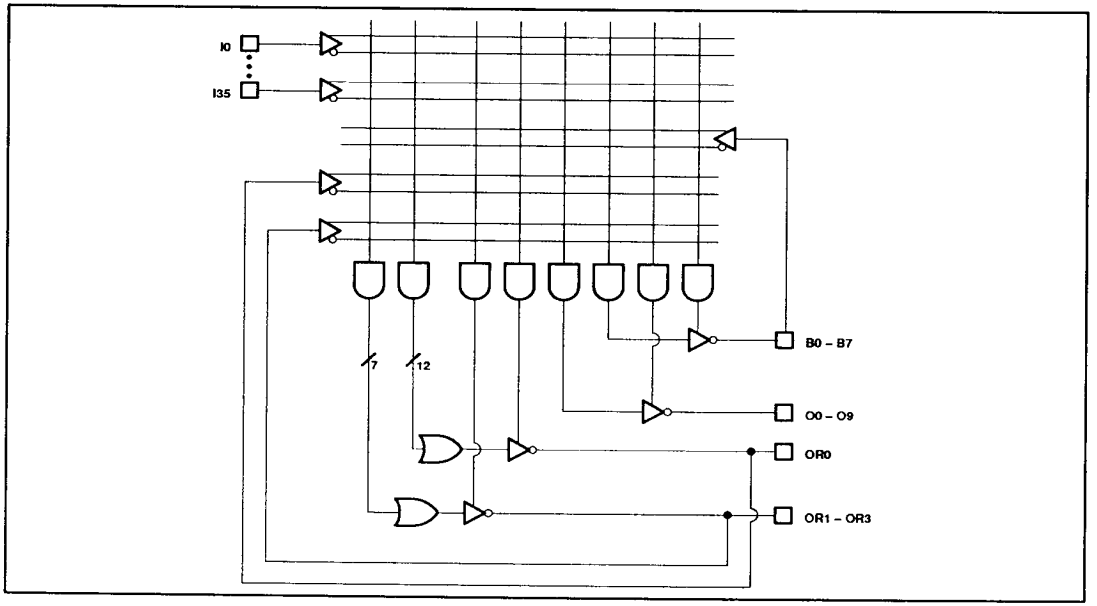


NOTES:
1. All unprogrammed or virgin "AND" gate locations are pulled to logic "0"
2. ▒ Programmable connections

Programmable high-speed decoder logic (48 × 73 × 22)

PHD48N22–7

FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS MIN	RATINGS MAX	UNIT
V_{CC}	Supply voltage	–0.5	+7	V_{DC}
V_{IN}	Input voltage	–0.5	+5.5	V_{DC}
V_{OUT}	Output voltage		+5.5	V_{DC}
I_{IN}	Input currents	–30	+30	mA
I_{OUT}	Output currents		+100	mA
T_{amb}	Operating temperature range	0	+75	°C
T_{stg}	Storage temperature range	–65	+150	°C

NOTES:
1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

OPERATING RANGES

SYMBOL	PARAMETER	RATINGS MIN	RATINGS MAX	UNIT
V_{CC}	Supply voltage	+4.75	+5.25	V_{DC}
T_{amb}	Operating free-air temperature	0	+75	°C

DC ELECTRICAL CHARACTERISTICS

$0°C \leq T_{amb} \leq +75°C$, $4.75 \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP[1]	MAX	
Input voltage[2]						
V_{IL}	Low	V_{CC} = MIN			0.8	V
V_{IH}	High	V_{CC} = MAX	2.0			V
V_{IC}	Clamp	V_{CC} = MIN, I_{IN} = –18mA		–0.8	–1.5	V
Output voltage						
		V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}				
V_{OL}	Low	I_{OL} = +24mA			0.5	V
V_{OH}	High	I_{OH} = –3.2mA	2.4			V
Input current						
		V_{CC} = MAX				
I_{IL}	Low	V_{IN} = +0.40V		–20	–250	µA
I_{IH}	High	V_{IN} = +2.7V			25	µA
I_I	High	V_{IN} = V_{CC} = $V_{CC\ MAX}$			100	µA
Output current						
		V_{CC} = MAX				
I_{OZH}	Output leakage [3]	V_{OUT} = +2.7V			100	µA
I_{OZL}	Output leakage [3]	V_{OUT} = +0.40V			–100	µA
I_{OS}	Short circuit [4]	V_{OUT} = +0V	–30	–60	–90	mA
I_{CC}	V_{CC} current	V_{CC} = MAX			420	mA
Capacitance[5]						
		V_{CC} = +5V				
C_{IN}	Input	V_{IN} = 2.0V @ f = 1MHz		8		pF
C_{OUT}	I/O	V_{OUT} = 2.0V @ f = 1MHz		8		pF

NOTES:
1. Typical limits are at V_{CC} = 5.0V and T_{amb} = +25°C.
2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3. Leakage current for bidirectional pins is the worst case of I_{IL} and I_{OZL} or I_{IH} and I_{OZL}.
4. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second.
5. These parameters are not 100% tested, but are periodically sampled.

AC ELECTRICAL CHARACTERISTICS

$0°C \leq T_{amb} \leq +75°C$, $4.75 \leq V_{CC} \leq 5.25V$, $R_1 = 200\Omega$, $R_2 = 390\Omega$
Operating temerature at 200 CFM Minimum air flow.

SYMBOL	PARAMETER	FROM	TO	TEST CONDITIONS	LIMITS MIN	LIMITS MIN	UNIT
t_{PD1}[1]	Propagation delay through B/O outputs	(I, B, OR) ±	Output ±	C_L = 50pF		7.5	ns
t_{PD2}[1]	Propagation delay through OR outputs	(I, B, OR) ±	Output ±	C_L = 50pF		8.0	ns
t_{OE}[2]	Output Enable	(I, B, OR) ±	Output enable	C_L = 50pF		10	ns
t_{OD}[2]	Output Disable	(I, B, OR) ±	Output disable	C_L = 5pF		10	ns

NOTES:
1. $t_{PD1, 2}$ are tested with switch S_1 closed and C_L = 50pF.
2. For 3-State output; output enable times are tested with C_L = 50pF to the 1.5V level, and S_1 is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with C_L = 5pF. High-to-High impedance tests are made to an output voltage of $V_T = (V_{OH} - 0.5V)$ with S_1 open, and Low-to-High impedance tests are made to the $V_T = (V_{OL} + 0.5V)$ level with S_1 closed.

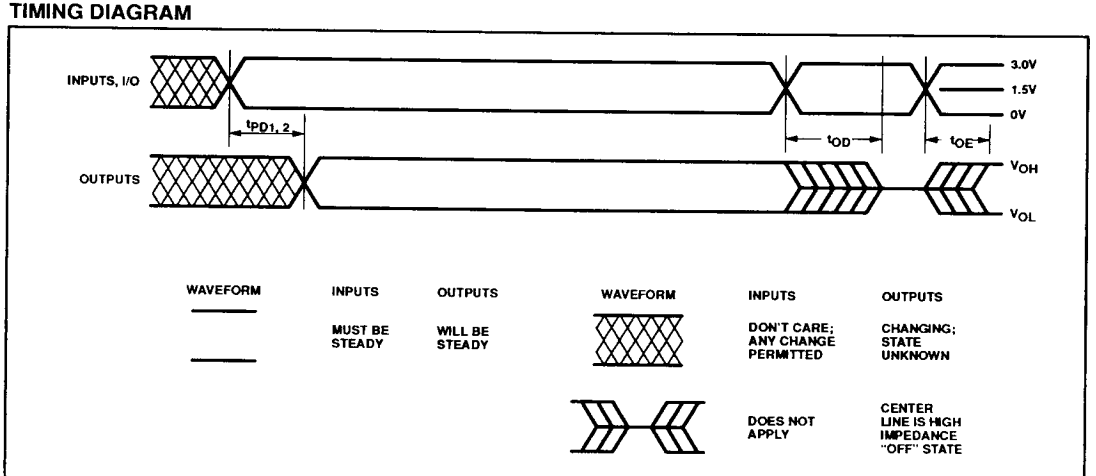
VIRGIN STATE

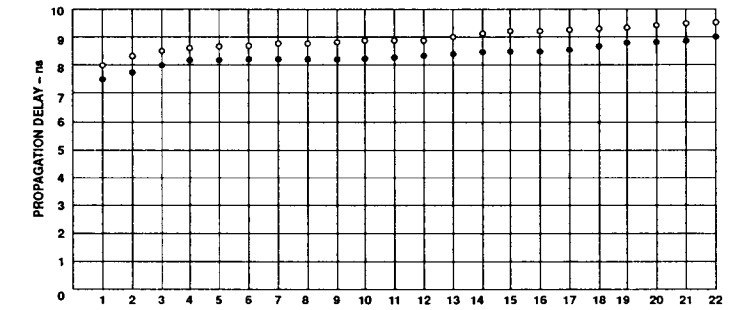
A factory shipped virgin device contains all fusible links intact, such that:
1. All outputs are disabled.
2. All p-terms are disabled in the AND array.

TIMING DEFINITIONS

SYMBOL	PARAMETER
t_{PD1}	Input to output propagation delay (through B/O outputs).
t_{PD2}	Input to output propagation delay (through OR outputs).
t_{OD}	Input to Output Disable (3-State) delay (Output Disable).
t_{OE}	Input to Output Enable delay (Output Enable).

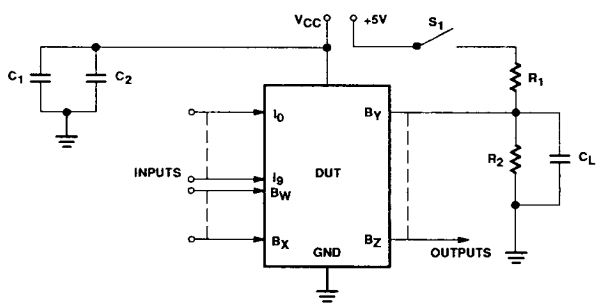
TIMING DIAGRAM





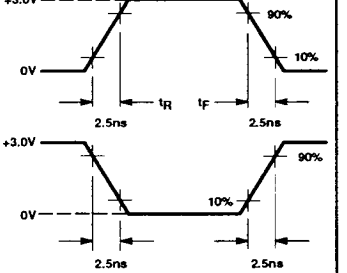
Worst-Case Propagation Delay vs. Number of Outputs Switching

AC TEST LOAD CIRCUIT



NOTE:
C_1 and C_2 are to bypass V_{CC} to GND.

VOLTAGE WAVEFORMS



MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

Programmable high-speed decoder logic (48 × 73 × 22) — PHD48N22–7

LOGIC PROGRAMMING

The PHD48N22–7 is fully supported by industry standard (JEDEC compatible) PLD CAD tools, including Philips Semiconductors SNAP design software package. ABEL™ and CUPL™ 90 design software packages also support the architecture.

All packages allow Boolean and state equation entry formats. SNAP, ABEL and CUPL also accept, as input, schematic capture format.

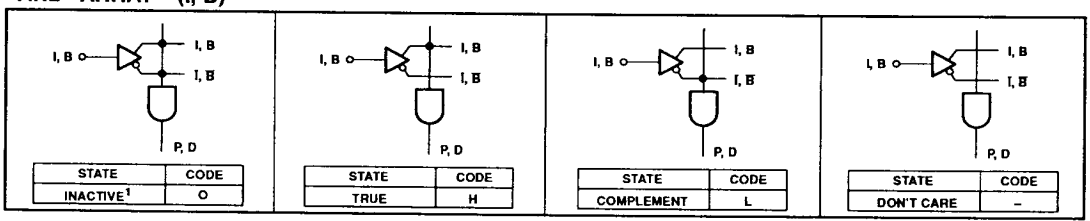
PHD48N22–7 logic designs can also be generated using the program table entry format, which is detailed on the following pages. This program table entry format is supported by SNAP only.

To implement the desired logic functions, each logic variable (I, B, P and D) from the logic equations is assigned a symbol. TRUE (High), COMPLEMENT (Low), DON'T CARE and INACTIVE symbols are defined below.

PROGRAMMING/SOFTWARE SUPPORT

Refer to Section 9 *(Development Software)* and Section 10 *(Third-Party Programmer/ Software Support)* of this data handbook for additional information.

"AND" ARRAY – (I, B)



STATE	CODE
INACTIVE[1]	O

STATE	CODE
TRUE	H

STATE	CODE
COMPLEMENT	L

STATE	CODE
DON'T CARE	–

NOTE:
1. This is the initial state.

ABEL is a trademark of Data I/O Corp.
CUPL is a trademark of Logical Devices, Inc.

Programmable high-speed decoder logic (48 × 73 × 22)

PHD48N22–7

PROGRAM TABLE

TERM	INPUTS																																															
	I																																				B								OR			
	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	3	2	1	0
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VARIABLE NAME																																																

PROGRAM TABLE (Continued)

TERM	OUTPUTS																			
	O										B								OR			
	9	8	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	3	2	1	0
0																			D			
1																			A			
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72																		A				
PIN	63	62	61	60	59	58	57	56	54	53	52	51	50	47	46	45	44	43	68	67	65	64
VARIABLE NAME																						

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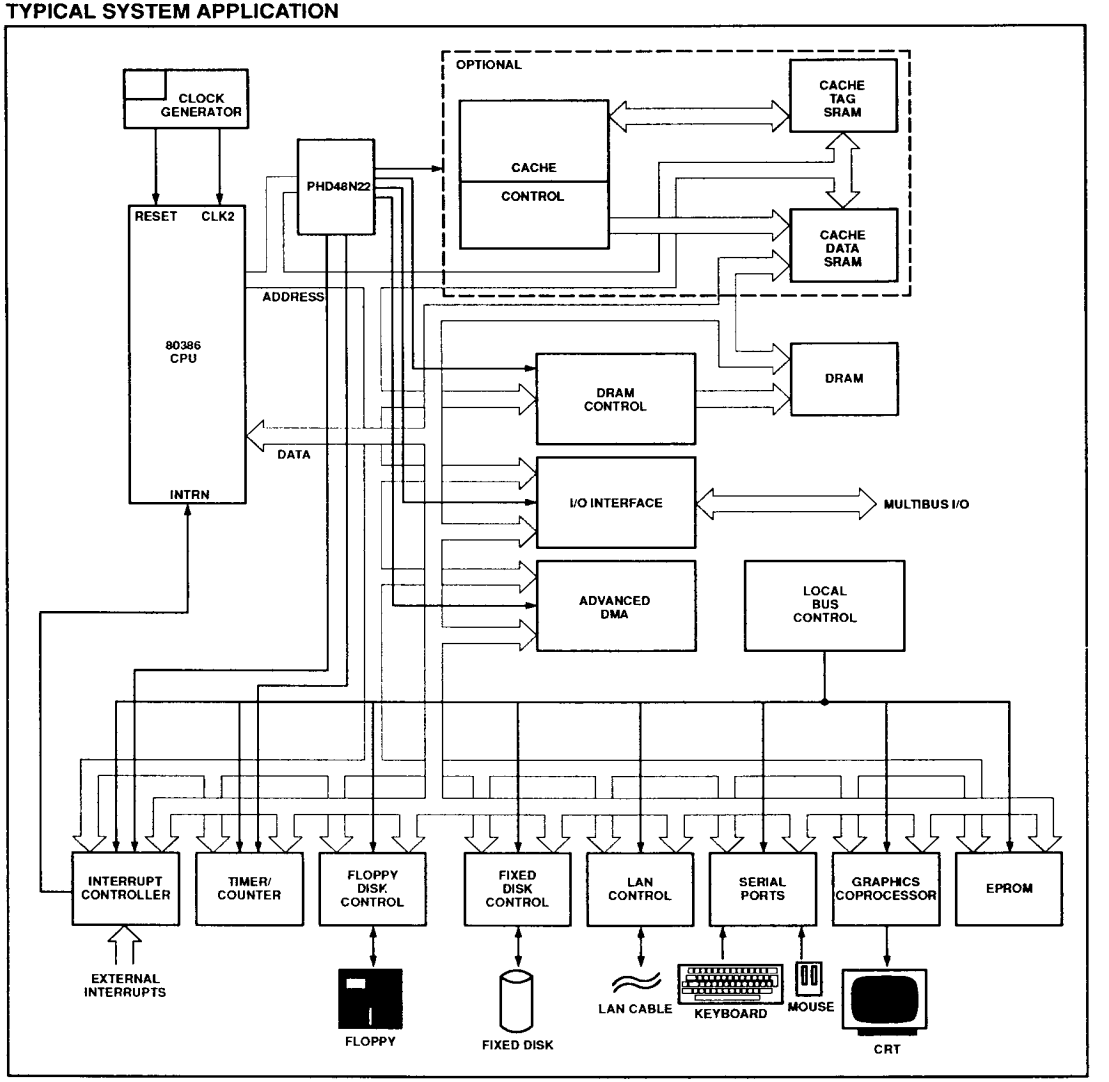
TYPICAL SYSTEM APPLICATION



SNAP RESOURCE SUMMARY DESIGNATIONS