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data sheet

29C53
DIGITAL LOOP CONTROLLER

ADVANCE INFORMATION

JANUARY 1986

- 4-Wire Full Duplex Digital Transceiver
- CCITT I.430 "S" Interface Compatible
- ISDN Basic Rate 144K Bit Per Second
- D-Channel Processing Support
- Point-To-Point or Point-To-Multipoint Bus Configuration
- Same Device Used at Both Ends of Loop
- Exceeds 1K Meter Range
- IATC Standard SLD Interface
- MCS Standard Microprocessor Interface
- Peripheral Interface/Status Port
- Low Power, High Density CHMOS
- Single + 5 Volt Supply

Description

The 29C53 Digital loop Controller (DLC) is a 4-wire transceiver/controller that is CCITT I.430 compatible and can function at either loop end. This part has integrated those features which are pertinent to the transceiver function ; yet it offers efficient interfacing to other system components such as combos, line card controllers and microcontrollers through the SLD and microprocessor interface ports. It is primarily intended for use in Integrated Services Digital Networks (ISDN) as a basic rate digital data transceiver which transfers data at 144 Kbps as three separate channels — two 64 Kbps digitized-voice/data channels (B-channels), and a 16 Kbps signaling/data channel (D-channel). The B- and D-channel routing along with D-channel processing (packetization) is programmable through either the microprocessor or SLD interface ports. The 29C53's loop interface uses a 100 % pulse-width pseudo-ternary inverted line code similar to Alternate Mark Inversion, which meets CCITT's "S" interface recommendations. It is capable of interfacing with up to eight 29C53s in a passive or extended bus configuration as well as point-to-point.

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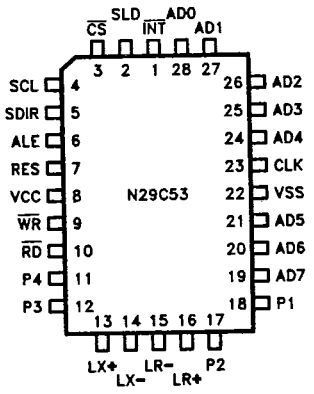
Plastic Chip Carrier
350 x 550 MILS



28-Lead Dual-In-Line Package

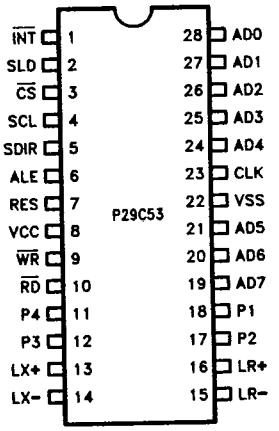


Figure 1. 29C53 Pin Configurations

29C53

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Symbol	Pin No.	Function
V_{CC}	8	**POSITIVE SUPPLY:** Input voltage is +5V ±5%.
V_{SS}	22	**GROUND:** 0V
CLK	23	**MASTER CLOCK:** The 3.84 MHz system clock input is the reference for the loop and the SLD interface.
RES	7	**RESET:** (Active high input). A high level on this pin initializes most control registers and places most interface outputs in a high impedance state. Operation begins when the high level is removed.
LX^+, LX^-	13, 14	**POLARIZED TRANSMIT LOOP INTERFACE PINS:** These pins will directly drive the twisted pair line through a 2.5:1 line transformer. The transmitted line code is similar to alternate mark inversion.
LR^-, LR^+	15, 16	**RECEIVE LOOP INTERFACE PINS :** The receiver is not sensitive to polarity.
SLD	2	**SUBSCRIBER LINE DATALINK :** This pin transfers serial data between the 29C53 and other SLD based components (e.g. 29C48, 2952, 29C55, etc.).
SCL	4	**SUBSCRIBER CLOCK:** 512 KHz signal may be either generated or received by the 29C53. This signal clocks the data on the SLD pin.
SDIR	5	**SUBSCRIBER DIRECTION:** An 8 KHz signal may be either generated or received by the 29C53 to indicate SLD data direction and framing. A high level indicates and enables master to slave transfer; a low level indicates slave to master transfers.
$\overline{CS}$	3	**CHIP SELECT:** (Active low input). A low level on this pin enables the 29C53 bus interface for the next bus cycle. The value is latched by the falling edge of ALE.
$\overline{RD}$	10	**READ STROBE:** (Active low input). When low, data is transferred from the selected register to the data pins AD (0–7). When no local microprocessor is connected, this pin should be tied to V_{SS}.
$\overline{WR}$	9	**WRITE STROBE:** (Active low input). When $\overline{WR}$ changes from low to high, data on pins AD (0–7) is latched into the 29C53. When no local microprocessor is connected, this pin should be tied to V_{SS}.
AD (0–7)	19–21, 24–28	**ADDRESS/DATA PINS:** This is a standard MCS microprocessor bus used to transfer address and data between the local microprocessor and the internal registers of the 29C53. When a local microprocessor is not used, these pins should be tied to V_{SS}.
ALE	6	**ADDRESS LATCH ENABLE:** Address is latched from AD(0–7) on falling edge of this signal. State of $\overline{CS}$ is also latched at this time.
$\overline{INT}$	1	**INTERRUPT REQUEST:** This is an open drain active low output. (See text for the interrupt conditions.)
P1, P2	18, 17	**PERIPHERAL INTERFACE INPUTS :** These are standard CHMOS high impedance inputs that are sampled at a 4 KHz rate (once per "S" frame). The sampled data is stored in the LPS register (bits 5 and 6). If any peripheral input bits have changed value since the previous frame, an interrupt condition is indicated; only present status is available.
P3	12	**PERIPHERAL INTERFACE INPUT/OUTPUT PIN:** When configured as an input, this pin has the same characteristics as P1 and P2. The sampled data is stored in the LPS register (bit 7). When programmed as an output, this pin outputs the data stored in the PEC register (bit 1). The pin is configured by bit 2 of the PEC register. An alternate function of this pin and P4 is to indicate the status of the SLD interface. See the section on the SLD interface.
P4	11	**PERIPHERAL INTERFACE OUTPUT PIN:** This pin outputs data stored in the PEC register (bit 0) or SLD status.

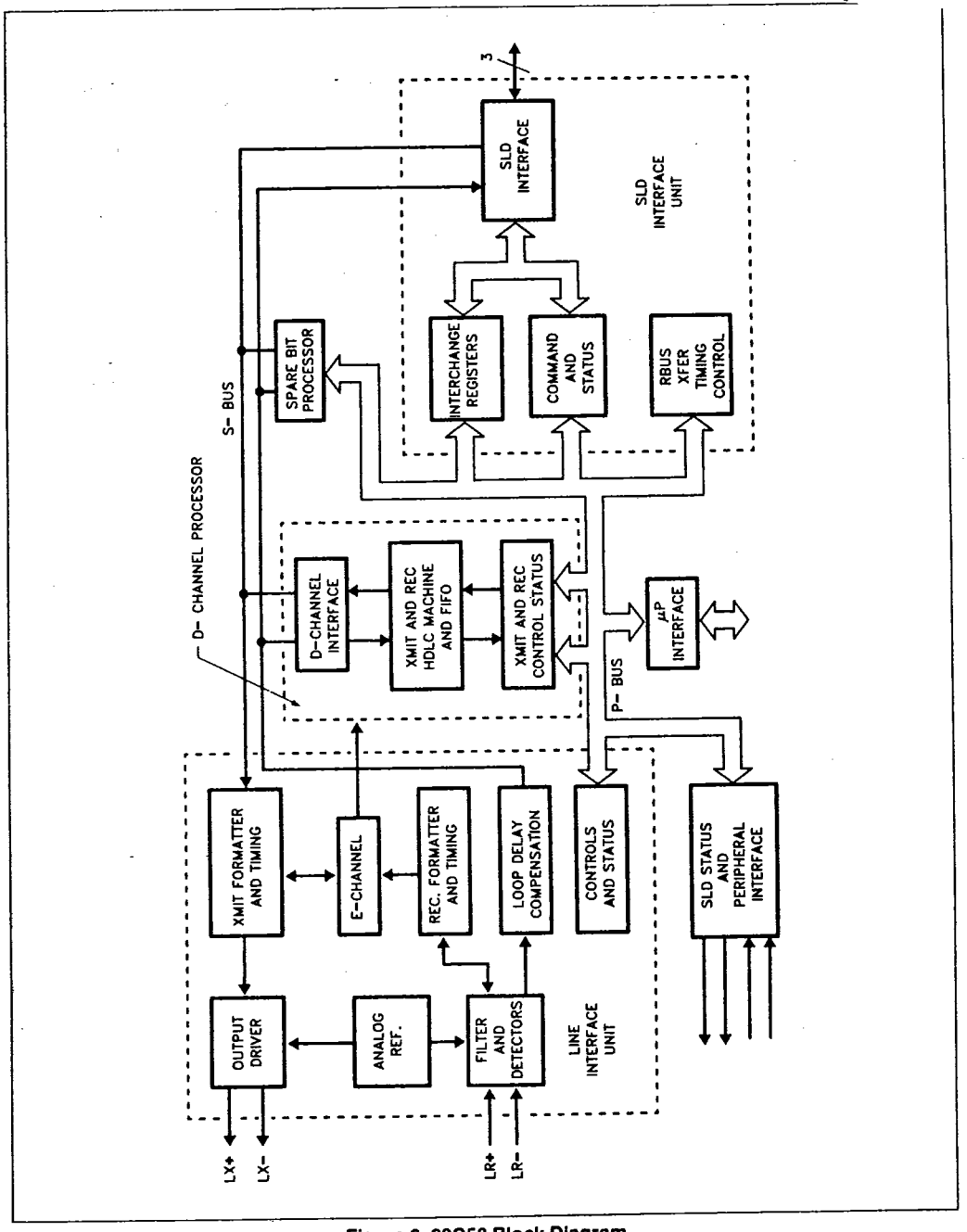

Figure 2. 29C53 Block Diagram

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29C53 FUNCTIONAL DESCRIPTION

The 29C53 Digital Loop Controller is a multi-channel ISDN transceiver which provides a multiplicity of advanced communication functions and services. The 29C53 allows the extension of digital voice and data directly to subscriber equipment over a 192 Kbps baseband 4-wire serial interface. The 29C53 is a 28-pin device which, when used with the 29C48, 2952 and a microprocessor implements flexible point-to-point or point-to-multipoint CCITT I.430 compatible voice/data communications. It is primarily intended for use in PBX's and ISDN terminal equipment.

The 29C53 may be incorporated at either end of a subscriber loop interface (at the line card or digital telephone/terminal). As shown in Figure 2, the 29C53 has four separate interfaces : a serial SLD system interface ; a parallel peripheral interface ; a parallel microprocessor interface and a 4-wire CCITT compatible S-interface (subscriber loop interface).

THE BLOCK DIAGRAM

Figure 2 represents a block diagram of the 29C53. Its three major blocks, the line interface unit, the D-channel processor and the SLD interface unit are interconnected by two buses. The parallel bus (P-bus) is used to transfer processed D-channel data and general status and control information while the serial bus (S-bus) is used to transfer B-channel data and unprocessed D-channel data between the line interface unit and the SLD interface unit.

The SLD interface unit consists of shift registers and serial to parallel converters. Data from both the S-bus and the SLD interface is stored here in appropriate parallel registers before it is loaded into shift registers and passed on. All of the timing circuitry for the SLD interface is located here. This block also contains a command processor which is responsible for controlling the functionality of the chip.

The D-channel processor has three major sections. An HDLC section performs some of the basic LAPD protocol functions such as zero insertion or deletion, flag recognition or insertion for frame delineation, abort flag recognition, idle state transmission, and end of packet frame check sequence for both data directions. The FIFO section consists of two 32-byte buffers, one for transmit and one for receive. The control and status section monitors the FIFO data levels and the HDLC section for progress. Interrupts or requests for service may be generated for conditions such as a full or empty FIFO, loss of sync, frame check error, overflows and aborts.

The line interface unit contains the line drivers and receivers for the S interface. Connection is made to the transmission lines through a 2.5:1 line transformer. Formatting, timing and synchronization are also provided here. The receiver includes filters, AGC circuitry, threshold detectors and a loop delay shift register. The loop delay shift register maintains the proper internal frame relationship regardless of loop length (it allows extra propagation delay time for long loops or line repeaters). The received D-channel bits are logically looped back to create the E-channel bits in an NT application through the E-channel circuitry.

The microprocessor interface circuitry allows the 29C53 to function as a peripheral to a microcontroller. The internal P-bus actually becomes an extension of the microcontroller's bus. All internal registers are directly accessible.

The spare bits processing block provides access to all the miscellaneous bits in the S frame except for the framing bits and the balance bits. When spare bit functions become defined, they can be easily monitored and modified.

The peripheral interface circuitry provides an auxiliary port for controlling auxiliary peripherals such as power controllers, etc.

SLD INTERFACE

The SLD interface provides half-duplex 512 Kbps communication with other devices incorporating SLD interfaces (such as line card controllers and codec/filters). Of the 256 Kbps in each direction, 128 Kbps is dedicated to voice/data channels B1 and B2. The remaining bandwidth is used for the D-channel data and various control and status transfers depending on the exact application.

As shown in Figure 3, the SLD interface consists of three lines : the SLD bidirectional data line, the 512KHz SCL clock line ; and the 8 KHz data direction line. SLD data is updated on the rising edge of SCL and is latched on its falling edge. The 125 µs SLD frame period consists of 32 bits transferred in master to slave direction followed by 32 bits in the slave to master direction. The 32 bits compose four 8-bit bytes in the following order: B1 and B2 (voice or data bytes); C (control byte); and S (signaling or status byte). Unprocessed D-channel data may be transported over the S-byte in bits 0 and 1, or over the B2 byte.

The 29C53 can be operated as an SLD master or slave. As an SLD master, it generates the SCL and SDIR signals. When SDIR is high, the SLD pin outputs data. As a slave, it receives SCL and SDIR sig-

nals and SDIR enables the SLD output driver when it is low. The SLD bus is always active; no powered-down or inactive mode is defined.

In a network termination (NT) application (line card), whether a microprocessor is connected to the 29C53 or not, the SLD control and signal bytes may be used for 29C53 configuration and D-channel transfers. The command bytes are interpreted and executed by the 29C53's command processor circuit. The command processor generates internal P-bus cycles to carry out those commands. Internal prioritization resolves P-bus collisions between microprocessor-interface generated and command-processor generated cycles. In case of collisions, the microprocessor interface has higher priority to minimize access time but both cycles will be completed.

"S" TRANSCEIVER

The 4-wire "S" transceiver circuit in the 29C53 conforms to CCITT recommendation. I.430. This transceiver provides the internal drivers for transformer coupling to standard telephone type twisted pair cables.

The "S" transceiver line code is 100% Pseudo-Ternary Inverted code which is similar to Alternate Mark Inversion, except that logical ones are transmitted as spaces, logical zeros as marks. A space has a nominal differential voltage of zero volts. Marks may be either positive or negative differential signals, nominally 0.75 volts in amplitude. Marks alternate polarity except when a "code violation" is created for establishing frame reference timing.

The nominal bit rate is 192 Kbps. Figure 4 shows the frame structure. The 250 μs frame transfers two octets of B1, B2 and four bits of D data. The E bits in the master to slave direction, echo received D-channel data. The "S" interface slave compares the receive E-channel data to its transmitted D-channel data for D-channel contention as defined in CCITT recommendation I.440. If these bits do not agree, then the slave will abort its transmission effort. The S, FA, and N bits are all accessible and programmable.

The activation protocol described in I.430 is supported by the 29C53. An inactive receiver can achieve bit synchronization to an incoming signal with approximately 30 mark-mark transitions. Info 2 or 3 frame alignment is not officially recognized until reception of 16 frames, to allow settling of the 29C53's adaptive receive data thresholds. The full activation sequence will complete in approximately 10 ms.

The 29C53 is not sensitive to the polarity of the wire pair connected to LR^+ and LR^-. Marks are always interpreted as zeros and framing relies on violations; not on absolute polarity. System configurations may dictate that care be taken in connecting the LX outputs. In a multi-drop bus configuration all TE transmitters must be connected with the same polarity so that positive mark to negative mark contention does not take place in the framing and D-channel bits.

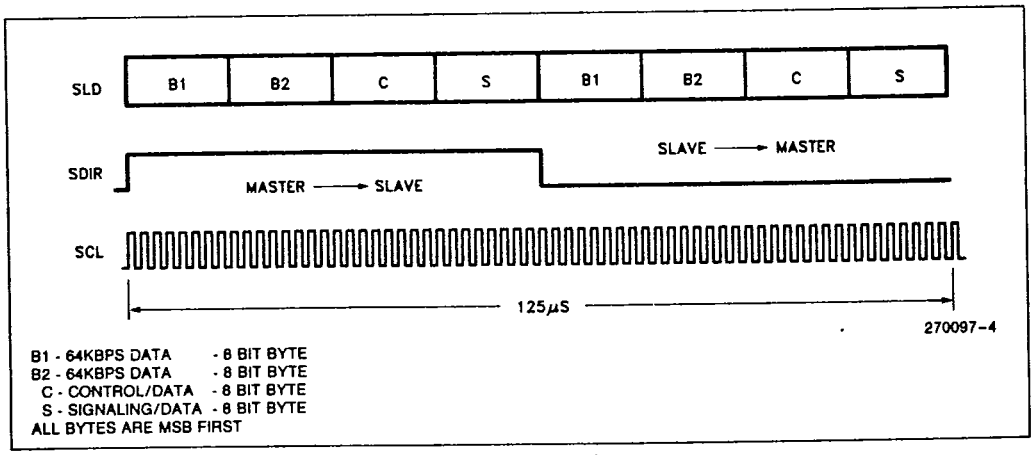


Figure 3. SLD Interface

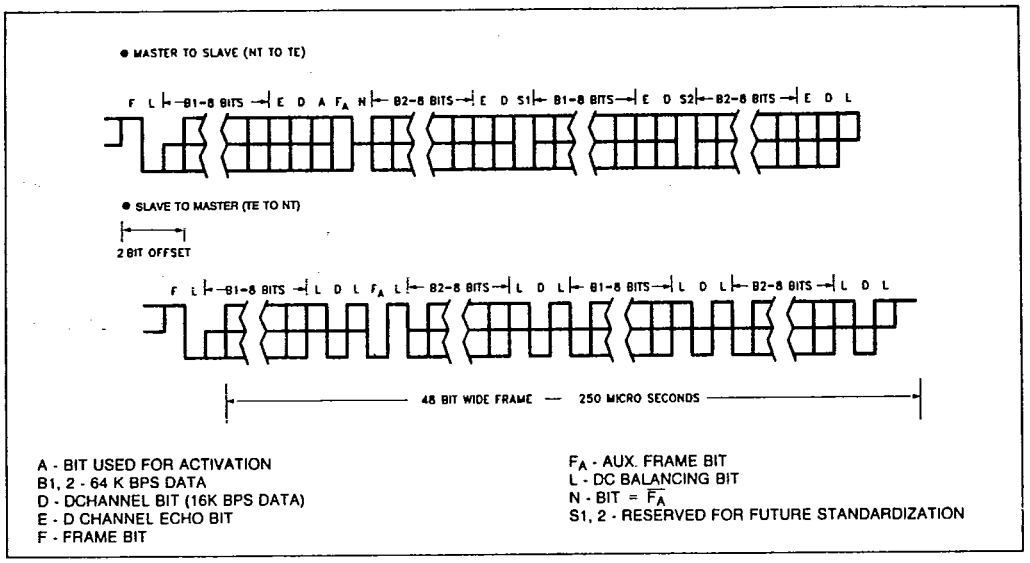


Figure 4. The S-Interface Frame Structure

The 29C53, functioning as an "S" interface master in a multi-drop application, can interface with up to eight slave systems. In this multiplexing operation a slave initiates a data transfer to the master, by requesting access and transferring the data in accordance with the D-channel line access protocol (I.440). Figure 5 shows typical applications of the 29C53.

The frame alignment timing diagram Figure 6(b) shows the relationship of the "S" interface data to the SLD data. Figure 6(a) shows the block diagram used for the timing diagram. The top timing diagram shows the transmitted "S" data stream from the network terminator (master). The dotted lines depict up to 20 μs propagation delay to the "S" receiver at the terminal equipment (slave) end. The terminal equipment's transmitted "S" interface frame is designed to have a fixed 2-bit frame alignment delay from that of its received frame. The adjustment for loop propagation delay is accounted for in the network terminator's receive circuitry (loop delay section of block diagram). The loop delay circuitry will compensate for up to 10 bit periods of round trip propagation delay which allows line repeaters to be placed in a loop that is several thousand meters long.

MICROPROCESSOR INTERFACE

This interface is designed to operate with standard 8-bit microprocessors such as the 8051, 8086 and 8088 families. All of the 29C53's internal registers are accessible and most are available by a single microprocessor cycle access.

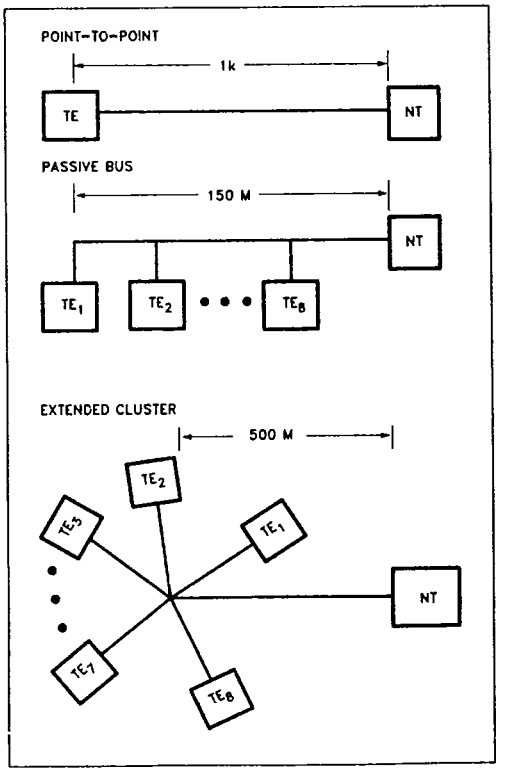


Figure 5. 29C53 Bus Configurations

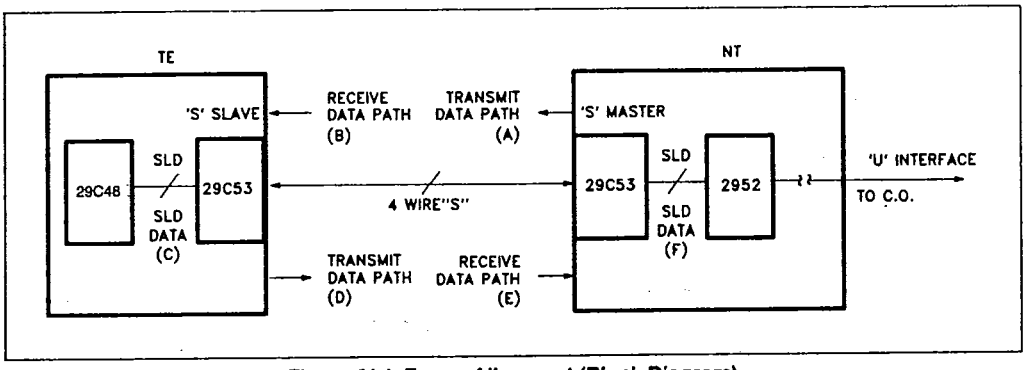


Figure 6(a). Frame Alignment (Block Diagram)

The maskable interrupt pin, on this port, is activated by the following interrupt status features: D-channel errors; loss of sync on "S" loop; change in spare bits or peripheral interface data; FIFO data transfer requests.

Alternatively, the 29C53 can operate in the stand-alone mode in line card and NT applications. This mode is determined on a power-up condition or after a reset, provided all the microprocessor interface pins have been tied to V_{SS}, except for the interrupt pin.

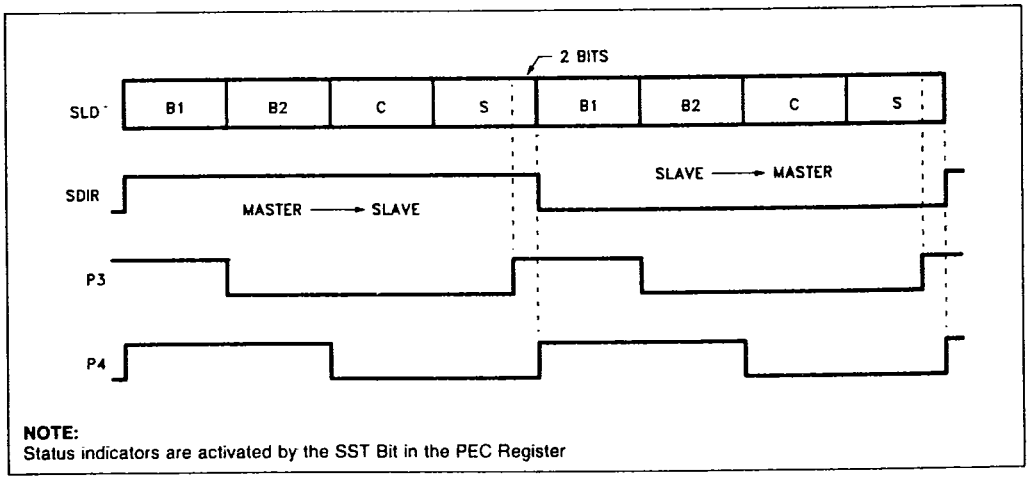
PERIPHERAL INTERFACE

The peripheral interface uses four pins to provide control to, and to accept status from, external devices. Two pins are inputs, one is an output and one is configurable either as an input or an output. The configurable pin defaults to the input mode on power up.

The peripheral interface can also be used to indicate SLD status. Figure 7 shows the timing diagram of P3 and P4. B1, B2 and D-channel data on the SLD pin can be selected or gated by using these signals. As noted on the P3 timing, the D-channel is imbedded in the last two bits (0, 1) of the signaling byte.

INTERNAL CONTROL AND STATUS REGISTERS

All of the 29C53's internal control and status registers may be accessed through the microprocessor interface or through the SLD interface. When a microprocessor accesses a register, the address and CS inputs are latched on the trailing edge of ALE.



NOTE:
Status indicators are activated by the SST Bit in the PEC Register

Figure 7. 29C53 SLD Status Indicators

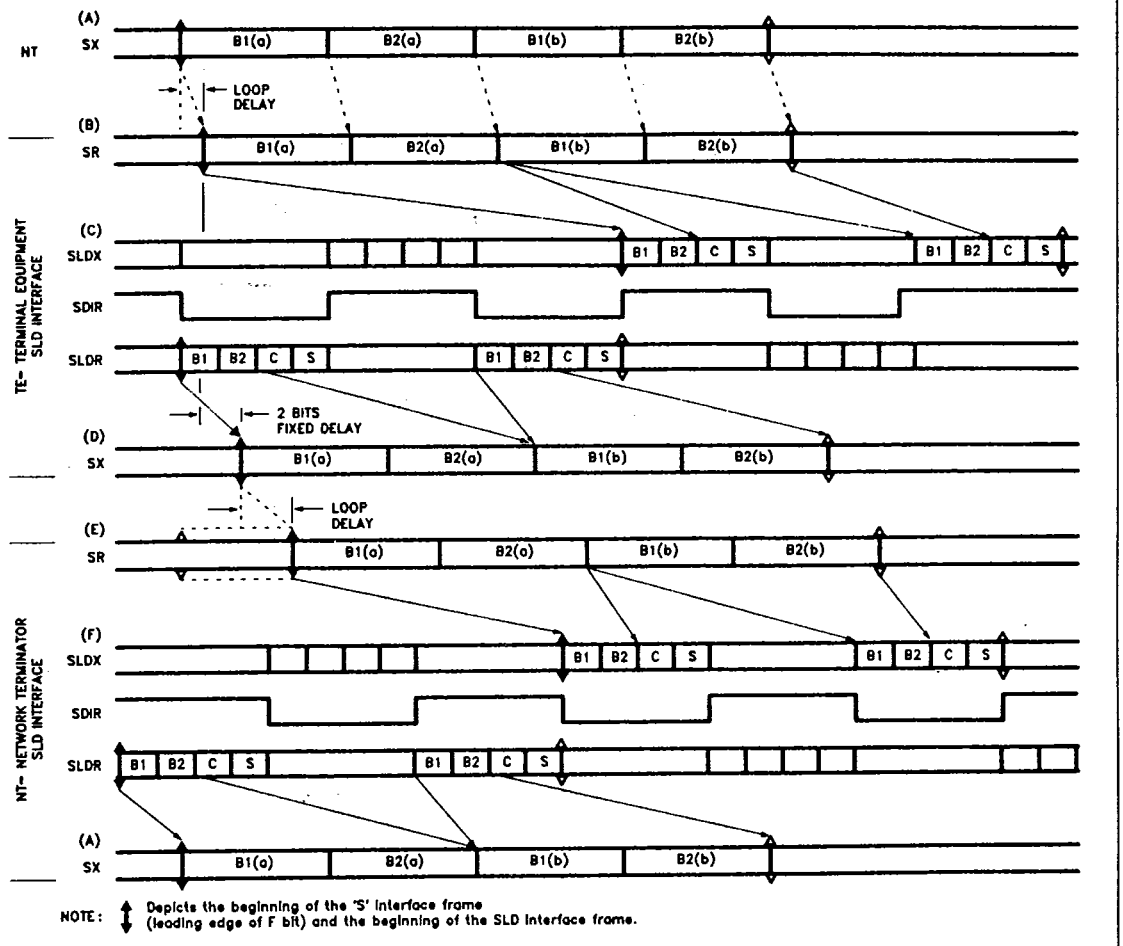


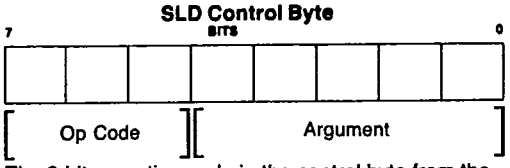
Figure 6(b). Frame Alignment (Timing Diagram)

Op Code Table

OpCode	Operation	Argument
000	Reserved For Status Poll (Call Verify) By Master	—
001	Single Byte Transfer To Slave	Reg Adr
010	Prepare Single Byte For Transfer To Master	Reg Adr
011	Multiple-Byte D Data Transfer To Slave	#Bytes
100	Multiple-Byte D Data Transfer To Master	Max # Bytes
101	Multiple-Byte Configuration Transfer To Slave	# Bytes
110	Multiple-Byte Status Transfer To Master	# Bytes
111	Reserved For Status Poll (Call Verify) Tail & Idle	—

In an SLD access, the 29C53 receives a control byte containing an operation code and an argument. The three most significant bits contain the operation code and the remaining five bits contain the argument. The operation code defines eight transfer types.

SLD Control Byte



The 3-bit operation code in the control byte from the line card controller should normally be 111, indicating the idle state. The transferring of data to and from the 29C53 is accomplished by indicating the type and the number of bytes to transfer in a non-idle control byte. When a polled response is requested, the 29C53 responds to the poll operation code 000. This can be used for the transfer of one or several bytes of information.

The register table below identifies the address of each 29C53 register. The status registers are read-only registers while all control registers are read/write registers. Because all the register addresses do not fit into the 5-bit address space, a register test mode has been included which permits reading the contents of control registers at addresses which normally are status registers. Where no register is assigned a location in the register test mode, the normal status register located at this address is read.

The D-channel block transfers from the 29C53 to the line card controller preface the data bytes with a byte header specifying the number of following bytes (less than or equal to the maximum specified) and the status of the packet they belong to. All transferred data bytes belong to the same packet; the transfers occur until the selected number of bytes are transferred or an EOP (end of packet) is detected. The EOP may occur even when there are additional bytes in the FIFO. The header byte contains the byte count in the lowest five bits and the status in the upper three bits.

Data transfers within the 29C53 cannot be made in both directions simultaneously. Multiple commands and data bytes may follow each other directly from the line card controller to the 29C53 if the previous command has been fully executed.

It is possible to fully configure the 29C53 over the SLD interface, as is done with analog per-line components. Provisions are also made to perform this transfer at a 2 byte-per frame rate using both the C and S bytes of the SLD. The first control byte of a configuration transfer to the 29C53 specifies the type of operation to be performed and the number of data bytes to follow. The system interface command unit loads the internal registers with the information as it is received. When the specified number of data bytes have been transferred, the 29C53 assumes the next input is a control byte.

The order of the bytes in a configuration or status block transfer is determined by the addresses of the internal registers. A multiple-byte transfer, beginning with register 00H, transfers the data to or from that register and increments the address counter.

29C53

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Table 1. 29C53 Registers

Address	Access	Symbol	Name
00000	RD	IXS	Interrupt Status
00000	WR (RT)	IMR	Interrupt Mask
00001	RD	DPS	D-Channel Processor Status
00001	WR (RT)	DPC	D-Channel Processor Control
00010	RD	LPS	Loop and Peripheral Interface Status
00010	WR (RT)	LCR	Loop Interface Control
00011	RDWR	PEC	Peripheral Interface and E-Channel Control
00100	RD	RFN	Receive FIFO Status - # of Bytes Used
00100	WR (RT)	SCR	SLD Interface Control
00101	RD	XFN	Transmit FIFO Status - # of Free Bytes
00101	WR (RT)	SDC	SLD Data Transfer Configuration
00110	RD	SBR	Spare Bits Receive Status
00110	WR (RT)	SBX	Spare Bits Transmit
00111	RDWR	LLB	Loop Interface Loopback Control
01000	RD	RFO	Receive FIFO Output
01001	WR	XFI	Transmit FIFO Input
01010	RDWR	GCR	General Command Register
01011	RDWR	DPR	D-Channel Priority Counter
01100	RDW	RFIL	Receive FIFO Interrupt Level
01101	RDWR	XFIL	Transmit FIFO Interrupt Level
01110	RD	PLENH	Packet Length High Byte
01110	WR (RT)	DUTH	D-Channel Byte Counter Underflow and Overflow Threshold
01111	RD	PLENL	Packet Length Low Byte
01111	WR (RT)	DOTH	D-Channel Byte Counter Overflow Threshold
10000	RDWR	AFD	Auxiliary Frame/Multiframe Division
10001	RDWR	PSR	Position Selection
10010	RD	RSR	Receive Service Request
10011	RD	XSR	Transmit Service Request
11000	RDWR	B1LS	B1 Data in Loop to SLD Direction
11001	RDWR	B2LS	B2 Data in Loop to SLD Direction
11010	RDWR	CR	Control Byte from SLD
11011	RDWR	SR	Signaling Byte from SLD
11100	RDWR	B1SL	B1 Data in SLD to Loop Direction
11101	RDWR	B2SL	B2 Data in SLD to Loop Direction
11110	RDWR	CX	Control Byte to SLD
11111	RDWR	SX	Signaling Byte to SLD

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias ..... −10°C to +80°C
Storage Temperature ..... −65°C to +150°C
Voltage on any Pin .... V_{SS} −0.5V to V_{CC} to +0.5V
Maximum Voltage on V_{CC}
with Respect to V_{SS} ..... +7V
Total Power Dissipation ..... 500 mW

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

NOTICE: Specifications contained within the following tables are subject to change.

D.C. CHARACTERISTICS V_{CC} = +5V ±5%; V_{SS} = 0V; T_A = 0°C to 70°C;

Typical Values are at T_A = 25°C and Nominal Power Supply Values

DIGITAL INTERFACES

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
I_{IL}	Input Leakage Current (Excluding LR+, LR−)			±10	µA	$V_{SS} \le V_{IN} \le V_{CC}$
V_{IL}	Input Low Voltage	−0.5		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = +2.0 mA
V_{OH1}	Output High Voltage	2.4			V	I_{OH} = −400 µA
V_{OH2}	Output High Voltage	0.9 V_{CC}			V	I_{OH} = −40 µA

POWER SUPPLY CURRENT (Averaged over 1 ms)

Symbol	Parameter	Min	Typ	Max	Units	Comments
I_{CC} (P)	Power Down (Standby)		4		mA	SLD and CLK Active
I_{CC} (I)	Idle Operating Current		8		mA	Receiver, SLD, OSC Active
I_{CC} (N)	Normal Operating Current		20		mA	Everything is Active (Excluding (Current for Output Loads)

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A.C. Characteristics V_{CC} = 5V ±5%; V_{SS} = 0V; T_A = 0°C − 70°C; CLK = 3.84 MHz

RECEIVER

Symbol	Parameter	Min	Typ	Max	Units	Comments
V_{RD}	Received Differential Mark Voltage	200		3000	mV	
Z_{IR}	LR+, LR− Input Impedance		60		kΩ	Each Pin
C_{IR}	LR+, LR− Input Capacitance		30		pF	Each Pin

TRANSMITTER

Symbol	Parameter	Min	Typ	Max	Units	Comments
V_{XD}	Transmit Differential Mark Voltage	1780		1980	mV	200 Ω < R_L < 2.5 kΩ
Z_{OX}	LX+, LX− Output Impedance		60		kΩ	Each Pin
C_{OX}	Output Capacitance		30		pF	Each Pin
R_L	Resistive Load Between LX+, LX−	200			Ω	
C_L	Capacitive Load Between LX+, LX−			1500	pF	
t_{LD}	Load Time Constant			0.5	µs	R_L = 300Ω, C_L = 1500 pF
t_{MR}	Transmit Mark Rise Time			400	ns	Note 1
t_D	Damping Time Constant			1.5	µs	
I_{XL}	Source, Sink Current Limit		18		mA	
V_{XL}	Voltage Limiting		125		%	Nominal Mark Voltage

TIMING

Symbol	Parameter	Min	Typ	Max	Units	Comments
J	Timing Extraction Jitter ("S" Slave Mode)	−5		+5	%	I.430 8.2.2
PD	Total Phase Deviation LX with Respect to LR	−7		+15	%	I.430 8.2.3

NOTE:
1. Risetime is measured as 10% to 90% for space mark transitions and 90% to 0% and 0% to 90% for mark-to-mark transitions with respect to final value.

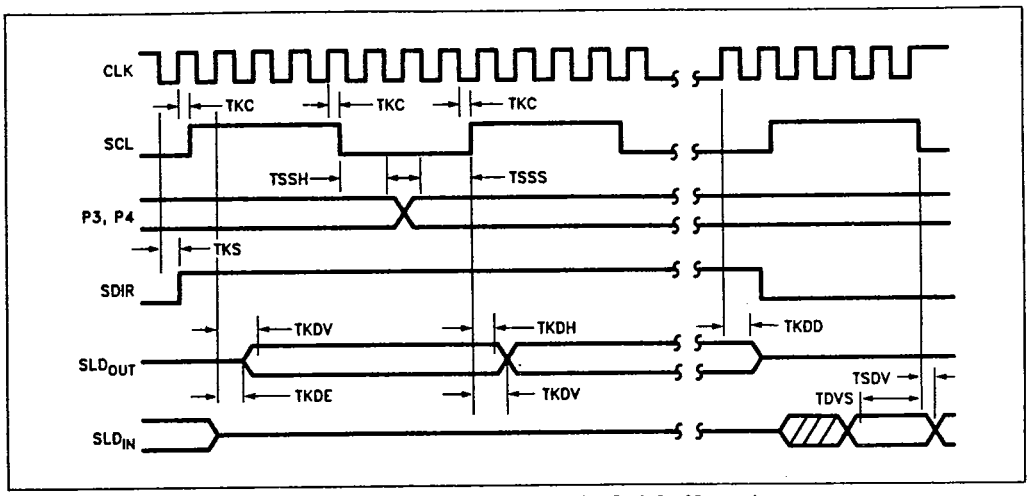

Figure 8. SLD Interface Timing (29C53 As Master)

SLD INTERFACE TIMING (29C53 as Master)

Symbol	Parameter	Min	Max	Units
TKC	CLK to SCL Delay		150	ns
TKS	CLK to SDIR Delay		150	ns
TKDE	CLK to SLD Driver Enabled	0		ns
TKDV	CLK to SLD Data Valid		150	ns
TKDH	SLD Data Hold After Clock Edge	0		
TKDD	CLK to SLD FLoat		150	ns
TDVS	SLD Data Input Setup Time to SCL	50		ns
TSDV	SLD Data Hold Time After SCL	80		ns
TSSH	SLD Status Hold After SCL	80		ns
TSSS	SLD Status Setup Before SCL	80		ns

NOTES:
1. 29C53 samples SLD input data on SCL falling edge.
2. 29C53 changes SLD output data on SCL rising edge.
3. 29C53 SLD out is enabled one CLK cycle after the SDIR rising edge and disabled one CLK cycle before the SDIR falling edge (as master only).

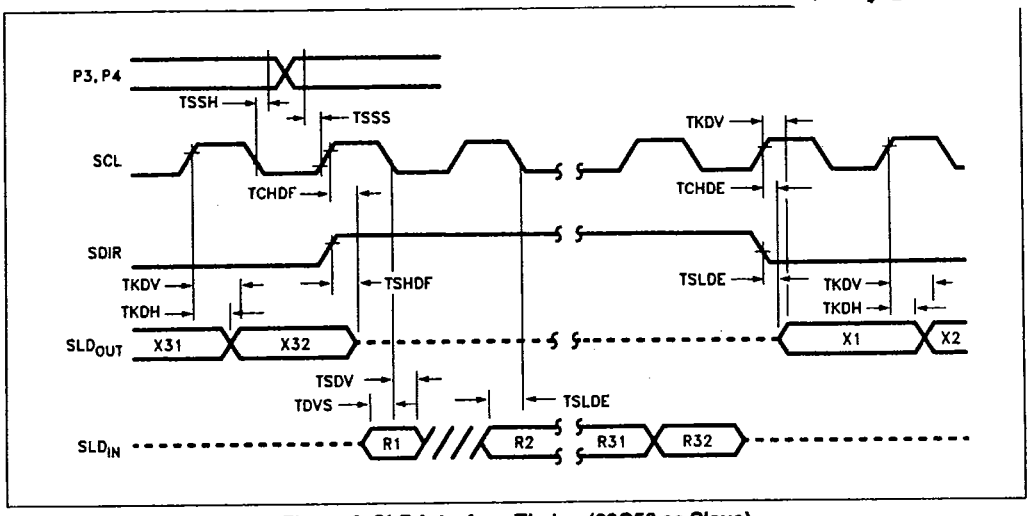

Figure 9. SLD Interface Timing (29C53 as Slave)

SLD INTERFACE TIMING (29C530 as Slave)

Symbol	Parameter	Min	Max	Units
TCHDF	SCL High to Data Out Float		50	ns
TSHDF	SDIR High to Data Out Float		50	ns
TKDH	Output Data Hold After SCL Edge	0		
TKDV	Output Data Valid After SCL Edge		100	ns
TDVS	SLD Input Data Setup Time	50		ns
TSDV	SLD Input Data Hold Time	80		ns
TCHDE	Enable SLD Output After SCL	0		ns
TSLDE	Enable SLD Output After SDIR	0		ns
TSSH	SLD Status Hold After SCL	80		ns
TSSS	SLD Status Setup Before SCL	80		ns

NOTES:
1. 29C53 samples SLD input data on SCL falling edge.
2. 29C53 changes SLD output data on SCL rising edge.

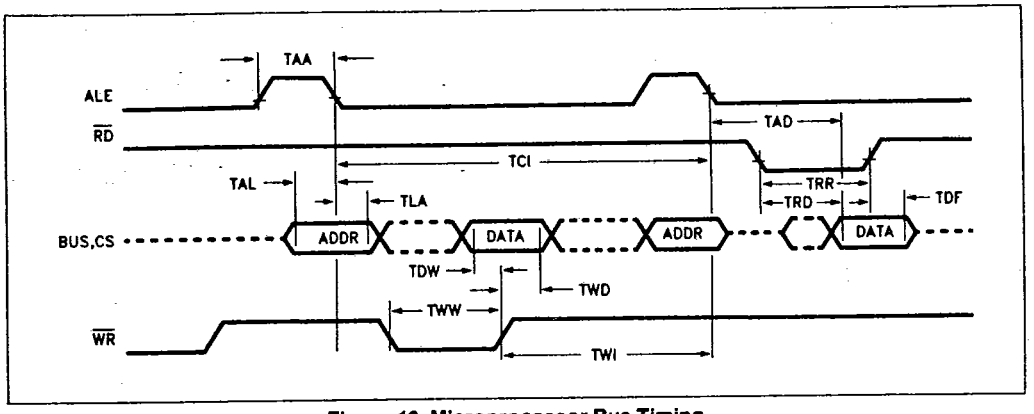

Figure 10. Microprocessor Bus Timing

MICROPROCESSOR BUS TIMING

Symbol	Parameter	Min	Max	Units
TAL	Address Setup Before ALE Trailing Edge	40		ns
TLA	Address Hold After ALE Trailing Edge	20		ns
TWW	Write Control Signal Width	100		ns
TDW	Data Setup Before $\overline{WR}$ Trailing Edge	40		ns
TWD	Data Hold After $\overline{WR}$ Trailing Edge	20		ns
TAA	ALE Pulse Width	60		ns
TWI	*Active $\overline{CS}$ Cycle Disallowed After $\overline{WR}$	2 × 1/CLK		
TRR	Read Control Signal Width	100		ns
TRD	Access Time from $\overline{RD}$ Leading Edge		80	ns
TAD	Access Time from ALE Trailing Edge		260	ns
TDF	Float Delay After $\overline{RD}$ Trailing Edge		40	ns
TCI	Active $\overline{CS}$ Cycle Time for FIFO Access	3 × 1/CLK		

NOTE:
1. * Allow 2 extra clock cycles for GCR commands to execute.

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