MCP6001/2/4

1 MHz, Low-Power Op Amp

Features

- Available in SC-70-5 and SOT-23-5 packages
- Gain Bandwidth Product: 1 MHz (typ.)
- Rail-to-Rail Input/Output
- Supply Voltage: 1.8V to 5.5V
- Supply Current: I_Q = 100 µA (typ.)
- Phase Margin: 90° (typ.)
- Temperature Range:
  - Industrial: -40°C to +85°C
  - Extended: -40°C to +125°C
- Available in Single, Dual and Quad Packages

Applications

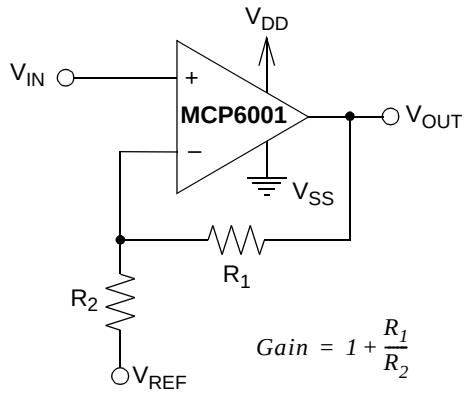
- Automotive
- Portable Equipment
- Photodiode Amplifier
- Analog Filters
- Notebooks and PDAs
- Battery-Powered Systems

Available Tools

SPICE Macro Models (at www.microchip.com)

FilterLab® Software (at www.microchip.com)

Typical Application



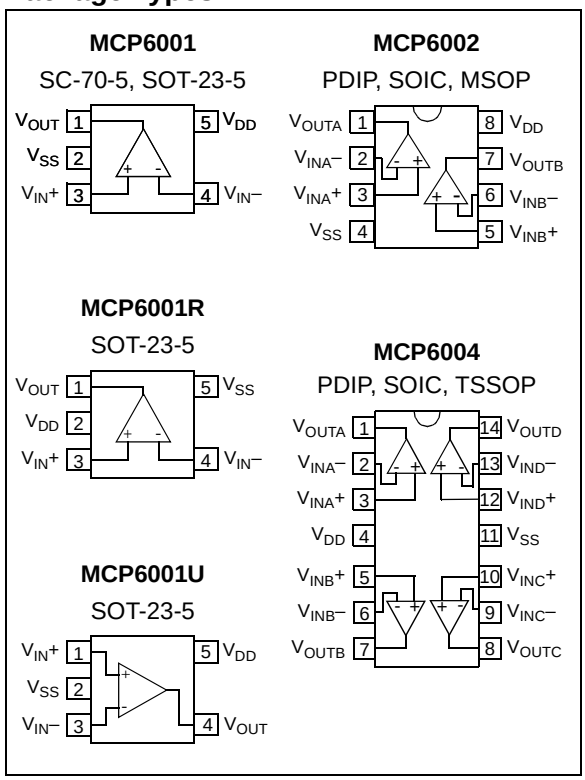
Non-Inverting Amplifier

Description

The Microchip Technology Inc. MCP6001/2/4 family of operational amplifiers (op amps) is specifically designed for general-purpose applications. This family has a 1 MHz Gain Bandwidth Product (GBWP) and 90° phase margin (typ.). It also maintains 45° phase margin (typ.) with a 500 pF capacitive load. This family operates from a single supply voltage as low as 1.8V, while drawing 100 µA (typ.) quiescent current. Additionally, the MCP6001/2/4 supports rail-to-rail input and output swing, with a common mode input voltage range of V_{DD} + 300 mV to V_{SS} – 300 mV. This family of op amps is designed with Microchip's advanced CMOS process.

The MCP6001/2/4 family is available in the industrial and extended temperature ranges, with a power supply range of 1.8V to 5.5V.

Package Types



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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

$V_{DD} - V_{SS}$ 7.0V
All Inputs and Outputs ..... $V_{SS} - 0.3V$ to $V_{DD} + 0.3V$
Difference Input Voltage ..... $|V_{DD} - V_{SS}|$
Output Short-Circuit Current .....continuous
Current at Input Pins .....±2 mA
Current at Output and Supply Pins .....±30 mA
Storage Temperature.....-65°C to +150°C
Maximum Junction Temperature (T_J).....+150°C
ESD Protection On All Pins (HBM;MM) ..... ≥ 4 kV; 200V

† Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, $V_{CM} = V_{DD}/2$, R_L = 10 kΩ to $V_{DD}/2$ and $V_{OUT} \approx V_{DD}/2$.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Input Offset						
Input Offset Voltage	V_{OS}	-4.5	—	+4.5	mV	$V_{CM} = V_{SS}$ **(Note 1)**
Input Offset Drift with Temperature	$\Delta V_{OS}/\Delta T_A$	—	±2.0	—	µV/°C	T_A= -40°C to +125°C, $V_{CM} = V_{SS}$
Power Supply Rejection Ratio	PSRR	—	86	—	dB	$V_{CM} = V_{SS}$
Input Bias Current and Impedance						
Input Bias Current:	I_B	—	±1.0	—	pA	
Industrial Temperature	I_B	—	19	—	pA	T_A = +85°C
Extended Temperature	I_B	—	1100	—	pA	T_A = +125°C
Input Offset Current	I_{OS}	—	±1.0	—	pA	
Common Mode Input Impedance	Z_{CM}	—	10^{13}||6	—	Ω||pF	
Differential Input Impedance	Z_{DIFF}	—	10^{13}||3	—	Ω||pF	
Common Mode						
Common Mode Input Range	V_{CMR}	$V_{SS} - 0.3$	—	$V_{DD} + 0.3$	V	
Common Mode Rejection Ratio	CMRR	60	76	—	dB	V_{CM} = -0.3V to 5.3V, V_{DD} = 5V
Open-Loop Gain						
DC Open-Loop Gain (Large Signal)	A_{OL}	88	112	—	dB	V_{OUT} = 0.3V to V_{DD} – 0.3V, $V_{CM} = V_{SS}$
Output						
Maximum Output Voltage Swing	V_{OL}, V_{OH}	V_{SS} + 25	—	V_{DD} – 25	mV	V_{DD} = 5.5V
Output Short-Circuit Current	I_{SC}	—	±6	—	mA	V_{DD} = 1.8V
		—	±23	—	mA	V_{DD} = 5.5V
Power Supply						
Supply Voltage	V_{DD}	1.8	—	5.5	V	
Quiescent Current per Amplifier	I_Q	50	100	170	µA	I_O = 0, V_{DD} = 5.5V, V_{CM} = 5V

Note 1: MCP6001/2/4 parts with date codes prior to December 2004 (week code 49) were tested to ±7 mV minimum/maximum limits.

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AC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8 to 5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, R_L = 10 kΩ to V_{DD}/2 and C_L = 60 pF.

Parameters	Sym	Min	Typ	Max	Units	Conditions
AC Response						
Gain Bandwidth Product	GBWP	—	1.0	—	MHz	
Phase Margin	PM	—	90	—	°	G = +1
Slew Rate	SR	—	0.6	—	V/µs	
Noise						
Input Noise Voltage	E_{ni}	—	6.1	—	µVp-p	f = 0.1 Hz to 10 Hz
Input Noise Voltage Density	e_{ni}	—	28	—	nV/√Hz	f = 1 kHz
Input Noise Current Density	i_{ni}	—	0.6	—	fA/√Hz	f = 1 kHz

TEMPERATURE SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, V_{DD} = +1.8V to +5.5V and V_{SS} = GND.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Temperature Ranges						
Industrial Temperature Range	T_A	-40	—	+85	°C	
Extended Temperature Range	T_A	-40	—	+125	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	**Note**
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 5L-SC70	θ_{JA}	—	331	—	°C/W	
Thermal Resistance, 5L-SOT-23	θ_{JA}	—	256	—	°C/W	
Thermal Resistance, 8L-PDIP	θ_{JA}	—	85	—	°C/W	
Thermal Resistance, 8L-SOIC (150 mil)	θ_{JA}	—	163	—	°C/W	
Thermal Resistance, 8L-MSOP	θ_{JA}	—	206	—	°C/W	
Thermal Resistance, 14L-PDIP	θ_{JA}	—	70	—	°C/W	
Thermal Resistance, 14L-SOIC	θ_{JA}	—	120	—	°C/W	
Thermal Resistance, 14L-TSSOP	θ_{JA}	—	100	—	°C/W	

Note: The industrial temperature devices operate over this extended temperature range, but with reduced performance. In any case, the internal Junction Temperature (T_J) must not exceed the Absolute Maximum specification of +150°C.

2.0 TYPICAL PERFORMANCE CURVES

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, R_L = 10 kΩ to V_{DD}/2 and C_L = 60 pF.

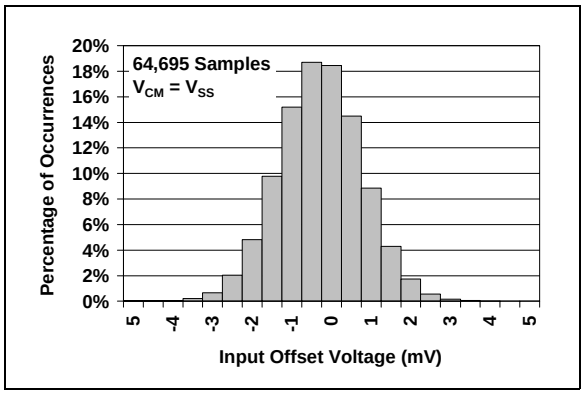

FIGURE 2-1: *Input Offset Voltage.*

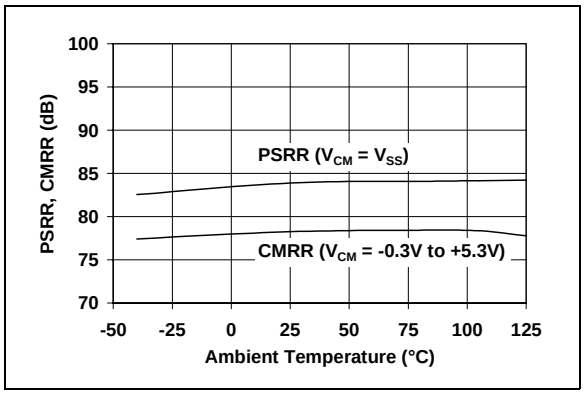

FIGURE 2-4: *CMRR, PSRR vs. Ambient Temperature.*

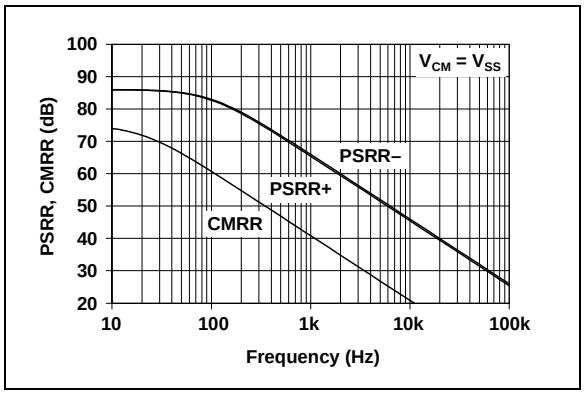

FIGURE 2-2: *PSRR, CMRR vs. Frequency.*

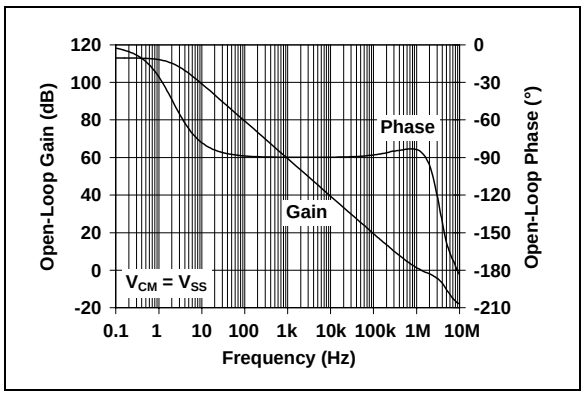

FIGURE 2-5: *Open-Loop Gain, Phase vs. Frequency.*

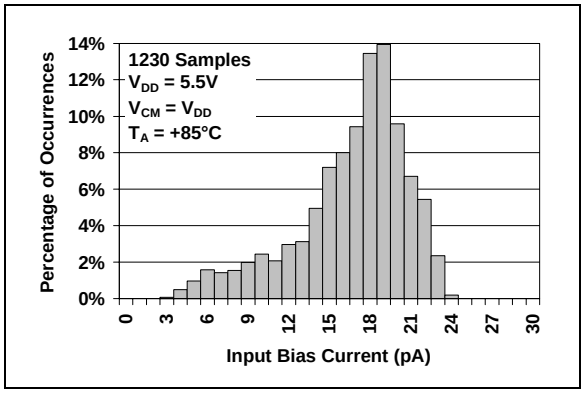

FIGURE 2-3: *Input Bias Current at +85°C.*

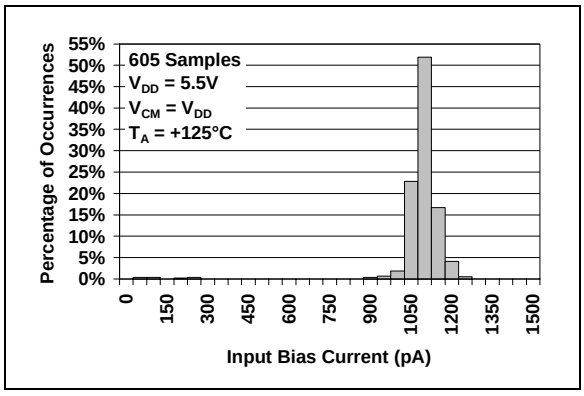

FIGURE 2-6: *Input Bias Current at +125°C.*

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Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, R_L = 10 kΩ to V_{DD}/2 and C_L = 60 pF.

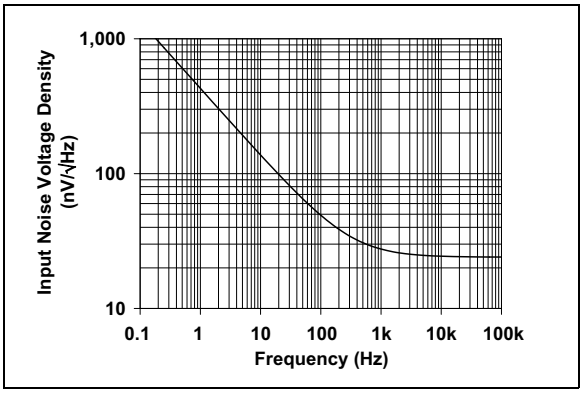

FIGURE 2-7: *Input Noise Voltage Density vs. Frequency.*

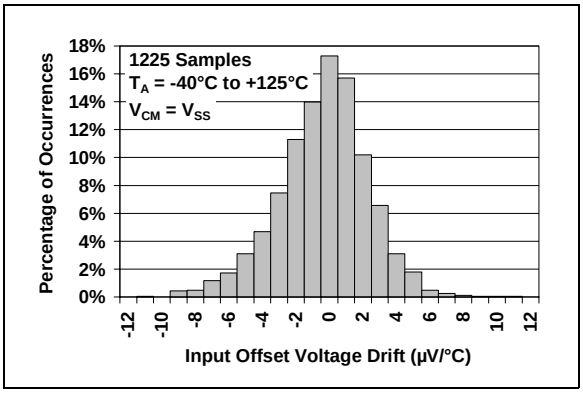

FIGURE 2-10: *Input Offset Voltage Drift.*

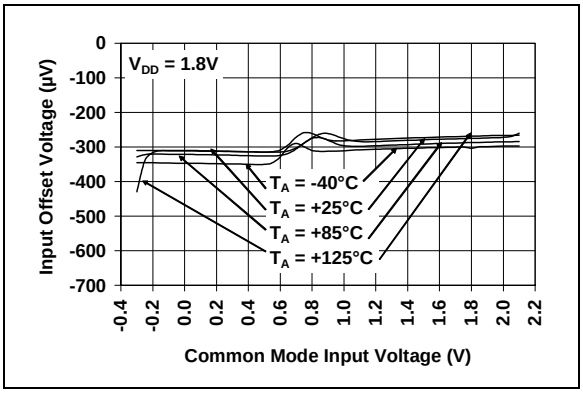

FIGURE 2-8: *Input Offset Voltage vs. Common Mode Input Voltage at V_{DD} = 1.8V.*

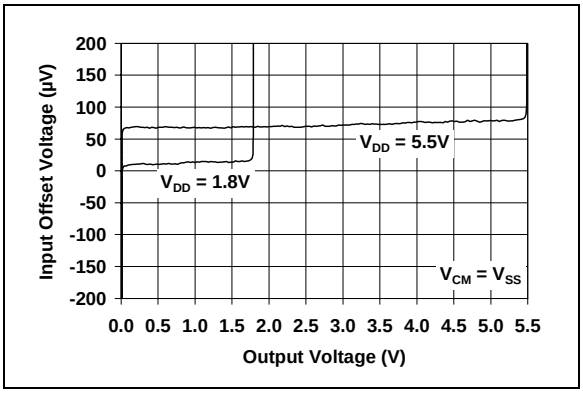

FIGURE 2-11: *Input Offset Voltage vs. Output Voltage.*

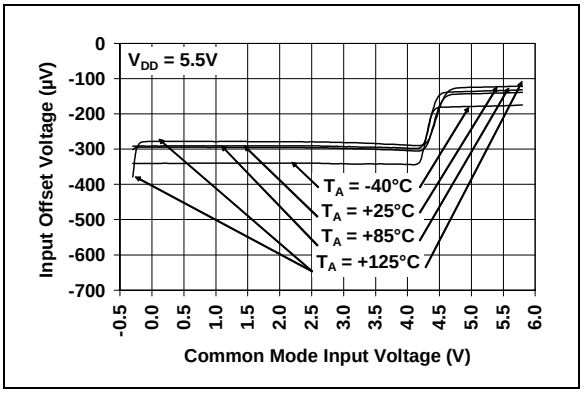

FIGURE 2-9: *Input Offset Voltage vs. Common Mode Input Voltage at V_{DD} = 5.5V.*

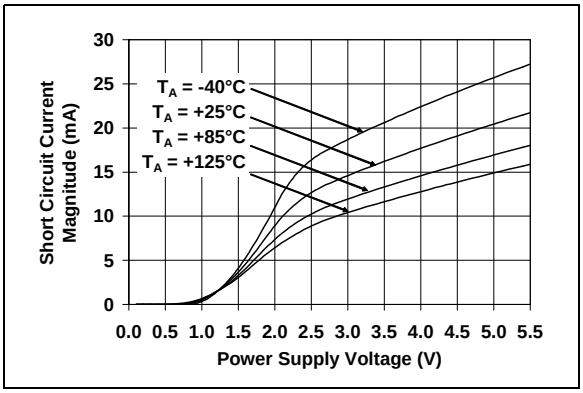

FIGURE 2-12: *Output Short-Circuit Current vs. Power Supply Voltage.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, R_L = 10 kΩ to V_{DD}/2 and C_L = 60 pF.

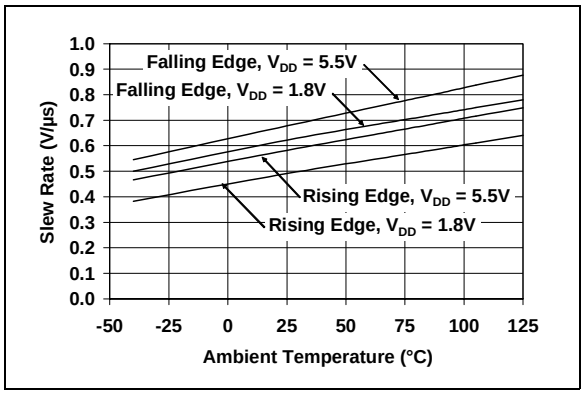

FIGURE 2-13: *Slew Rate vs. Ambient Temperature.*

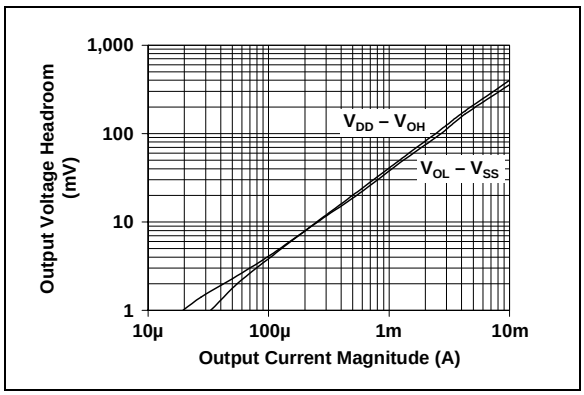

FIGURE 2-14: *Output Voltage Headroom vs. Output Current Magnitude.*

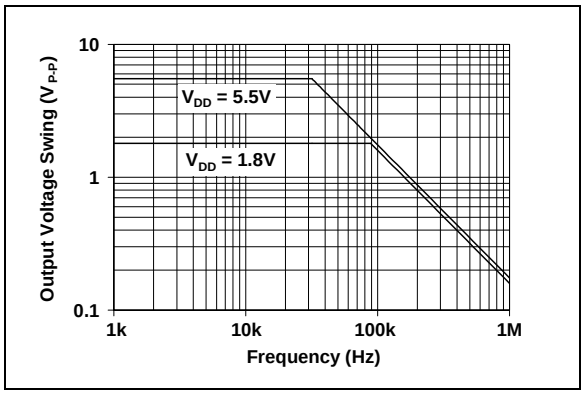

FIGURE 2-15: *Output Voltage Swing vs. Frequency.*

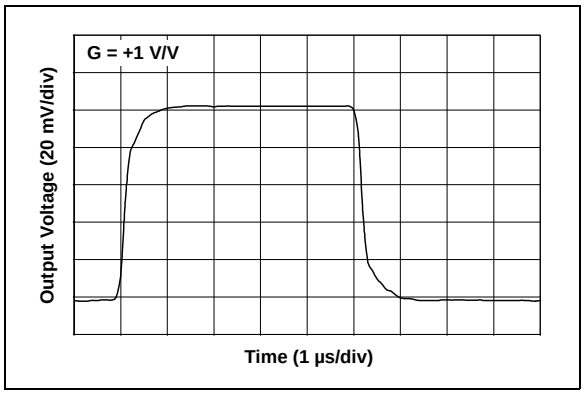

FIGURE 2-16: *Small-Signal, Non-Inverting Pulse Response.*

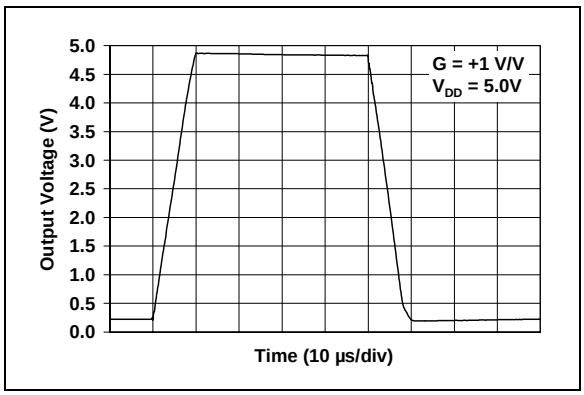

FIGURE 2-17: *Large-Signal, Non-Inverting Pulse Response.*

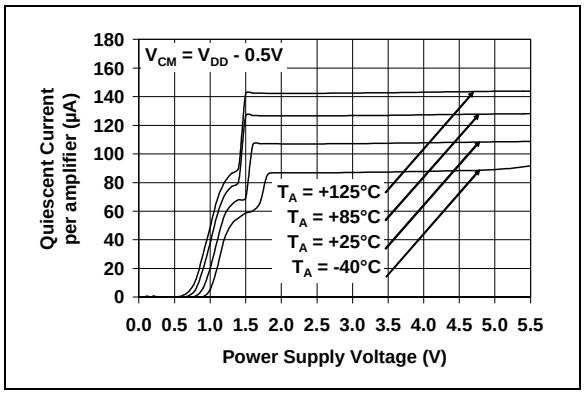

FIGURE 2-18: *Quiescent Current vs. Power Supply Voltage.*

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3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

MCP6001	MCP6001R	MCP6001U	MCP6002	MCP6004	Symbol	Description
1	1	4	1	1	V_{OUT}, V_{OUTA}	Analog Output (op amp A)
4	4	3	2	2	$V_{IN}-$, $V_{INA}-$	Inverting Input (op amp A)
3	3	1	3	3	$V_{IN}+$, $V_{INA}+$	Non-inverting Input (op amp A)
5	2	5	8	4	V_{DD}	Positive Power Supply
—	—	—	5	5	$V_{INB}+$	Non-inverting Input (op amp B)
—	—	—	6	6	$V_{INB}-$	Inverting Input (op amp B)
—	—	—	7	7	V_{OUTB}	Analog Output (op amp B)
—	—	—	—	8	V_{OUTC}	Analog Output (op amp C)
—	—	—	—	9	$V_{INC}-$	Inverting Input (op amp C)
—	—	—	—	10	$V_{INC}+$	Non-inverting Input (op amp C)
2	5	2	4	11	V_{SS}	Negative Power Supply
—	—	—	—	12	$V_{IND}+$	Non-inverting Input (op amp D)
—	—	—	—	13	$V_{IND}-$	Inverting Input (op amp D)
—	—	—	—	14	V_{OUTD}	Analog Output (op amp D)

3.1 Analog Outputs

The output pins are low-impedance voltage sources.

3.2 Analog Inputs

The non-inverting and inverting inputs are high-impedance CMOS inputs with low bias currents.

3.3 Power Supply (V_{SS} and V_{DD})

The positive power supply (V_{DD}) is 1.8V to 5.5V higher than the negative power supply (V_{SS}). For normal operation, the other pins are at voltages between V_{SS} and V_{DD}.

Typically, these parts are used in a single (positive) supply configuration. In this case, V_{SS} is connected to ground and V_{DD} is connected to the supply. V_{DD} will need a local bypass capacitor (typically 0.01 µF to 0.1 µF) within 2 mm of the V_{DD} pin. These parts can share a bulk capacitor with analog parts (typically 2.2 µF to 10 µF) within 100 mm of the V_{DD} pin.

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4.0 APPLICATION INFORMATION

The MCP6001/2/4 family of op amps is manufactured using Microchip's state-of-the-art CMOS process and is specifically designed for low-cost, low-power and general-purpose applications. The low supply voltage, low quiescent current and wide bandwidth makes the MCP6001/2/4 ideal for battery-powered applications. This device has high phase margin, which makes it stable for larger capacitive load applications.

4.1 Rail-to-Rail Input

The MCP6001/2/4 op amps are designed to prevent phase reversal when the input pins exceed the supply voltages. Figure 4-1 shows the input voltage exceeding the supply voltage without any phase reversal.

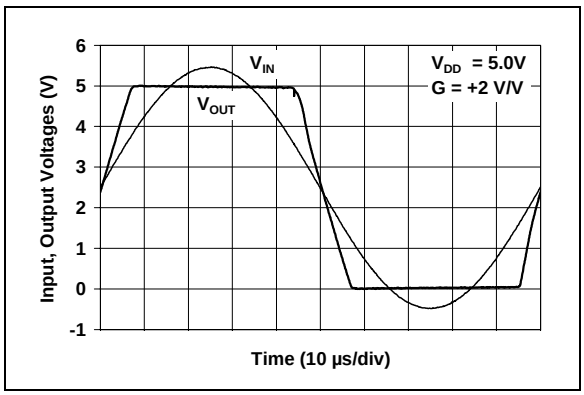

FIGURE 4-1: *The MCP6001/2/4 Show No Phase Reversal.*

The input stage of the MCP6001/2/4 op amps use two differential input stages in parallel. One operates at a low common mode input voltage (V_{CM}), while the other operates at a high V_{CM}. With this topology, the device operates with a V_{CM} up to 300 mV above V_{DD} and 300 mV below V_{SS}. The input offset voltage is measured at $V_{CM} = V_{SS} - 300$ mV and $V_{DD} + 300$ mV to ensure proper operation.

Input voltages that exceed the input voltage range ($V_{SS} - 0.3V$ to $V_{DD} + 0.3V$ at 25°C) can cause excessive current to flow into or out of the input pins, while current beyond ±2 mA can cause reliability problems. Applications that exceed this rating must be externally limited with a resistor, as shown in Figure 4-2.

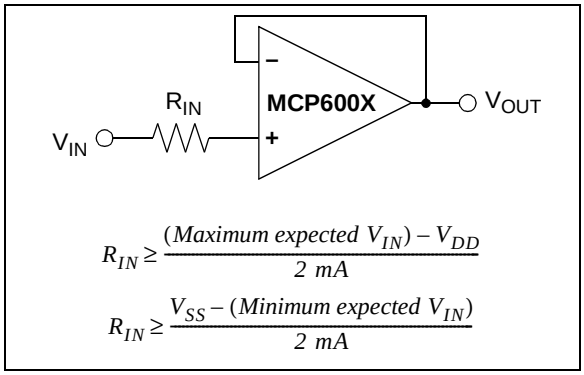

FIGURE 4-2: *Input Current Limiting Resistor (R_{IN}).*

4.2 Rail-to-Rail Output

The output voltage range of the MCP6001/2/4 op amps is $V_{DD} - 25$ mV (min.) and $V_{SS} + 25$ mV (max.) when $R_L = 10$ kΩ is connected to $V_{DD}/2$ and $V_{DD} = 5.5V$. Refer to Figure 2-14 for more information.

4.3 Capacitive Loads

Driving large capacitive loads can cause stability problems for voltage feedback op amps. As the load capacitance increases, the feedback loop's phase margin decreases and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response, with overshoot and ringing in the step response. While a unity-gain buffer (G = +1) is the most sensitive to capacitive loads, all gains show the same general behavior.

When driving large capacitive loads with these op amps (e.g., > 100 pF when G = +1), a small series resistor at the output (R_{ISO} in Figure 4-3) improves the feedback loop's phase margin (stability) by making the output load resistive at higher frequencies. The bandwidth will be generally lower than the bandwidth with no capacitance load.

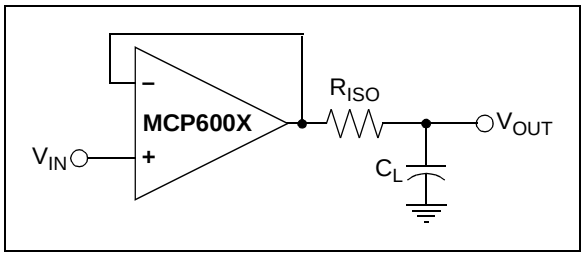

FIGURE 4-3: *Output resistor, R_{ISO} stabilizes large capacitive loads.*

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Figure 4-4 gives recommended R_{ISO} values for different capacitive loads and gains. The x-axis is the normalized load capacitance (C_L/G_N), where G_N is the circuit's noise gain. For non-inverting gains, G_N and the Signal Gain are equal. For inverting gains, G_N is 1+|Signal Gain| (e.g., -1 V/V gives G_N = +2 V/V).

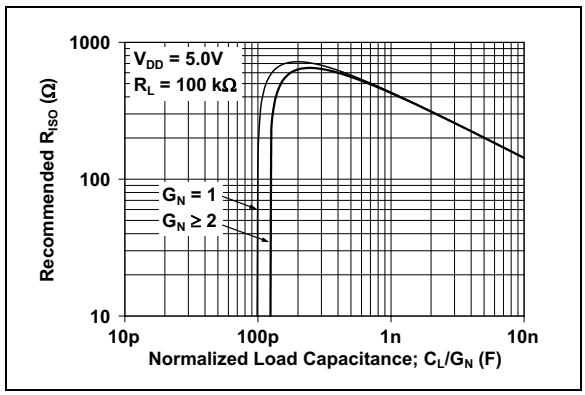

FIGURE 4-4: *Recommended R_{ISO} values for Capacitive Loads.*

After selecting R_{ISO} for your circuit, double-check the resulting frequency response peaking and step response overshoot. Modify R_{ISO}'s value until the response is reasonable. Bench evaluation and simulations with the MCP6001/2/4 SPICE macro model are very helpful.

4.4 Supply Bypass

With this family of operational amplifiers, the power supply pin (V_{DD} for single-supply) should have a local bypass capacitor (i.e., 0.01 µF to 0.1 µF) within 2 mm for good high-frequency performance. It also needs a bulk capacitor (i.e., 1 µF or larger) within 100 mm to provide large, slow currents. This bulk capacitor can be shared with other analog parts.

4.5 PCB Surface Leakage

In applications where low input bias current is critical, Printed Circuit Board (PCB) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is $10^{12}\Omega$. A 5V difference would cause 5 pA of current to flow; which is greater than the MCP6001/2/4 family's bias current at 25°C (1 pA, typ.).

The easiest way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 4-5.

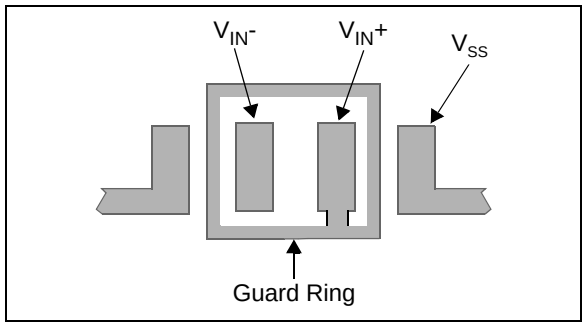

FIGURE 4-5: *Example Guard Ring Layout for Inverting Gain.*

1. Non-inverting Gain and Unity-Gain Buffer:
   a. Connect the non-inverting pin (V_{IN}+) to the input with a wire that does not touch the PCB surface.
   b. Connect the guard ring to the inverting input pin (V_{IN}–). This biases the guard ring to the common mode input voltage.
2. Inverting Gain and Transimpedance Gain Amplifiers (convert current to voltage, such as photo detectors):
   a. Connect the guard ring to the non-inverting input pin (V_{IN}+). This biases the guard ring to the same reference voltage as the op amp (e.g., V_{DD}/2 or ground).
   b. Connect the inverting pin (V_{IN}–) to the input with a wire that does not touch the PCB surface.

4.6 Application Circuits

4.6.1 UNITY-GAIN BUFFER

The rail-to-rail input and output capability of the MCP6001/2/4 op amp is ideal for unity-gain buffer applications. The low quiescent current and wide bandwidth makes the device suitable for a buffer configuration in an instrumentation amplifier circuit, as shown in Figure 4-6.

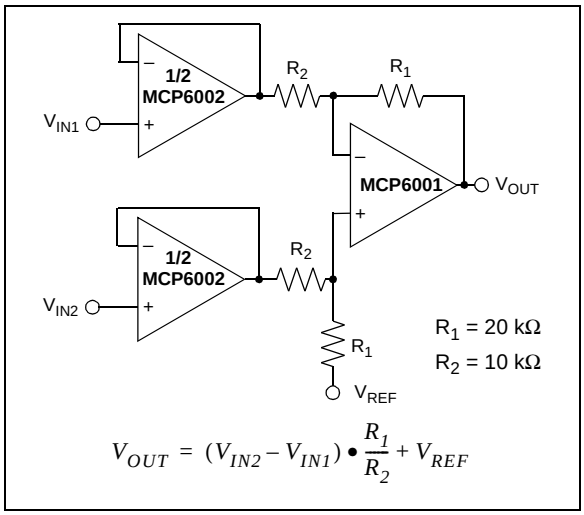

FIGURE 4-6: *Instrumentation Amplifier with Unity-Gain Buffer Inputs.*

4.6.2 ACTIVE LOW-PASS FILTER

The MCP6001/2/4 op amp's low input bias current makes it possible for the designer to use larger resistors and smaller capacitors for active low-pass filter applications. However, as the resistance increases, the noise generated also increases. Parasitic capacitances and the large value resistors could also modify the frequency response. These trade-offs need to be considered when selecting circuit elements.

Usually, the op amp bandwidth is 100X the filter cutoff frequency (or higher) for good performance. It is possible to have the op amp bandwidth 10X higher than the cutoff frequency, thus having a design that is more sensitive to component tolerances.

Figure 4-7 shows a second-order Butterworth filter with 100 kHz cutoff frequency and a gain of +1 V/V; the op amp bandwidth is only 10X higher than the cutoff frequency. The component values were selected using Microchip's FilterLab® software.

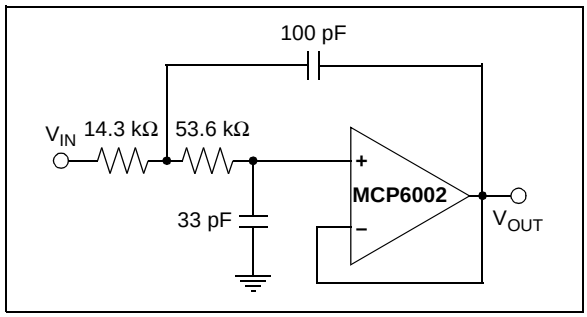

FIGURE 4-7: *Active Second-Order Low- Pass Filter.*

4.6.3 PEAK DETECTOR

The MCP6001/2/4 op amp has a high input impedance, rail-to-rail input/output and low input bias current, which makes this device suitable for peak detector applications. Figure 4-8 shows a peak detector circuit with clear and sample switches. The peak-detection cycle uses a clock (CLK), as shown in Figure 4-8.

At the rising edge of CLK, Sample Switch closes to begin sampling. The peak voltage stored on C_1 is sampled to C_2 for a sample time defined by t_{SAMP}. At the end of the sample time (falling edge of Sample Signal), Clear Signal goes high and closes the Clear Switch. When the Clear Switch closes, C_1 discharges through R_1 for a time defined by t_{CLEAR}. At the end of the clear time (falling edge of Clear Signal), op amp A begins to store the peak value of V_{IN} on C_1 for a time defined by t_{DETECT}.

In order to define t_{SAMP} and t_{CLEAR}, it is necessary to determine the capacitor charging and discharging period. The capacitor charging time is limited by the amplifier source current, while the discharging time (τ) is defined using R_1 ($\tau = R_1C_1$). t_{DETECT} is the time that the input signal is sampled on C_1 and is dependent on the input voltage change frequency.

The op amp output current limit, and the size of the storage capacitors (both C_1 and C_2), could create slewing limitations as the input voltage (V_{IN}) increases. Current through a capacitor is dependent on the size of the capacitor and the rate of voltage change. From this relationship, the rate of voltage change or the slew rate can be determined. For example, with an op amp short-circuit current of I_{SC} = 25 mA and a load capacitor of C_1 = 0.1 µF, then:

EQUATION 4-1:

$$I_{SC} = C_1 \frac{dV_{C1}}{dt}$$

$$\frac{dV_{C1}}{dt} = \frac{I_{SC}}{C_1}$$

$$= \frac{25mA}{0.1\mu F}$$

$$\frac{dV_{C1}}{dt} = 250mV/\mu s$$

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This voltage rate of change is less than the MCP6001/2/4 slew rate of 0.6 V/µs. When the input voltage swings below the voltage across C_1, D_1 becomes reverse-biased. This opens the feedback loop and rails the amplifier. When the input voltage increases, the amplifier recovers at its slew rate. Based on the rate of voltage change shown in the above equation, it takes an extended period of time to charge a 0.1 µF capacitor. The capacitors need to be selected so that the circuit is not limited by the amplifier slew rate. Therefore, the capacitors should be less than 40 µF and a stabilizing resistor (R_{ISO}) needs to be properly selected. (Refer to **Section 4.3 "Capacitive Loads"**).

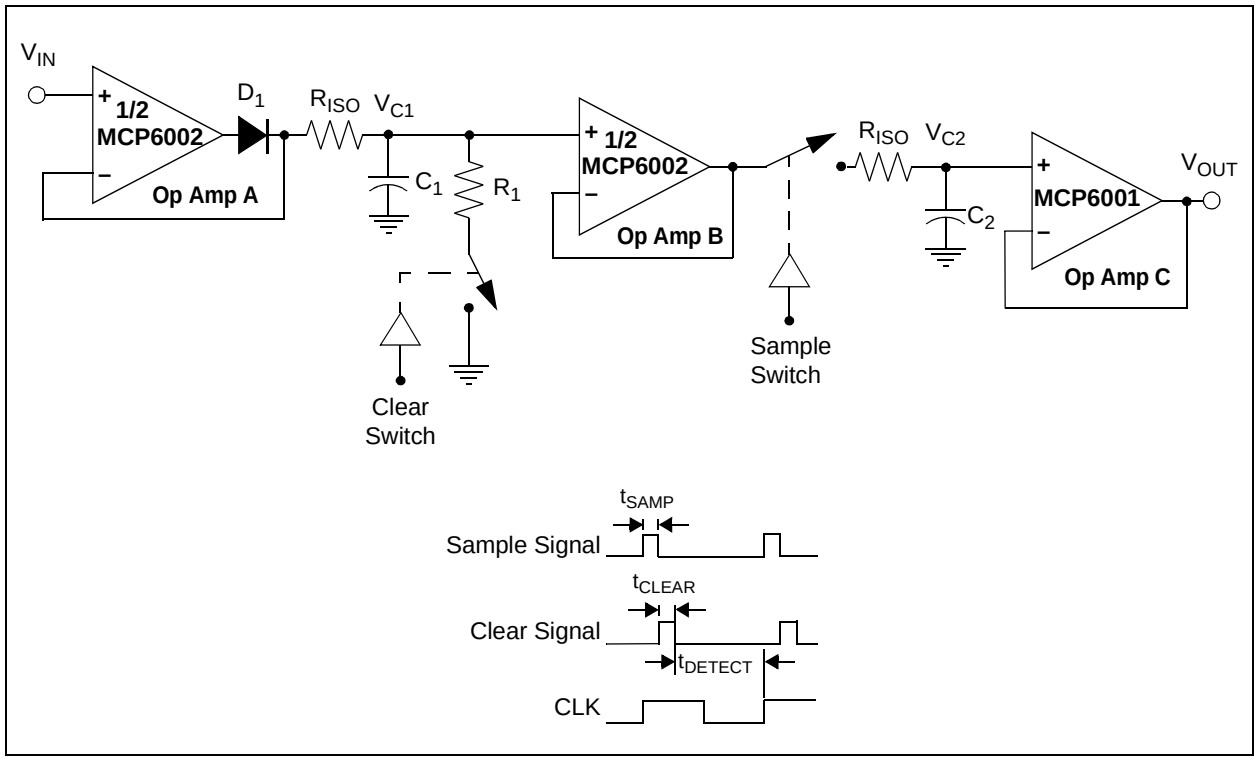

FIGURE 4-8: *Peak Detector with Clear and Sample CMOS Analog Switches.*

5.0 DESIGN TOOLS

Microchip provides the basic design tools needed for the MCP6001/2/4 family of op amps.

5.1 SPICE Macro Model

The latest SPICE macro model for the MCP6001/2/4 op amps is available on our web site at www.microchip.com. This model is intended to be an initial design tool that works well in the op amp's linear region of operation at room temperature. See the model file for information on its capabilities.

Bench testing is a very important part of any design and cannot be replaced with simulations. Also, simulation results using this macro model need to be validated by comparing them to the data sheet specifications and characteristic curves.

5.2 FilterLab® Software

Microchip's FilterLab® software is an innovative software tool that simplifies analog active filter (using op amps) design. Available at no cost from our web site at www.microchip.com, the FilterLab design tool provides full schematic diagrams of the filter circuit with component values. It also outputs the filter circuit in SPICE format, which can be used with the macro model to simulate actual filter performance.

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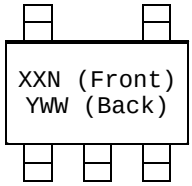
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

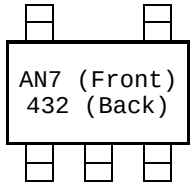
5-Lead SC-70 (**MCP6001**)



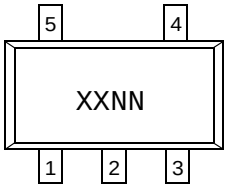
Device	I-Temp Code	E-Temp Code
MCP6001	ANN	CDN

Note: Applies to 5-Lead SC-70.

Example: (I-Temp)



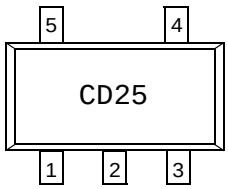
5-Lead SOT-23 (**MCP6001/1R/1U**)



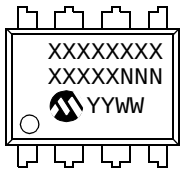
Device	I-Temp Code	E-Temp Code
MCP6001	AANN	CDNN
MCP6001R	ADNN	CENN
MCP6001U	AFNN	CFNN

Note: Applies to 5-Lead SOT-23.

Example: (E-Temp)



8-Lead PDIP (300 mil)



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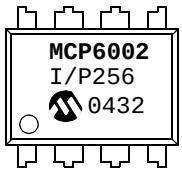
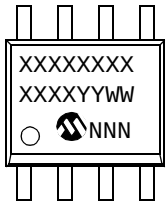
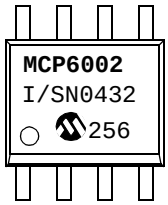


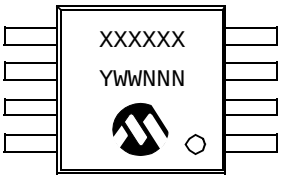
8-Lead SOIC (150 mil)



Example:



8-Lead MSOP



Example:

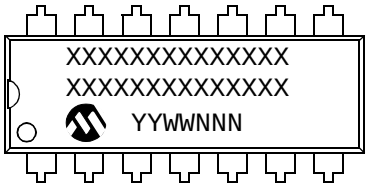
Legend:	XX...X	Customer specific information*
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

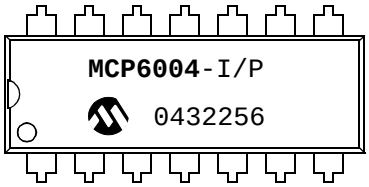
***** Standard marking consists of Microchip part number, year code, week code, traceability code (facility code, mask rev#, and assembly code). For marking beyond this, certain price adders apply. Please check with your Microchip Sales Office.

Package Marking Information (Continued)

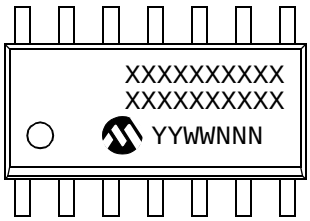
14-Lead PDIP (300 mil) (**MCP6004**)



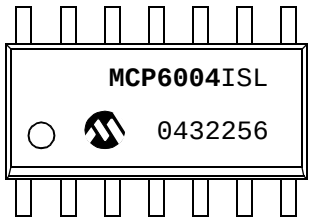
Example:



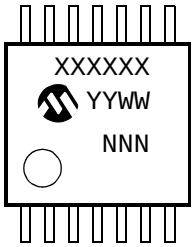
14-Lead SOIC (150 mil) (**MCP6004**)



Example:



14-Lead TSSOP (**MCP6004**)



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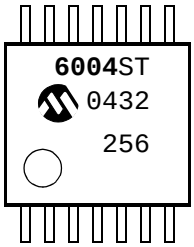

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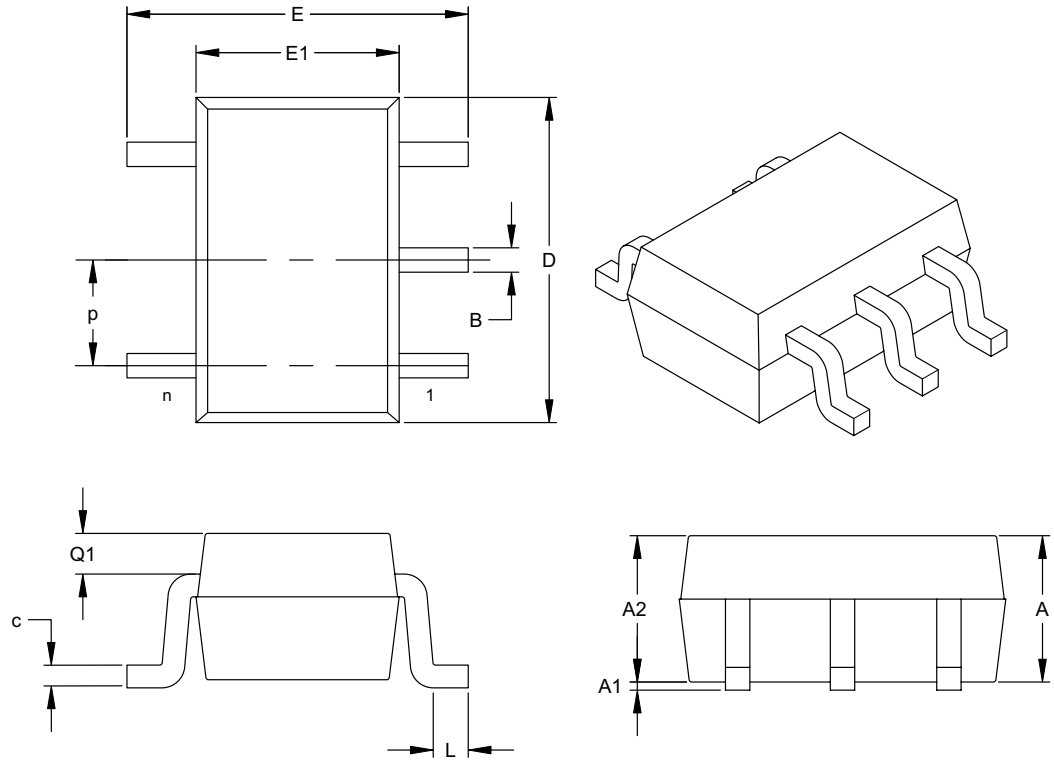
5-Lead Plastic Package (SC-70)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		5			5	
Pitch	p		.026 (BSC)			0.65 (BSC)	
Overall Height	A	.031		.043	0.80		1.10
Molded Package Thickness	A2	.031		.039	0.80		1.00
Standoff	A1	.000		.004	0.00		0.10
Overall Width	E	.071		.094	1.80		2.40
Molded Package Width	E1	.045		.053	1.15		1.35
Overall Length	D	.071		.087	1.80		2.20
Foot Length	L	.004		.012	0.10		0.30
Top of Molded Pkg to Lead Shoulder	Q1	.004		.016	0.10		0.40
Lead Thickness	c	.004		.007	0.10		0.18
Lead Width	B	.006		.012	0.15		0.30

*Controlling Parameter

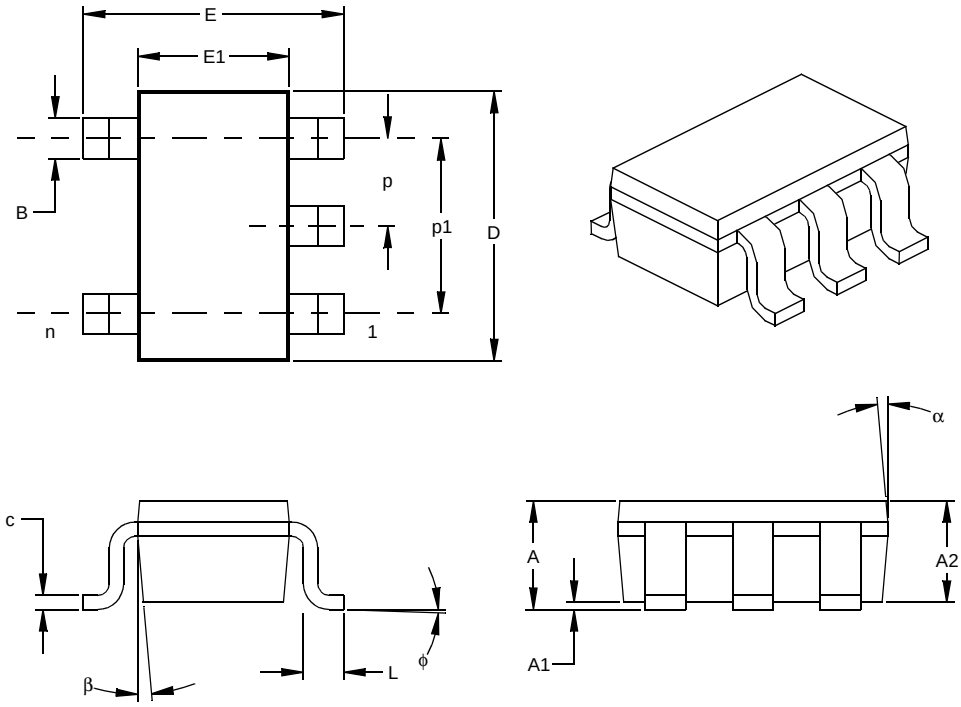
Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" (0.127mm) per side.

JEITA (EIAJ) Standard: SC-70

Drawing No. C04-061

5-Lead Plastic Small Outline Transistor (OT) (SOT23)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		5			5	
Pitch	p		.038			0.95	
Outside lead pitch (basic)	p1		.075			1.90	
Overall Height	A	.035	.046	.057	0.90	1.18	1.45
Molded Package Thickness	A2	.035	.043	.051	0.90	1.10	1.30
Standoff §	A1	.000	.003	.006	0.00	0.08	0.15
Overall Width	E	.102	.110	.118	2.60	2.80	3.00
Molded Package Width	E1	.059	.064	.069	1.50	1.63	1.75
Overall Length	D	.110	.116	.122	2.80	2.95	3.10
Foot Length	L	.014	.018	.022	0.35	0.45	0.55
Foot Angle	ϕ	0	5	10	0	5	10
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B	.014	.017	.020	0.35	0.43	0.50
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MO-178
Drawing No. C04-091

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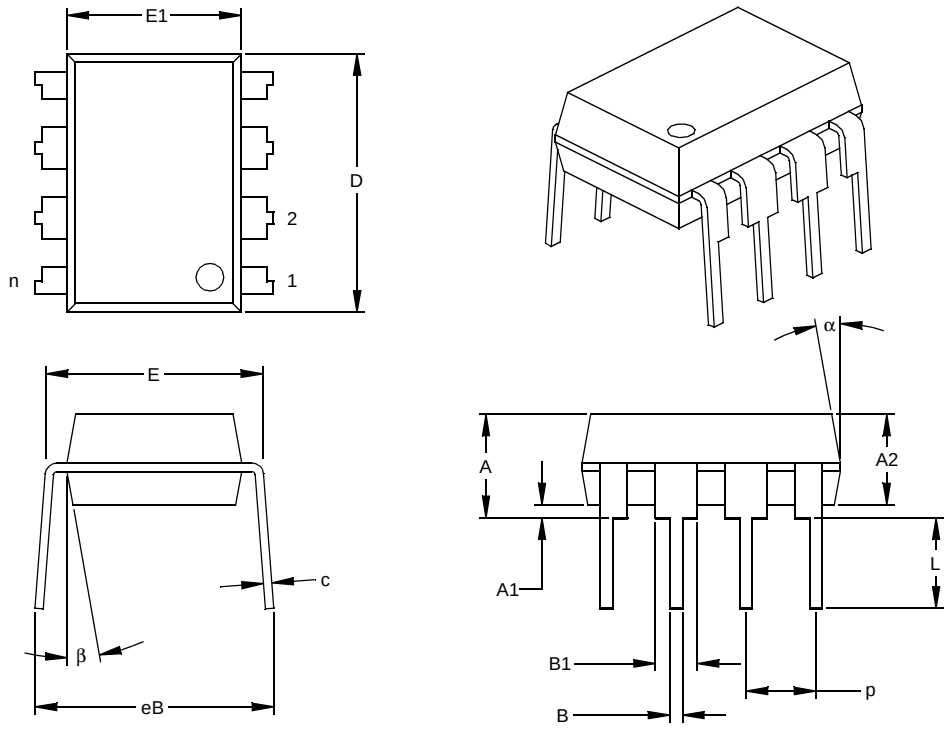
8-Lead Plastic Dual In-line (P) – 300 mil (PDIP)

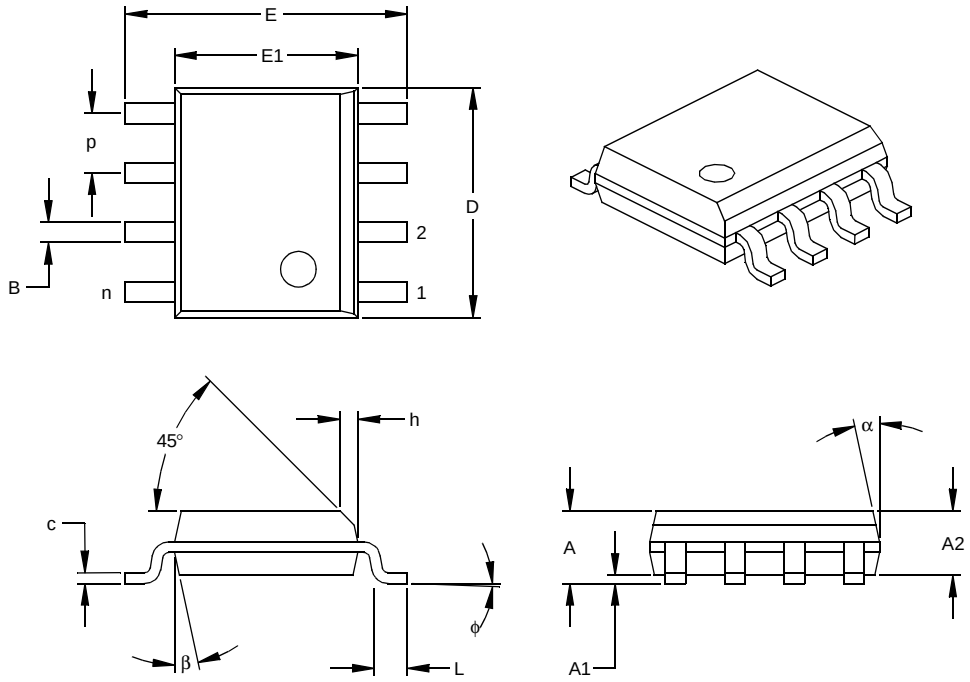


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-018

8-Lead Plastic Small Outline (SN) – Narrow, 150 mil (SOIC)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-057

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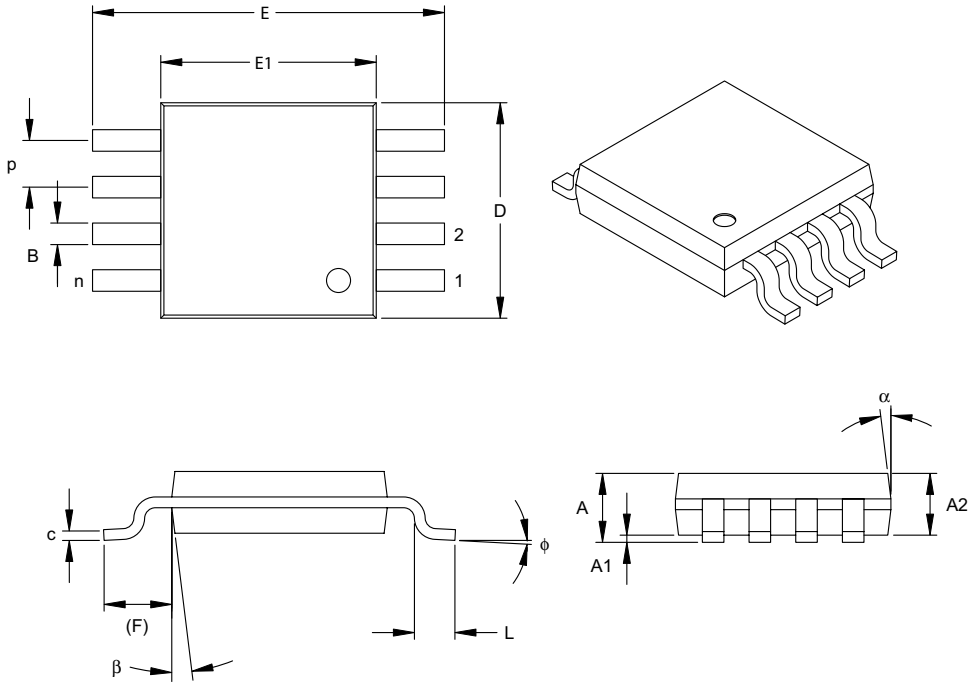
8-Lead Plastic Micro Small Outline Package (MS) (MSOP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.026 BSC			0.65 BSC	
Overall Height	A	-	-	.043	-	-	1.10
Molded Package Thickness	A2	.030	.033	.037	0.75	0.85	0.95
Standoff	A1	.000	-	.006	0.00	-	0.15
Overall Width	E		.193 TYP.			4.90 BSC	
Molded Package Width	E1		.118 BSC			3.00 BSC	
Overall Length	D		.118 BSC			3.00 BSC	
Foot Length	L	.016	.024	.031	0.40	0.60	0.80
Footprint (Reference)	F		.037 REF			0.95 REF	
Foot Angle	ϕ	0°	-	8°	0°	-	8°
Lead Thickness	c	.003	.006	.009	0.08	-	0.23
Lead Width	B	.009	.012	.016	0.22	-	0.40
Mold Draft Angle Top	α	5°	-	15°	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°	5°	-	15°

*Controlling Parameter

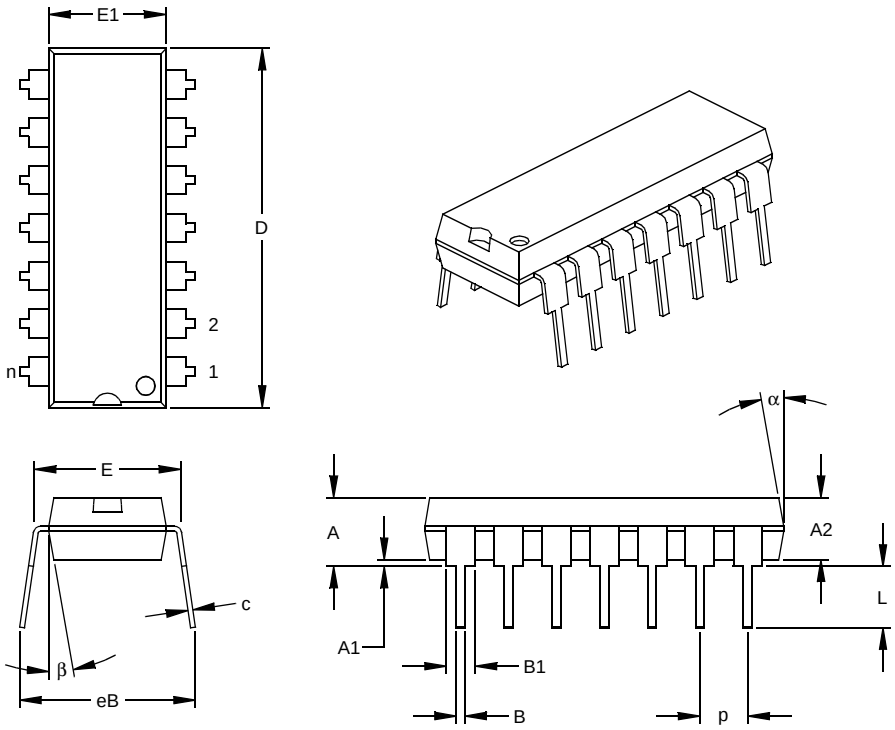
Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MO-187

Drawing No. C04-111

14-Lead Plastic Dual In-line (P) – 300 mil (PDIP)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.740	.750	.760	18.80	19.05	19.30
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-005

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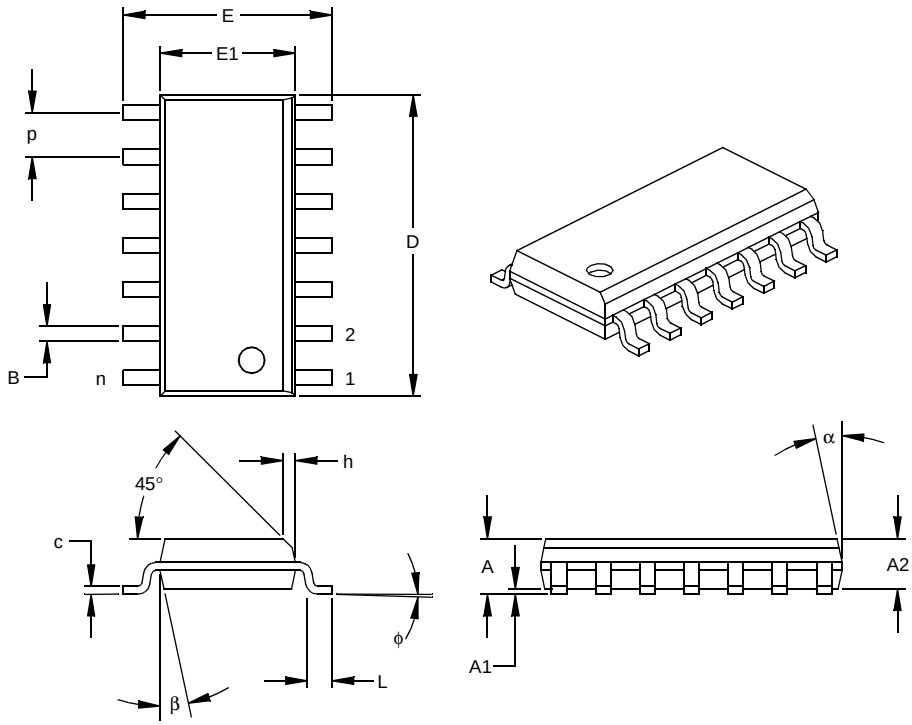
14-Lead Plastic Small Outline (SL) – Narrow, 150 mil (SOIC)

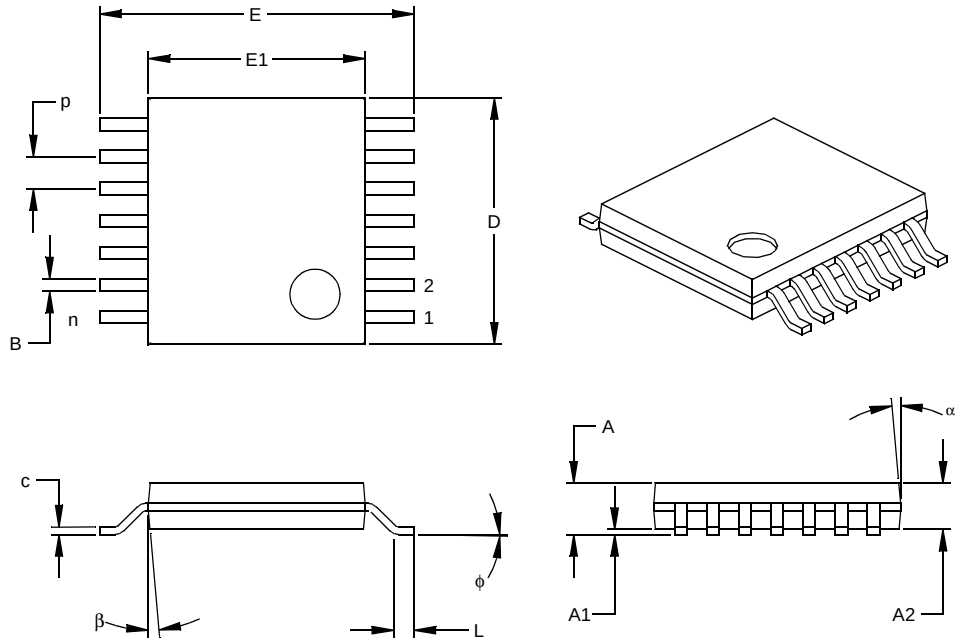


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.236	.244	5.79	5.99	6.20
Molded Package Width	E1	.150	.154	.157	3.81	3.90	3.99
Overall Length	D	.337	.342	.347	8.56	8.69	8.81
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-065

14-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm (TSSOP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.026			0.65	
Overall Height	A			.043			1.10
Molded Package Thickness	A2	.033	.035	.037	0.85	0.90	0.95
Standoff §	A1	.002	.004	.006	0.05	0.10	0.15
Overall Width	E	.246	.251	.256	6.25	6.38	6.50
Molded Package Width	E1	.169	.173	.177	4.30	4.40	4.50
Molded Package Length	D	.193	.197	.201	4.90	5.00	5.10
Foot Length	L	.020	.024	.028	0.50	0.60	0.70
Foot Angle	ϕ	0	4	8	0	4	8
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B1	.007	.010	.012	0.19	0.25	0.30
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005” (0.127mm) per side.
JEDEC Equivalent: MO-153
Drawing No. C04-087

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APPENDIX A: REVISION HISTORY

Revision A (June 2002)

Original data sheet release.

Revision B (October 2002)

Revision C (December 2002)

Revision D (May 2003)

Revision E (December 2004)

The following is the list of modifications:

1. V_{OS} specification reduced to ±4.5 mV from ±7.0 mV for parts starting with date code YYWW = 0449
2. Corrected package markings in **Section 6.0 "Packaging Information"**
3. Added Appendix A: Revision History.

NOTES:

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX
Device	Temperature Range	Package

Device:	MCP6001T:	Single Op Amp (Tape and Reel) (SC-70, SOT-23)
	MCP6001RT:	Single Op Amp (Tape and Reel) (SOT-23)
	MCP6001UT:	Single Op Amp (Tape and Reel) (SOT-23)
	MCP6002:	Dual Op Amp
	MCP6002T:	Dual Op Amp (Tape and Reel) (SOIC, MSOP)
	MCP6004:	Quad Op Amp
	MCP6004T:	Quad Op Amp (Tape and Reel) (SOIC, MSOP)
Temperature Range:	I =	-40°C to +85°C
	E =	-40°C to +125°C
Package:	LT =	Plastic Package (SC-70), 5-lead (MCP6001 only)
	OT =	Plastic Small Outline Transistor (SOT-23), 5-lead (MCP6001, MCP6001R, MCP6001U)
	MS =	Plastic MSOP, 8-lead
	P =	Plastic DIP (300 mil Body), 8-lead, 14-lead
	SN =	Plastic SOIC, (150 mil Body), 8-lead
	SL =	Plastic SOIC (150 mil Body), 14-lead
	ST =	Plastic TSSOP (4.4mm Body), 14-lead

Examples:

a)	MCP6001T-I/LT:	Tape and Reel, Industrial Temperature, 5LD SC-70 package
b)	MCP6001T-I/OT:	Tape and Reel, Industrial Temperature, 5LD SOT-23 package.
c)	MCP6001RT-I/OT:	Tape and Reel, Industrial Temperature, 5LD SOT-23 package.
d)	MCP6001UT-E/OT:	Tape and Reel, Extended Temperature, 5LD SOT-23 package.
a)	MCP6002-I/MS:	Industrial Temperature, 8LD MSOP package.
b)	MCP6002-I/P:	Industrial Temperature, 8LD PDIP package.
c)	MCP6002-E/P:	Extended Temperature, 8LD PDIP package.
d)	MCP6002-I/SN:	Industrial Temperature, 8LD SOIC package.
e)	MCP6002T-I/MS:	Tape and Reel, Industrial Temperature, 8LD MSOP package.
a)	MCP6004-I/P:	Industrial Temperature, 14LD PDIP package.
b)	MCP6004-I/SL:	Industrial Temperature,, 14LD SOIC package.
c)	MCP6004-E/SL:	Extended Temperature,, 14LD SOIC package.
d)	MCP6004-I/ST:	Industrial Temperature, 14LD TSSOP package.
e)	MCP6004T-I/SL:	Tape and Reel, Industrial Temperature, 14LD SOIC package.
f)	MCP6004T-I/ST:	Tape and Reel, Industrial Temperature, 14LD TSSOP package.

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Data Sheets
Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

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2. The Microchip Worldwide Site (www.microchip.com)

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

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NOTES:

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