EPSON

E0C6266

4-bit Single Chip Microcomputer

Wide Voltage Operation Products

- Core CPU Architecture
- 38.4kHz/500kHz Twin Clock Operation
- Built-in, 2-ch. Serial Ports
- SVD Circuit/2-ch. Analog Comparators

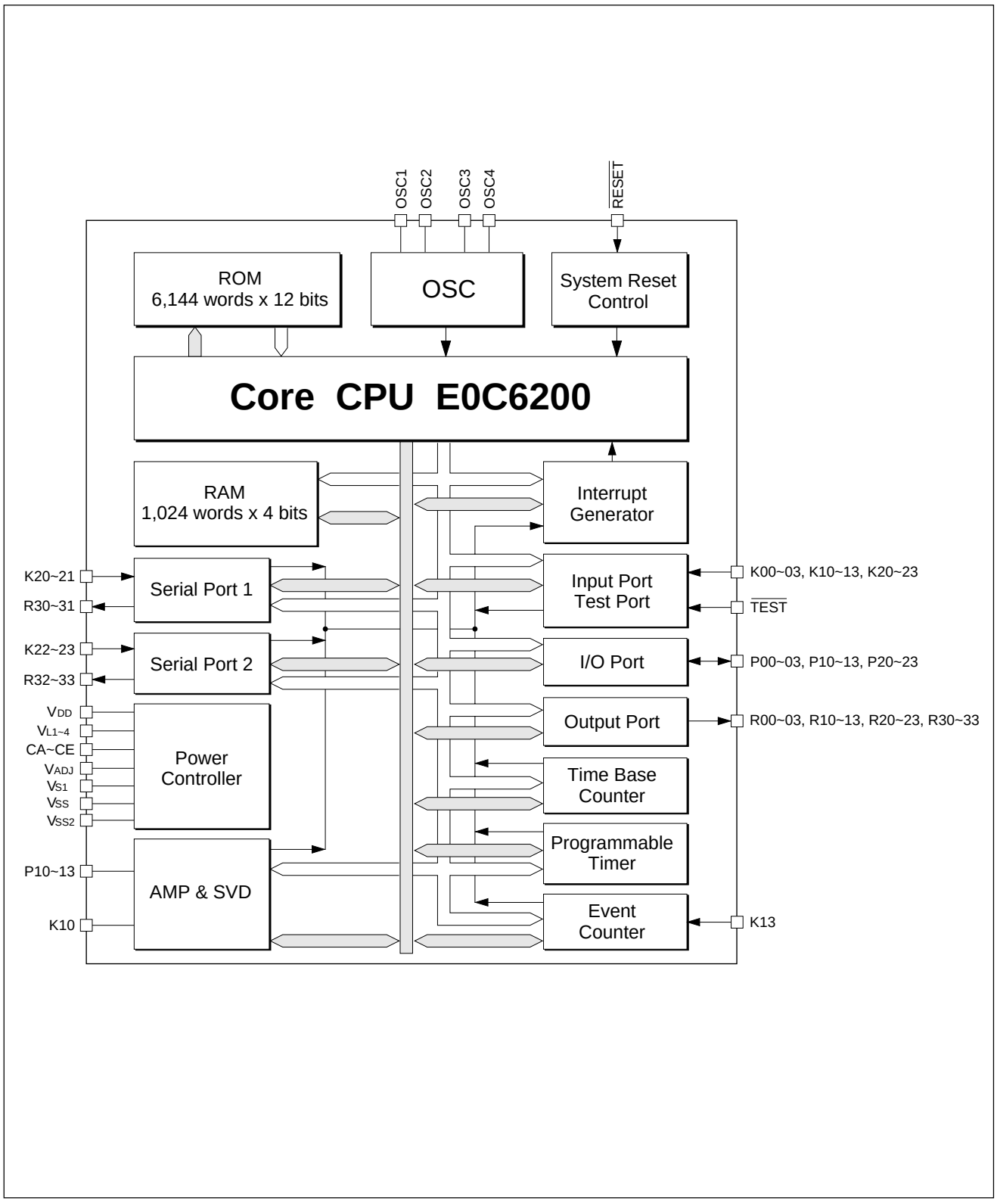
■ DESCRIPTION

The E0C6266 is an advanced single-chip CMOS 4-bit microcomputer consisting of the E0C6200 CMOS 4-bit core CPU. It also contains the ROM, RAM, 2-channel timer, event counter, start-stop serial ports, clock sync serial ports and 40 I/O ports.
The E0C6266 provides an excellent solution for low-power consumption systems with clock functions.

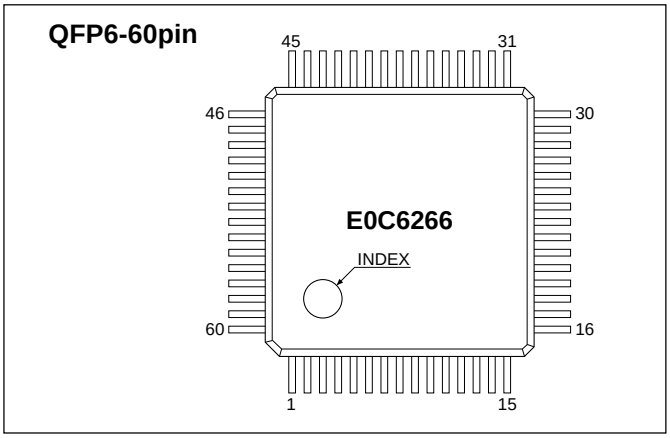
■ FEATURES

- CMOS LSI 4-bit parallel processing
- Clock ..... 38.4kHz (Typ.)/500kHz (Max.) (selectable by software)
- Instruction set ..... 108 instructions
- Instruction cycle time ..... 130µsec, 182µsec or 312µsec at 38kHz (depending on instruction)
  10µsec, 14µsec or 24µsec at 500kHz (depending on instruction)
- ROM capacity ..... 6,144 × 12 bits
- RAM capacity ..... 1,024 × 4 bits
- Input port ..... 12 bits
- Output port ..... 16 bits
- I/O port ..... 12 bits
- Serial I/O port ..... 2 ports
  - Async; half-duplex, start-stop; transmission speed at 200, 300, 600, 1200, 2400 or 4800 bps; 6 to 8-bit data length; built-in error detect circuit and built-in send/receive buffer register.
  - Clock sync.; operating by external clock; start-stop can be set by mask option.
- Built-in time base counter, programmable timer, event counter, and watchdog timer
- Built-in SVD circuit, 2 channels (internal voltage detection)
- Built-in comparator, 2 channels
- Built-in LCD drive power supply, double boosting, external adjustment of output voltage
- Interrupts ..... External : Input interrupt 3 lines
  Internal : Timer interrupt 2 lines (4ch.)
  Comparator interrupt 2 lines
  Event counter interrupt 1 line
  Serial I/O interrupt 2 lines
- Supply voltage ..... 2.2V to 5.5V
- Current consumption ..... HALT mode (38.4kHz) : 1.8µA (Typ.)
  OPERATING mode (500kHz) : 110µA (Typ.)/150µA (Max.)
- Package ..... QFP6-60pin (plastic)
  Die form

■ BLOCK DIAGRAM



■ PIN CONFIGURATION



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	P13	16	V_{SS2}	31	K20	46	V_{L1}
2	P20	17	R22	32	K21	47	V_{DD}
3	P21	18	R23	33	K22	48	OSC1
4	P22	19	R30	34	K23	49	OSC2
5	P23	20	R31	35	$\overline{RESET}$	50	V_{S1}
6	R00	21	R32	36	$\overline{TEST}$	51	OSC3
7	R01	22	R33	37	CE	52	OSC4
8	R02	23	K00	38	CD	53	V_{SS}
9	R03	24	K01	39	CC	54	P00
10	R10	25	K02	40	CB	55	P01
11	R11	26	K03	41	CA	56	P02
12	R12	27	K10	42	V_{L4}	57	P03
13	R13	28	K11	43	V_{L3}	58	P10
14	R20	29	K12	44	V_{L2}	59	P11
15	R21	30	K13	45	V_{ADJ}	60	P12

■ PIN DESCRIPTION

Pin name	Pin No.	In/Out	Function
V_{DD}	47	I	Power source (+) terminal
V_{SS}	53	I	Power source (-) terminal ...analog power source
V_{SS2}	16	I	Power source (-) terminal ...power source for output ports (R20–R23)
V_{S1}	50	–	Power source for oscillation circuit
V_{L1}	46	–	Reduction power source for LCD
V_{L2}	44	–	Power source for LCD
V_{L3}	43	–	Booster power source for LCD
V_{L4}	42	–	Booster power source for LCD
V_{ADJ}	45	I	Input terminal for setting V_L
CA–CE	41–37	–	Booster/reduction capacitor connecting terminals for LCD
OSC1	48	I	Crystal oscillation input terminal
OSC2	49	O	Crystal oscillation output terminal
OSC3	51	I	Ceramic oscillation input terminal
OSC4	52	O	Ceramic oscillation output terminal
$\overline{RESET}$	35	I	Initial reset input terminal
K00–K03	23–26	I	Input terminal
K10/V_{BLD}	27	I	Input terminal (Input terminal for setting SVD detection voltage)
K11–K12	28–29	I	Input terminal
K13/EVN	30	I	Input terminal (Event counter input terminal)
K20/SI1A	31	I	Input terminal (Serial port 1 data input terminal)
K21/SI1B	32	I	Input terminal (Serial port 1 data input terminal)
K22/SI2	33	I	Input terminal (Serial port 2 data input terminal)
K23/SCLK	34	I	Input terminal (Serial port 2 clock input terminal)
P00–P03	54–57	I/O	I/O terminal
P10/CMPP1	58	I/O	I/O terminal (Comparator 1 non-inverted input terminal)
P11/CMPM1	59	I/O	I/O terminal (Comparator 1 inverted input terminal)
P12/CMPP2	60	I/O	I/O terminal (Comparator 2 non-inverted input terminal)
P13/CMPM2	1	I/O	I/O terminal (Comparator 2 inverted input terminal)
P20–P23	2–5	I/O	I/O terminal
R00–R03	6–9	O	Output terminal
R10, R11	10, 11	O	Output terminal
R12/FOUT	12	O	Output terminal (FOUT or $\overline{BZ}$ output terminal)
R13/BZ	13	O	Output terminal (BZ or OSC3 clock output terminal)
R20–R23	14, 15, 17, 18	O	Output terminal (10 mA output available)
R30/SO1A	19	O	Output terminal (Serial port 1 data output terminal)
R31/SO1B	20	O	Output terminal (Serial port 1 data output terminal)
R32/SO2	21	O	Output terminal (Serial port 2 data output terminal)
R33/SRDY	22	O	Output terminal (Serial port 2 status output terminal)
$\overline{TEST}$	36	I	Test input terminal

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{DD}=0V)

Rating	Symbol	Value	Unit
Supply voltage (1)	V_{SS}	-7.0 to 0.5	V
Supply voltage (2)	V_{SS2}	-7.0 to V_{SS}	V
Supply voltage (3)	V_{L1}–V_{L4}	-7.0 to 0.5	V
Input voltage (1)	V_I	V_{SS} - 0.3 to 0.3	V
Input voltage (2) *1	V_{IOSC}	-2.0 to 0.3	V
Permissible total output current (1)*2	ΣI_{VSS}	15	mA
Permissible total output current (2)*2	ΣI_{VSS2}	40	mA
Operating temperature	Topr	-20 to 70	°C
Storage temperature	Tstg	-65 to 150	°C
Soldering temperature / Time	Tsol	260°C, 10sec (lead section)	–
Permissible dissipation *3	P_D	250	mW

*1: OSC1, OSC2 pin
*2: The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pins (or is draw in).
*3: In case of plastic package (QFP6-60pin).

● Recommended Operating Conditions

(Ta=-20 to 70°C)

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit
Supply voltage (1)	V_{SS}	V_{DD}=0V	-5.5		-2.2	V
Supply voltage (2) *1	V_{SS2}	V_{DD}=0V	-5.5		V_{SS}	V
Oscillation frequency (1)	f_{OSC1}		–	38.400	–	kHz
Oscillation frequency (2) *2	f_{OSC3}	duty: 50±5%	50		500	kHz
Capacitor between V_{DD} and V_{S1}	C_{S1}		0.1			µF
Capacitor between V_{DD} and V_{L1} *3	C_{L1}		0.1			µF
Capacitor between V_{DD} and V_{L2} *3	C_{L2}		0.1			µF
Capacitor between V_{DD} and V_{L3} *3	C_{L3}		0.1			µF
Capacitor between V_{DD} and V_{L4} *3	C_{L4}		0.1			µF
Capacitor between CA and CB *3	C1		0.1			µF
Capacitor between CA and CC *3	C2		0.1			µF
Capacitor between CD and CE *3	C3		0.1			µF

*1: When selecting not to use V_{SS2} power by option, you can release the V_{SS2} terminal.
*2: When selecting not to use OSC3 oscillation circuit by option, you can release the OSC3 terminal.
*3: When selecting not to use LCD drive power by option, you can release the above capacitors are not required. However, you should connect V_{L1}–V_{L4} terminals with the V_{DD} and release the CA–CE and V_{ADJ} terminals.

● DC Characteristics

(Unless otherwise specified: V_{DD}=0V, V_{SS}(V_{SS2})=-2.2 to -5.5V, Ta=25°C)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–03•10–13•20–23 P00–03•10–13•20–23	0.2•V_{SS}		0	V
High level input voltage (2)	V_{IH2}		$\overline{RESET}$	0.1•V_{SS}		0	V
Low level input voltage (1)	V_{IL1}		K00–03•10–13•20–23 P00–03•10–13•20–23	V_{SS}		0.8•V_{SS}	V
Low level input voltage (2)	V_{IL2}		$\overline{RESET}$	V_{SS}		0.9•V_{SS}	V
High level input current	I_{IH}	V_{IH}=V_{DD}	K00–03•10–13•20–23 P00–03•10–13•20–23 $\overline{RESET}$, $\overline{TEST}$			0.5	µA
Low level input current (1)	I_{IL1}	V_{IL1}=V_{SS} No pull up resistor	K00–03•10–13•20–23 P00–03•10–13•20–23	-0.5			µA
Low level input current (2)	I_{IL2}	V_{IL2}=V_{SS} With pull up resistor	K00–03•10–13•20–23	-20		-3	µA
Low level input current (3)	I_{IL3}	V_{IL3}=V_{SS} With pull up resistor	P00–03•10–13•20–23	-30		-3	µA
Low level input current (4)	I_{IL4}	V_{IL4}=V_{SS}	$\overline{RESET}$	-20		-0.5	µA
Low level input current (5)	I_{IL5}	V_{IL5}=0.1•V_{SS}	$\overline{RESET}$	-100			µA
High level output current (1)	I_{OH1}	V_{OH1}=0.1•V_{SS}	R00–03•10–13•30–33•40–43 P00–03•10–13•20–23			-300	µA
High level output current (2)	I_{OH2}	V_{OH2}=0.1•V_{SS2}	R20–23			-300	µA
Low level output current (1)	I_{OL1}	V_{OL1}=0.9•V_{SS}	R00–03•10–13•30–33•40–43 P00–03•10–13•20–23	500			µA
Low level output current (2)	I_{OL2}	V_{OL2}=0.9•V_{SS2}	R20–23	5			mA

● Analog Circuit Characteristics and Current Consumption

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-2.2 to -5.5V, f_{OSC1}=38.4kHz(crystal), f_{OSC3}=500kHz(ceramic), Ta=25°C, C_G=10pF, C_{GC}/C_{DC}=108pF, $V_{ADJ}=V_{L2}$, RA1/RA2=1MΩ, C_{S1}/C_{L1}–C_{L4}/C1–C3=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage *1	V_{L1}	Connect 1MΩ load resistor between V_{DD} and V_{L1} (No panel load), V_{SS}=-2.5 to -5.5V		0.50 ×V_{L2}		0.45 ×V_{L2}	V
	V_{L2}	Connect 1MΩ load resistor between V_{DD} and V_{L2} (No panel load), V_{SS}=-2.5 to -5.5V		-2.25	-2.10	-1.95	V
	V_{L3}	Connect 1MΩ load resistor between V_{DD} and V_{L3} (No panel load), V_{SS}=-2.5 to -5.5V		1.50 ×V_{L2}		1.45 ×V_{L2}	V
	V_{L4}	Connect 1MΩ load resistor between V_{DD} and V_{L4} (No panel load), V_{SS}=-2.5 to -5.5V		2.00 ×V_{L2}		1.95 ×V_{L2}	V
BLD voltage (internal)	V_{BLD1}			-2.50	-2.35	-2.20	V
BLD voltage (external)	V_{BLD2}			-1.13	-1.05	-0.97	V
BLD circuit stability time *2	t_{BLD}					100	µS
BLD circuit current consumption	I_{BLD}	V_{SS}=-3.0V			10	20	µA
Analog comparator input voltage	V_{IP}	Noninverted input (CMPP)		V_{SS}+0.3		-1.0	V
	V_{IM}	Inverted input (CMPM)					
Analog comparator offset voltage	V_{OF}	V_{IP}=-1.0 to V_{SS}+0.3V V_{IM}=-1.0 to V_{SS}+0.3V				50	mV
Analog comparator stabilizing time *2	t_{CMP1}	V_{IP}=-1.0 to V_{SS}+0.3V V_{IM}=-1.0 to V_{SS}+0.3V				100	µS
Analog comparator response time	t_{CMP2}	V_{SS}=-2.2V V_{IP}=-1.1V, V_{IM}=-1.1±0.1V				100	µS
Analog comparator current consumption (1)	I_{CMP1}	V_{SS}=-3.0V V_{IP}=-1.4V, V_{IM}=-1.6V			4	10	µA
Analog comparator current consumption (2)	I_{CMP2}	V_{SS}=-3.0V V_{IP}=-1.6V, V_{IM}=-1.4V			8	15	µA
Current consumption	I_{OP}	During HALT (1) *3	OSCC="0"		1.8	4.0	µA
		During HALT (2) *4	No panel load		1.3	3.0	µA
		During operation at 38.4kHz *3			9	15	µA
		During operation at 500kHz *5	No panel load		110	150	µA

∗1: When selecting not to use LCD drive power by option, V_{DD} (=0V) is output to V_{L2}.
∗2: The stabilizing time is the time from turning the circuit on until the output data stabilizes.
∗3: The time base counter is RUN status, programmable timer, BLD circuit and analog comparator are OFF status, and the input and output terminals are static status.
∗4: The same status as ∗1 and is when not using LCD drive power by option, and selecting DC output to the R12 port output form.
∗5: The BLD circuit and analog comparator are OFF status and the input and output terminals are static status.

● Oscillation Characteristics

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

OSC1 crystal oscillation circuit

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-2.2 to -5.5V, Crystal: C2-TYPE(Seiko Epson), C_G=25pF, C_D=built-in, Ta=25°C)

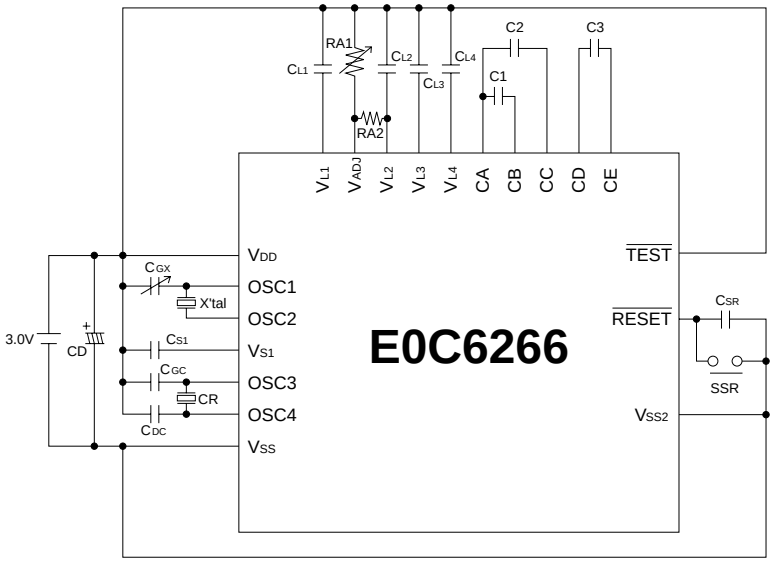
Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	t_{sta}	V_{SS}=-2.2 to -5.5V			3	Sec
Built-in capacitance (drain)	C_D	For 60 pin plastic package	–	20	–	pF
Frequency/voltage deviation	∂f/∂V	V_{SS}=-2.2 to -5.5V			5	ppm
Frequency/IC deviation	∂f/∂IC		-10		10	ppm
Frequency adjustment range	∂f/∂C_G	C_G=5 to 25pF	40			ppm
Permitted leak resistance	R_{leak}	Between OSC1 and V_{DD}, V_{S1}	200			MΩ

OSC3 ceramic oscillation circuit

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-2.2 to -5.5V, Ceramic: CSB500E(Murata Mfg. Co.), C_{GC}=C_{DC}=108pF, Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	t_{sta}	V_{SS}=-2.2 to -5.5V		4	10	mS

■ BASIC EXTERNAL CONNECTION DIAGRAM

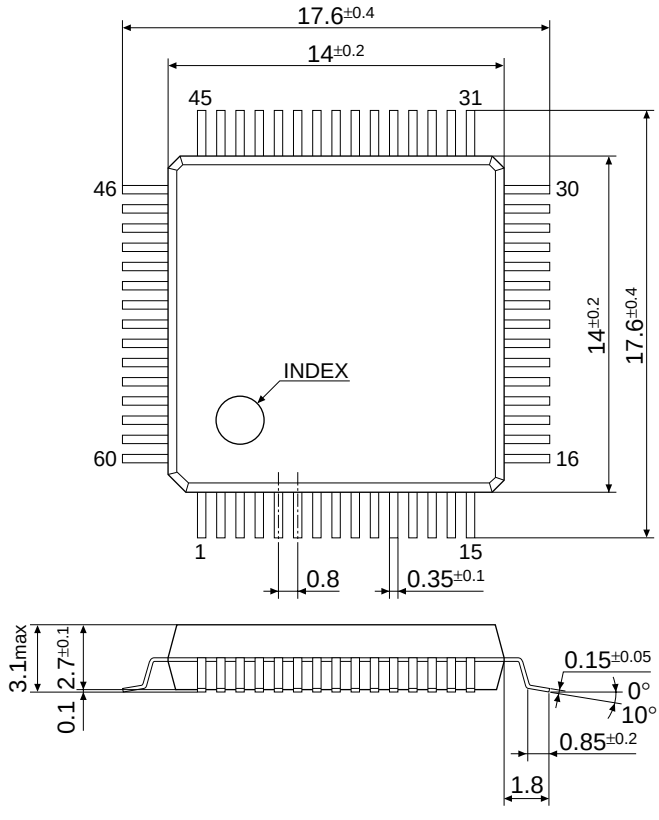


X'tal	Crystal oscillator	38.4kHz
C_{GX}	Trimmer capacitor	5~25pF
CR	Ceramic oscillator	500kHz
C_{GC}		108pF
C_{DC}		108pF
C_{SR}		3.3µF
RA1, RA2		1MΩ
C_{L1}~C_{L4}		0.1µF
C1~C3		0.1µF
C_{S1}		0.1µF
CD		6.8µF

Note: The above table is simply an example, and is not guaranteed to work.

■ PACKAGE DIMENSIONS

Plastic QFP6-60pin



Unit: mm

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