Data Sheet
October 1993

AT&T Microelectronics

# ATT3000 Series Field-Programmable Gate Arrays (–50, –70, –100, –125, and –150 MHz)

## Features

- High performance—up to 150 MHz toggle rates
- User-programmable gate array:
  - — I/O functions
  - — Digital logic functions
  - — Interconnections
- Flexible array architecture:
  - — Compatible arrays, 2000 to 9000 gate logic complexity
  - — Extensive register and I/O capabilities
  - — High fan-out signal distribution
  - — Internal 3-state bus capabilities
  - — TTL or CMOS input thresholds
  - — On-chip oscillator amplifier
- Standard product availability:
  - — Low-power submicron CMOS, static memory technology
  - — Pin-for-pin compatible with *Xilinx XC3000** and *XC3100* family
  - — Cost-effective, high-speed FPGAs
  - — 100% factory pretested
  - — Selectable configuration modes
- *NeoCAD*† or *XACT** development system support
- Commercial, industrial, military FPGAs processed on a QML-certified line
- Standard military drawings (SMDs):
  - — ATT3020 (SMD No. 5962-89948)
  - — ATT3042 (SMD No. 5962-89713)
  - — ATT3090 (SMD No. 5962-89823)

* *Xilinx*, *XC3000*, *XC3100*, and *XACT* are registered trademarks of Xilinx, Inc.
† *NeoCAD* is a trademark of NeoCAD, Inc.

## Description

The CMOS ATT3000 Series Field-Programmable Gate Array (FPGA) family provides a group of high-density, digital integrated circuits. Their regular, extendable, flexible, user-programmable array architecture is composed of a configuration program store plus three types of configurable elements: a perimeter of I/O blocks, a core array of logic blocks, and resources for interconnection. The general structure of an FPGA is shown in Figure 2.

The *XACT* and *NeoCAD* development systems provide auto place-and-route of netlists. Logic and timing simulation are available as design verification alternatives. The design editor is used for interactive design optimization and to compile the data pattern which represents the configuration program.

The FPGA's user logic functions and interconnections are determined by the configuration program data stored in internal static memory cells. The program can be loaded in any of several modes to accommodate various system requirements. The program data resides externally in an EEPROM, EPROM, or ROM on the application circuit board, or on a floppy disk or hard disk. On-chip initialization logic provides for optional automatic loading of program data at powerup. A serial configuration PROM can provide a very simple serial configuration program storage.

**Table 1. ATT3000 Series FPGAs**

| FPGA | Logic Capacity (Available Gates) | Configurable Logic Blocks | User I/Os | Program Data (Bits) |
|---|---|---|---|---|
| ATT3020 | 2000 | 64 | 64 | 14779 |
| ATT3030 | 3000 | 100 | 80 | 22176 |
| ATT3042 | 4200 | 144 | 96 | 30784 |
| ATT3064 | 6400 | 224 | 120 | 46064 |
| ATT3090 | 9000 | 320 | 144 | 64160 |

The ATT3000 series FPGAs are an enhanced family of field-programmable gate arrays, which provide a variety of logic capacities, package styles, temperature ranges, and speed grades. The ATT3020, ATT3042, and ATT3090 are available as military products with up to 125 MHz toggle rates.

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## Architecture

The perimeter of configurable I/O blocks (IOBs) provides a programmable interface between the internal logic array and the device package pins. The array of configurable logic blocks (CLBs) performs user-specified logic functions. The interconnect resources are programmed to form networks, carrying logic signals among blocks, analogous to printed-circuit board traces connecting MSI/SSI packages.

The blocks' logic functions are implemented by programmed look-up tables. Functional options are implemented by program-controlled multiplexers. Interconnecting networks between blocks are implemented with metal segments joined by program-controlled pass transistors. These functions of the FPGA are established by a configuration program which is loaded into an internal, distributed array of configuration memory cells. The configuration program is loaded into the FPGA at powerup and may be reloaded on command. The FPGA includes logic and control signals to implement automatic or passive configuration. Program data may be either bit serial or byte parallel. The *XACT* development system generates the configuration program bit-stream used to configure the FPGA. The memory loading process is independent of the user logic functions.

## Configuration Memory

The static memory cell used for the configuration memory in the FPGA has been designed specifically for high reliability and noise immunity. Integrity of the FPGA configuration memory based on this design is assured even under various adverse conditions. Compared with other programming alternatives, static memory is believed to provide the best combination of high density, high performance, high reliability and comprehensive testability. As shown in Figure 1, the basic memory cell consists of two CMOS inverters plus a pass transistor used for writing and reading cell data. The cell is only written to during configuration and only read fromduring readback. During normal operation, the cell provides continuous control and the pass transistor is off and does not affect cell stability. This is quite different from the operation of conventional memory devices, in which the cells are frequently read and rewritten.

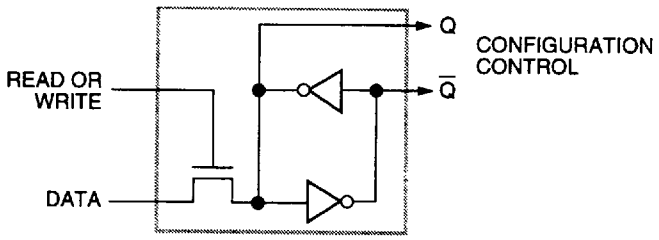



**Figure 1. Static Configuration Memory Cell**

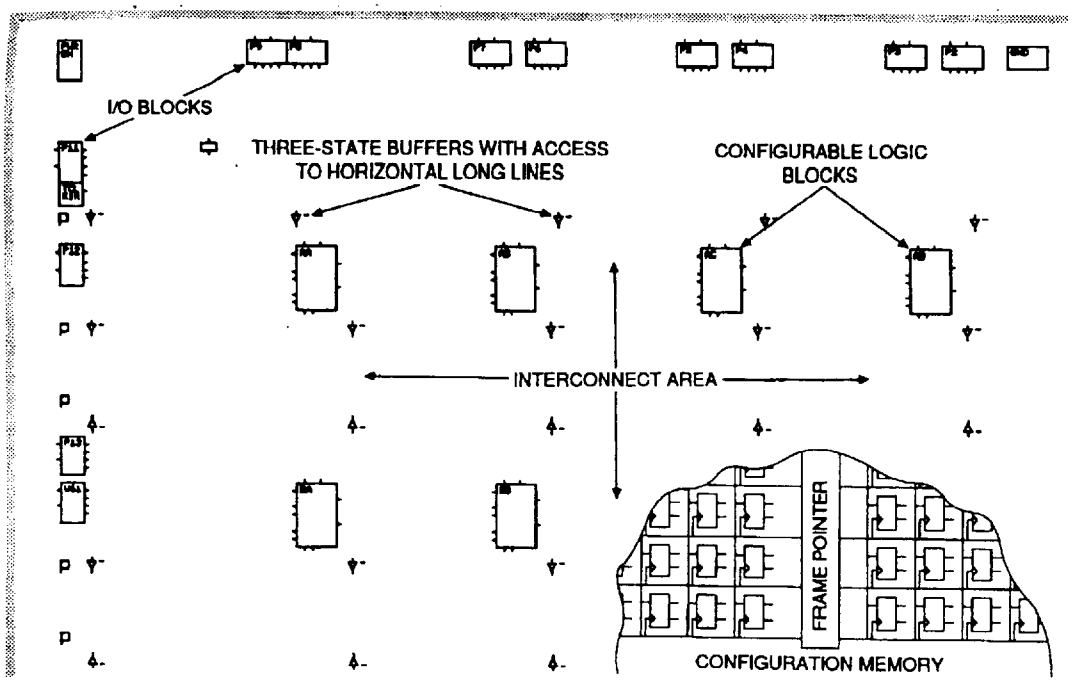



**Figure 2. Field-Programmable Gate Array Structure**

## Configuration Memory (continued)

The memory cell outputs Q and $\overline{Q}$ use full Ground and Vcc levels and provide continuous, direct control. The additional capacitive load and the absence of address decoding and sense amplifiers provide high stability to the cell. Due to their structure, the configuration memory cells are not affected by extreme power supply excursions or very high levels of alpha particle radiation. Soft errors have not been observed in reliability testing.

Two methods of loading configuration data use serial data, while three use byte-wide data. The internal configuration logic utilizes framing information, embedded in the program data by the *XACT* development system, to direct memory cell loading. The serial data framing and length count preamble provide programming compatibility for mixes of various AT&T programmable gate arrays in a synchronous, serial, daisy-chain fashion.

## I/O Block

Each user-configurable I/O block (IOB), shown in Figure 3, provides an interface between the external package pin of the device and the internal user logic. Each IOB includes both registered and direct input paths and a programmable 3-state output buffer which may be driven by a registered or direct output signal. Configuration options allow each IOB an inversion, a controlled slew rate, and a high-impedance pull-up. Each input circuit also provides input clamping diodes to provide electrostatic protection and circuits to inhibit latch-up produced by input currents.

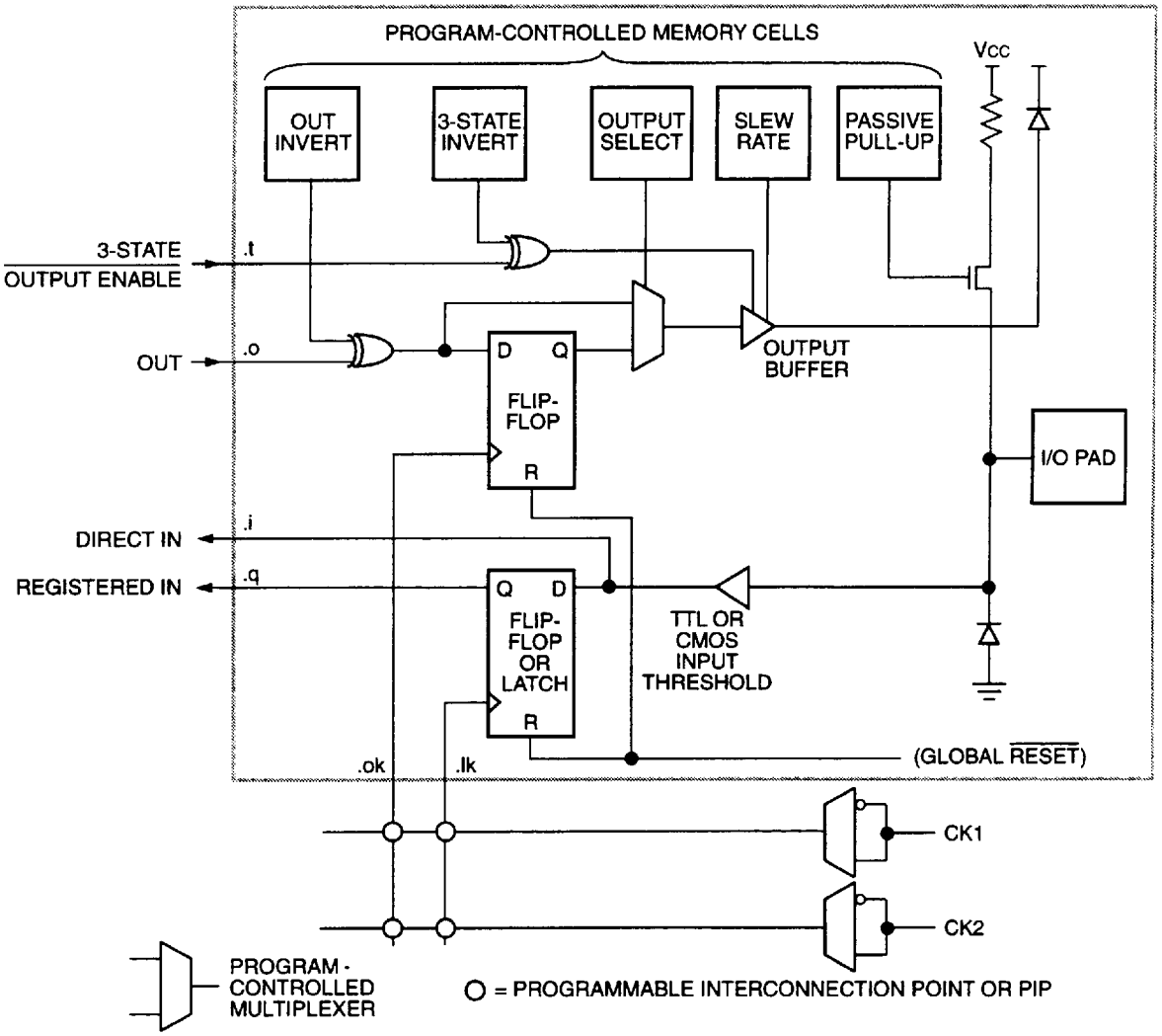



**Figure 3. Input/Output Block**

## I/O Block (continued)

The input buffer portion of each IOB provides threshold detection to translate external signals applied to the package pin to internal logic levels. The global input-buffer threshold of the IOB can be programmed to be compatible with either TTL or CMOS levels. The buffered input signal drives the data input of a storage element which may be configured as a positive edge-triggered D flip-flop or a low level-transparent latch. The sense of the clock can be inverted (negative edge/high transparent) as long as all IOBs on the same clock net use the same clock sense. Clock/load signals (IOB pins .ik and .ok) can be selected from either of two die edge metal lines. I/O storage elements are reset during configuration or by the active-low chip $\overline{\text{RESET}}$ input. Both direct input (from I/O block pin .i) and registered input (from IOB pin .q) signals are available for interconnect.

For reliable operation, inputs should have transition times of less than 100 ns and should not be left floating. Floating CMOS input-pin circuits might be at threshold and produce oscillations. This can produce additional power dissipation and system noise. A typical hysteresis of about 200 mV reduces sensitivity to input noise. Each user IOB includes a programmable high-impedance pull-up resistor which is selected by the program to provide a constant high for otherwise undriven package pins. Normal CMOS handling precautions should be observed.

Flip-flop loop delays for the IOB and logic block flip-flops are approximately 3 ns. This short delay provides good performance under asynchronous clock and data conditions. Short loop delays minimize the probability of a metastable condition which can result from assertion of the clock during data transitions. Because of the short loop delay characteristic in the FPGA, the IOB flip-flops can be used to synchronize external signals applied to the device. When synchronized in the IOB, the signals can be used internally without further consideration of their clock relative timing, except as it applies to the internal logic and routing path delays.

Output buffers of the IOBs provide CMOS-compatible 4 mA source-or-sink drive for high fan-out CMOS or TTL compatible signal levels. The network driving IOB pin .o becomes the registered or direct data source for the output buffer. The 3-state control signal (IOB pin .t) can control output activity. An open-drain type output may be obtained by using the same signal for driving the output and 3-state signal nets so that the buffer output is enabled only for a LOW.

Configuration program bits for each IOB control features such as optional output register, logical signal inversion, and 3-state and slew rate control of the output.

The program-controlled memory cells of Figure 3 control the following options:

- Logical inversion of the output is controlled by one configuration program bit per IOB.
- Logical 3-state control of each IOB output buffer is determined by the states of configuration program bits which turn the buffer on, or off, or select the output buffer 3-state control interconnection (IOB pin .t). When this IOB output control signal is high, a logic 1, the buffer is disabled and the package pin is high impedance. When this IOB output control signal is low, a logic 0, the buffer is enabled and the package pin is active. Inversion of the buffer 3-state control logic sense (output enable) is controlled by an additional configuration program bit.
- Direct or registered output is selectable for each IOB. The register uses a positive-edge, clocked flip-flop. The clock source may be supplied (IOB pin .ok) by either of two metal lines available along each die edge. Each of these lines is driven by an invertible buffer.
- Increased output transition speed can be selected to improve critical timing. Slower transitions reduce capacitive load peak currents of noncritical outputs and minimize system noise.
- A high-impedance pull-up resistor may be used to prevent unused inputs from floating.

### Summary of I/O Options

- Inputs
  - Direct
  - Flip-flop/latch
  - CMOS/TTL threshold (chip inputs)
  - Pull-up resistor/open circuit
- Outputs
  - Direct/registered
  - Inverted/not
  - 3-state/on/off
  - Full speed/slew limited
  - 3-state/output enable (inverse)

## Configurable Logic Block

The array of configurable logic blocks (CLBs) provides the functional elements from which the user's logic is constructed. The logic blocks are arranged in a matrix within the perimeter of IOBs. The ATT3020 has 64 such blocks arranged in eight rows and eight columns. The *XACT* or *NeoCAD* development systems are used to compile the configuration data which are to be loaded into the internal configuration memory to define the operation and interconnection of each block. User definition of CLBs and their interconnecting networks may be done by automatic translation from a schematic capture logic diagram or optionally by installing library or user macros.

Each CLB has a combinatorial logic section, two flip-flops, and an internal control section. See Figure 4 below. There are five logic inputs (.a, .b, .c, .d, and .e); a common clock input (.k); an asynchronous direct reset input (.rd); and an enable clock (.ec). All may be driven from the interconnect resources adjacent to the blocks. Each CLB also has two outputs (.x and .y) which may drive interconnect networks.

Data input for either flip-flop within a CLB is supplied from the function F or G outputs of the combinatorial logic, or the block input, data-in (.di). Both flip-flops in each CLB share the asynchronous reset (.rd) which, when enabled and high, is dominant over clocked inputs. All flip-flops are reset by the active-low chip input, $\overline{\text{RESET}}$, or during the configuration process.

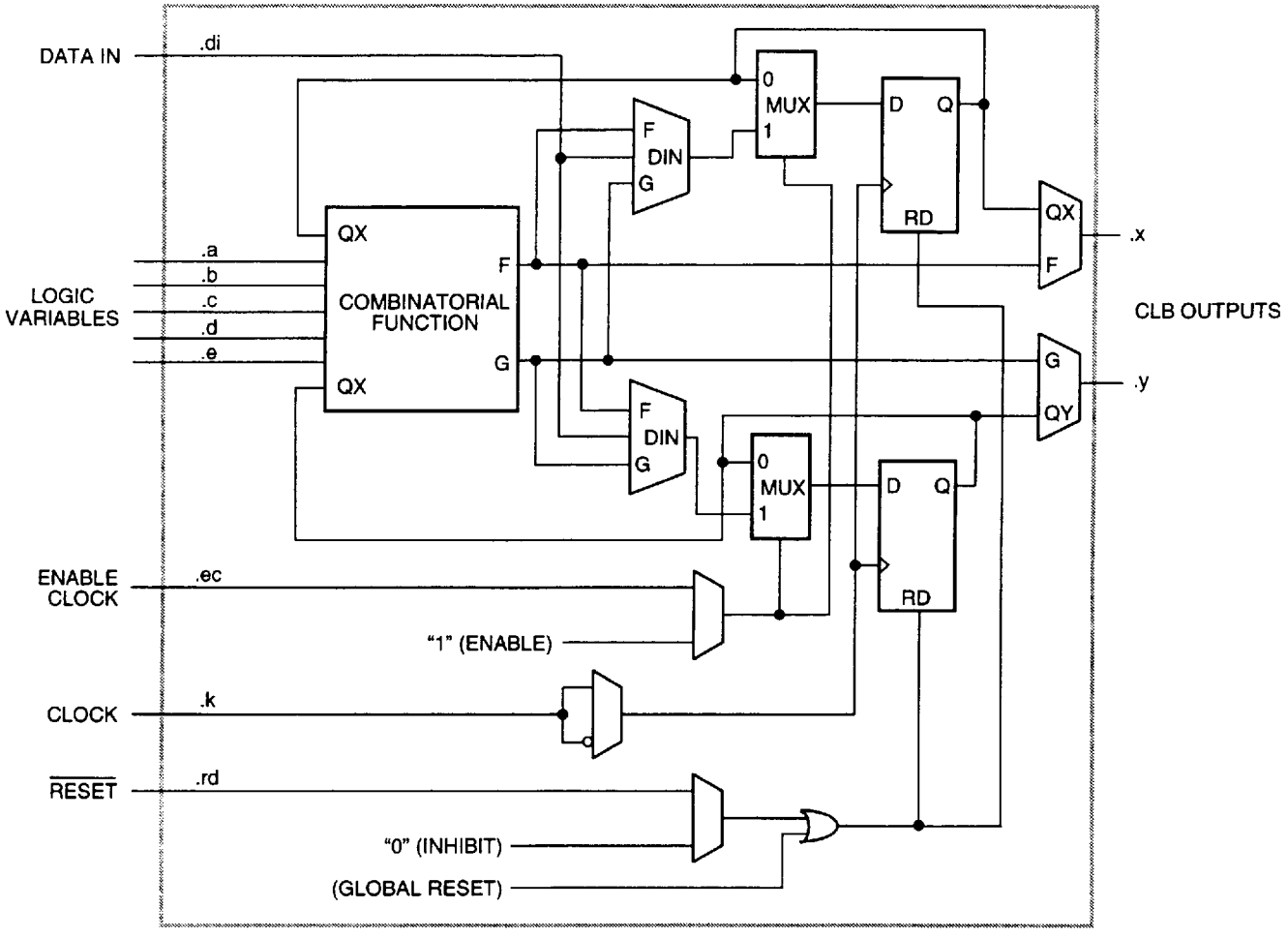
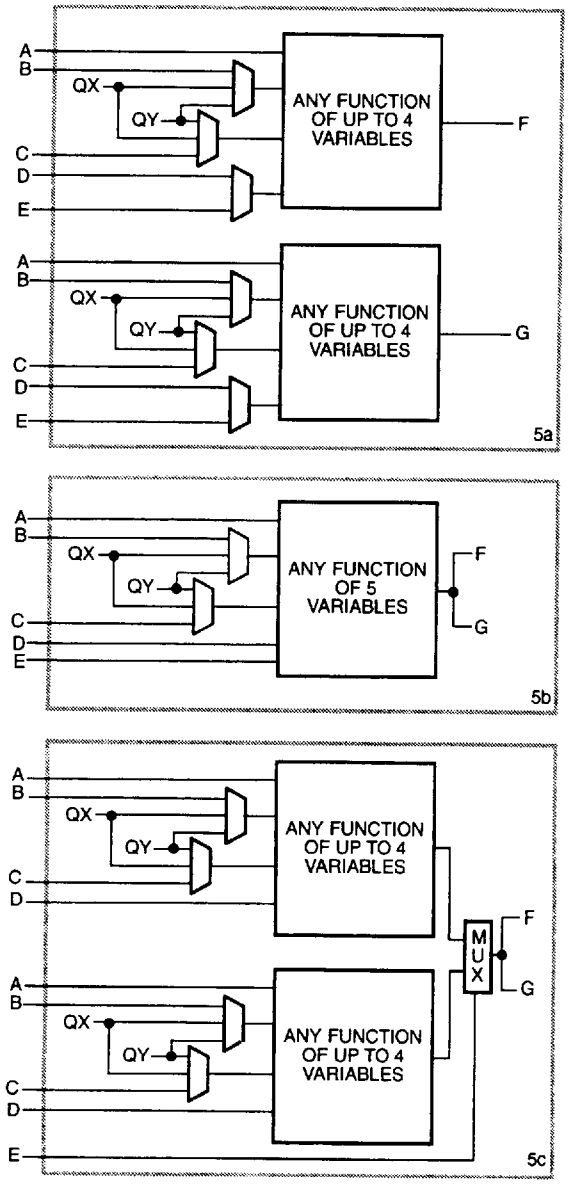



**Figure 4. Configurable Logic Block**

## Configurable Logic Block (continued)




**5A.** **Combinatorial Logic Option 1** generates two functions of four variables each. One variable, A, must be common to both functions. The second and third variables can be any choice among B, C, Qx, and Qy. The fourth variable can be any choice of D or E.

**5B.** **Combinatorial Logic Option 2** generates any function of five variables: A, D, E, and two choices among B, C, Qx, Qy.

**5C.** **Combinatorial Logic Option 3** allows variable E to select between two functions of four variables: both have common inputs, A and D, and any choice among B, C, Qx, and Qy for the remaining two variables. Option 3 can then implement some functions of six or seven variables.

**Figure 5. Combinatorial Logic Diagram**

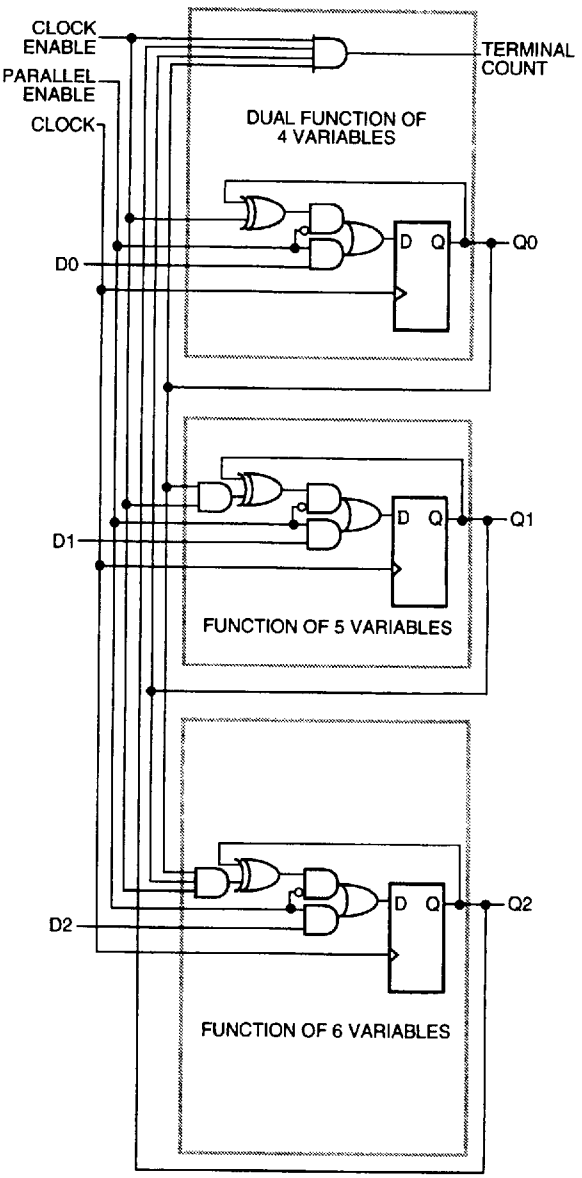



**Figure 6. C8BCP Macro**

The flip-flops share the enable clock (.ec) which, when low, recirculates the flip-flops' present states and inhibits its response to the data-in or combinatorial function inputs on a CLB. The user may enable these control inputs and select their sources. The user may also select the clock net input (.k), as well as its active sense within each logic block. This programmable inversion eliminates the need to route both phases of a clock signal throughout the device. Flexible routing allows use of common or individual CLB clocking.

## Configurable Logic Block (continued)

The combinatorial logic portion of the logic block uses a 32 x 1 look-up table to implement Boolean functions. Variables selected from the five logic inputs and two internal block flip-flops are used as table address inputs. The combinatorial propagation delay through the network is independent of the logic function generated and is spike-free for single-input variable changes. This technique can generate two independent logic functions of up to four variables each as shown in Figure 5A, or a single function of five variables as shown in Figure 5B, or some functions of seven variables as shown in Figure 5C (see page 6).

Figure 6 on page 7 shows a modulo 8 binary counter with parallel enable. It uses one CLB of each type. The partial functions of six or seven variables are implemented by using the input variable (.e) to dynamically select between two functions of four different variables. For the two functions of four variables each, the independent results (F and G) may be used as data inputs to either flip-flop or either logic block output. For the single function of five variables and merged functions of six or seven variables, the F and G outputs are identical. Symmetry of the F and G functions and the flip-flops allows the interchange of CLB outputs to optimize routing efficiencies of the networks interconnecting the logic and IOBs.

## Programmable Interconnect

Programmable interconnection resources in the FPGA provide routing paths to connect inputs and outputs of the IOBs and logic blocks into logical networks. Interconnections between blocks are composed from a two-layer grid of metal segments. Special designed pass transistors, each controlled by a configuration bit, form programmable interconnect points (PIPs) and switching matrices used to implement the necessary connections between selected metal segments and block pins. Figure 7 is an example of a routed net. The *XACT* development system provides automatic routing of these interconnections. Interactive routing (Editnet) is also available for design optimization. The inputs of the logic or IOBs are multiplexers which can be programmed to select an input network from the adjacent interconnect segments. Since the switch connections to block inputs are unidirectional (as are block outputs), they are usable only for block input connection and not routing. Figure 8 on page 9 illustrates routing access to logic block input variables, control inputs, and block outputs.

Three types of metal resources are provided to accommodate various network interconnect requirements:

- General-purpose interconnect
- Direct connection
- Long lines (multiplexed buses and wide-AND gates)

### General-Purpose Interconnect

General-purpose interconnect, as shown in Figure 9 on page 10, consists of a grid of five horizontal and five vertical metal segments located between the rows and columns of logic and IOBs. Each segment is the height or width of a logic block. Switching matrices join the ends of these segments and allow programmed interconnections between the metal grid segments of adjoining rows and columns. The switches of an unprogrammed device are all nonconducting. The connections through the switch matrix may be established by the automatic routing or by using Editnet to select the desired pairs of matrix pins to be connected or disconnected. The legitimate switching matrix combinations for each pin are indicated in Figure 10 on page 10 and may be highlighted by the use of the show matrix command in *XACT*.

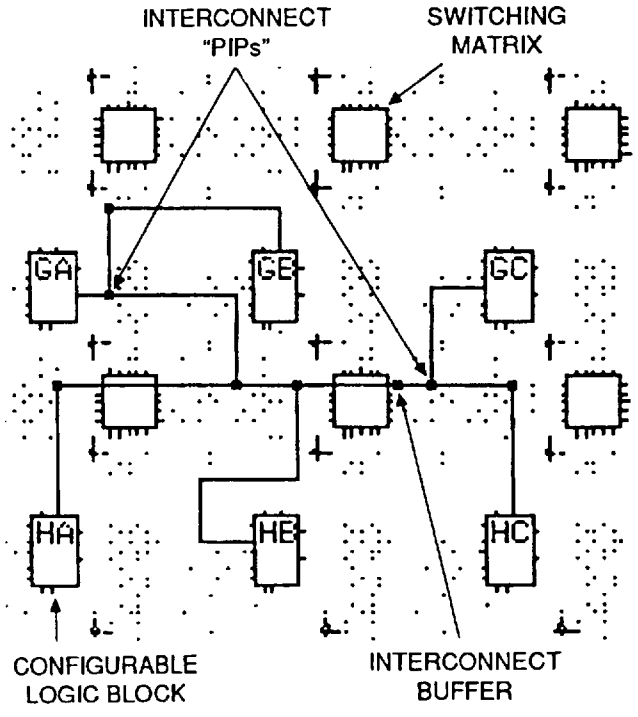



**Figure 7. *XACT* View of Routing Resources**

## Programmable Interconnect (continued)

Special buffers within the general interconnect areas provide periodic signal isolation and restoration for improved performance of lengthy nets. The interconnect buffers are available to propagate signals in either direction on a given general interconnect segment. These bidirectional (bidi) buffers are found adjacent to the switching matrices, above and to the right, and may be highlighted by the use of the "Show BIDI" command in *XACT*. The other PIPs adjacent to the matrices are accessed to or from long lines. The development system automatically defines the buffer direction based on the location of the interconnection network source. The delay calculator of the *XACT* development system automatically calculates and displays the block, interconnect, and buffer delays for any paths selected. Generation of the simulation netlist with a worst-case delay model is provided by an *XACT* option.

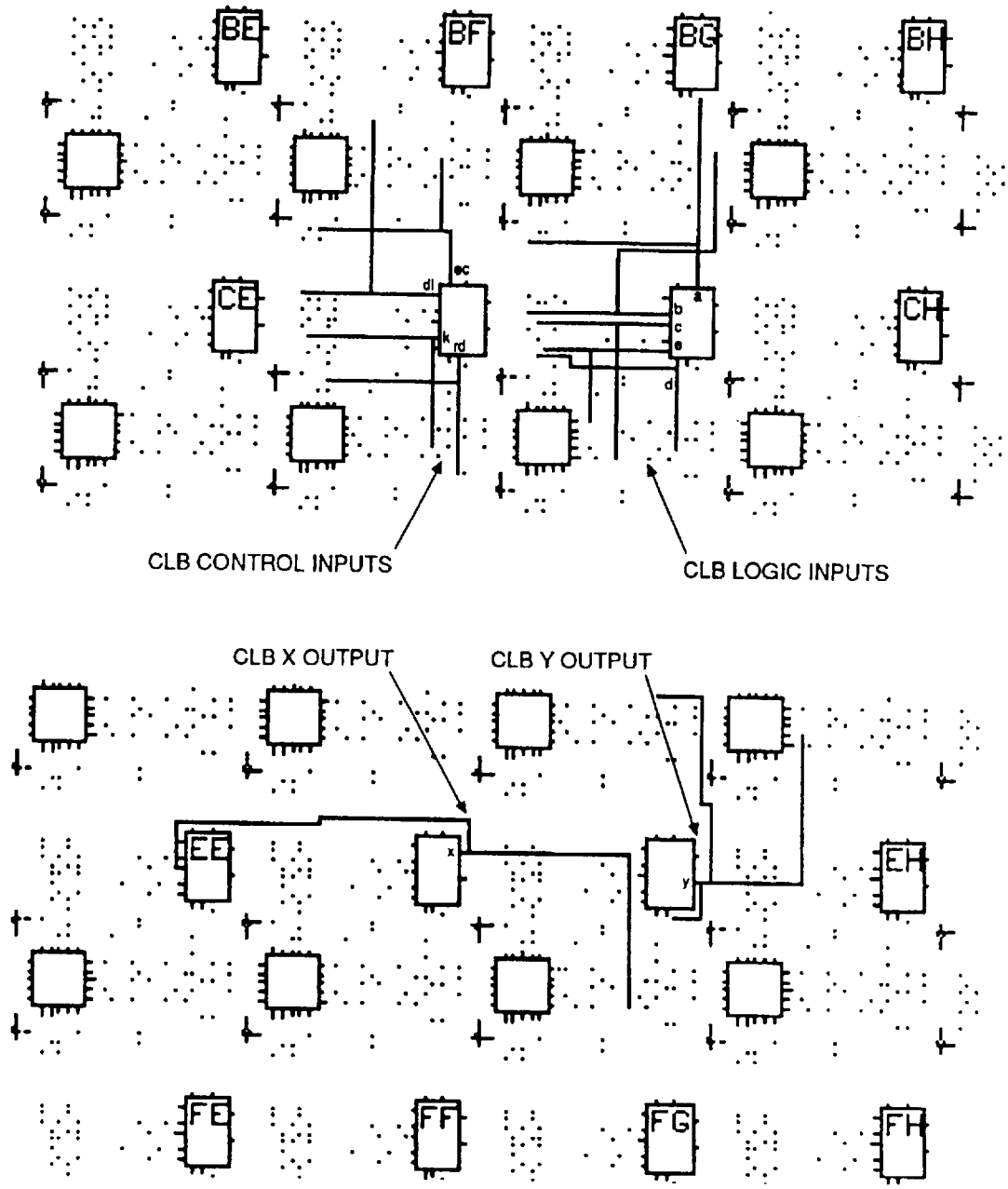



**Figure 8. AT&T *XACT* Development System**

## Programmable Interconnect (continued)

Some of the interconnect PIPs are directional. This is indicated on the *XACT* design editor status line:

- ND is a nondirectional interconnection.
- D:H->V is a PIP which drives from a horizontal to a vertical line.
- D:V->H is a PIP which drives from a vertical to a horizontal line.
- D:C->T is a "T" PIP which drives from a cross of a T to the tail.
- D:CW is a corner PIP which drives in the clockwise direction.
- P0 indicates the PIP is nonconducting, P1 is "on."

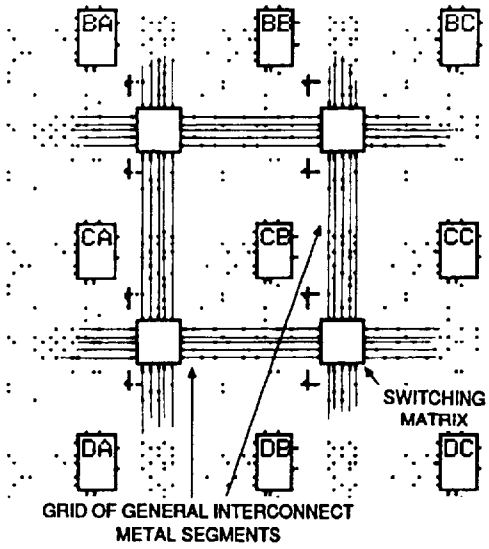



**Figure 9. FPGA General-Purpose Interconnect**

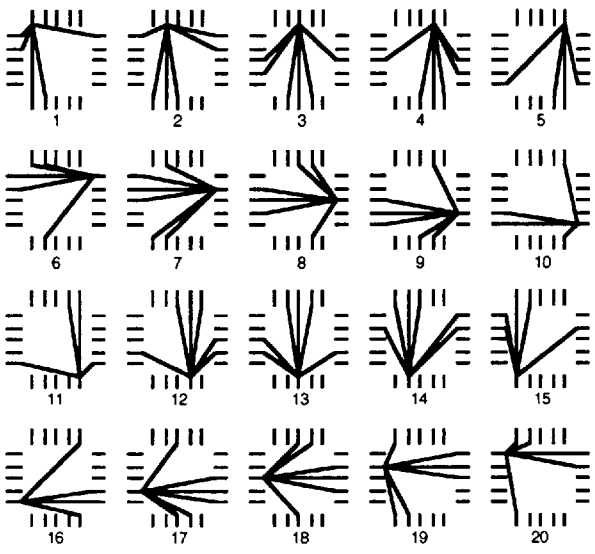



**Figure 10. Switch Matrix Interconnection Options**

## Direct Interconnect

Direct interconnect (shown in Figure 11) provides the most efficient implementation of networks between adjacent logic or IOBs. Signals routed from block to block using the direct interconnect exhibit minimum interconnect propagation and use no general interconnect resources. For each CLB, the .x output may be connected directly to the .b input of the CLB immediately to its right and to the .c input of the CLB to its left. The .y output can use direct interconnect to drive the .d input of the block immediately above, and the .a input of the block below. Direct interconnect should be used to maximize the speed of high-performance portions of logic. Where logic blocks are adjacent to IOBs, direct connect is provided alternately to the IOB inputs (.i), and outputs (.o) on all four edges of the die. The right edge provides additional direct connects from CLB outputs to adjacent IOBs. Direct interconnections of IOBs with CLBs are shown in Figure 12 on page 11.

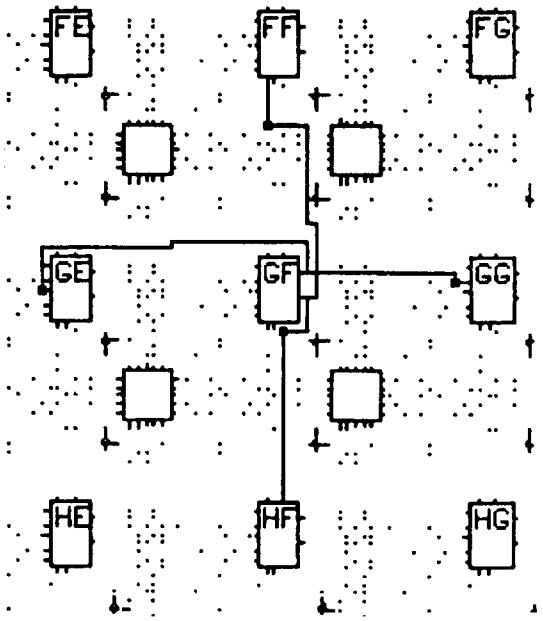



**Figure 11. Direct Interconnect**

## Programmable Interconnect (continued)

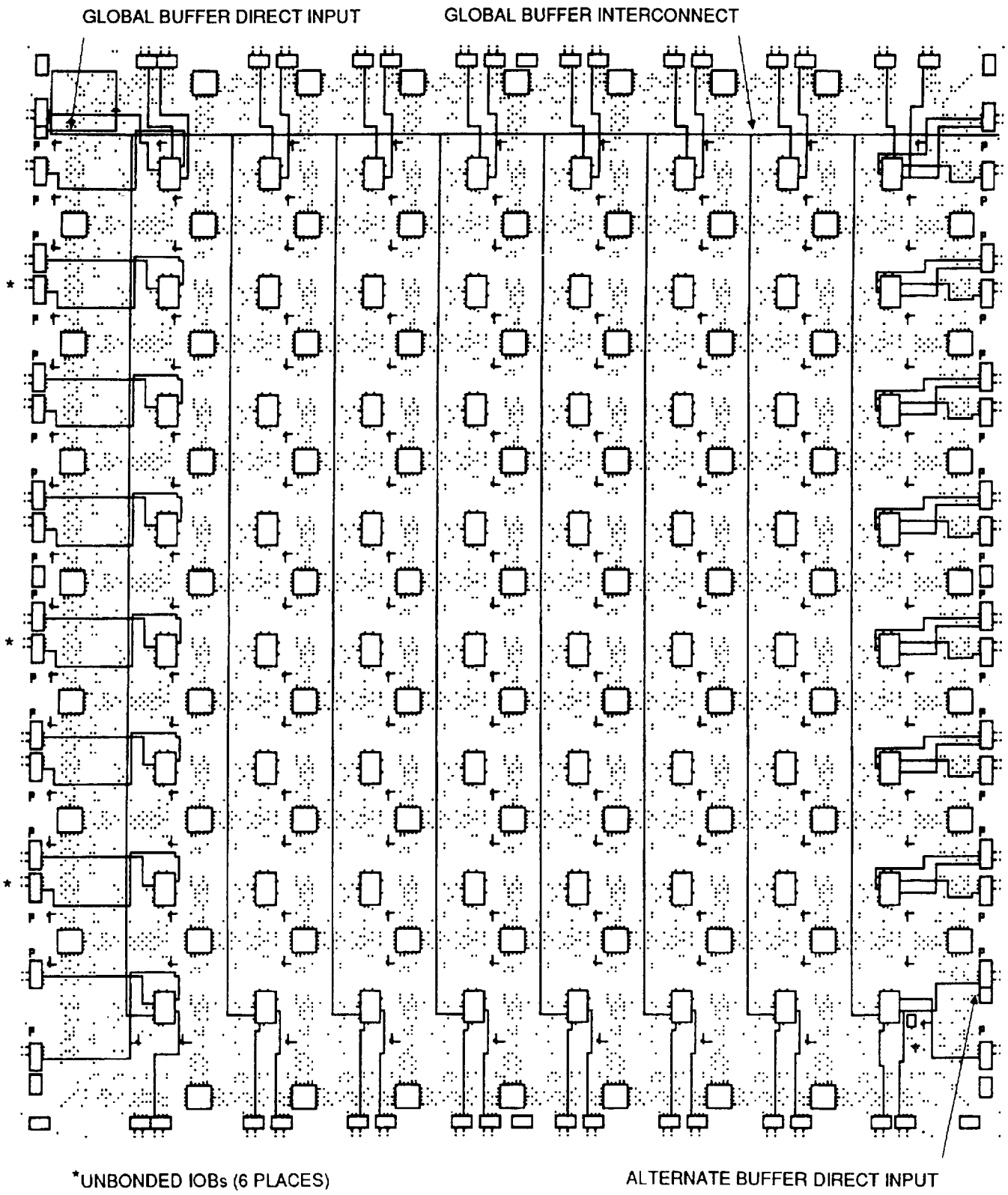



**Figure 12. ATT3020 Die Edge I/O Blocks with Direct Access to Adjacent CLB**

## Programmable Interconnect (continued)

### Long Lines

The long lines bypass the switch matrices and are intended primarily for signals which must travel a long distance, or must have minimum skew among multiple destinations. Long lines, shown in Figure 13, run vertically and horizontally the height or width of the interconnect area. Each interconnection column has three vertical long lines, and each interconnection row has two horizontal long lines. An additional two long lines are located adjacent to the outer sets of switching matrices. Two vertical long lines in each column are connectable half-length lines, except on the ATT3020, where only the outer long lines serve that function.

Long lines can be driven by a logic block or IOB output on a column-by-column basis. This capability provides a common low-skew control or clock line within each column of logic blocks. Interconnections of these long lines are shown in Figure 14 on page 13. Isolation buffers are provided at each input to a long line and are enabled automatically by the development system when a connection is made.

A buffer in the upper left corner of the FPGA chip drives a global net which is available to all .k inputs of logic blocks. Using the global buffer for a clock signal provides a skew-free, high fan-out, synchronized clock for use at any or all of the I/O and logic blocks. Configuration bits for the .k input to each logic block can select this global line, or another routing resource, as the clock source for its flip-flops. This net may also be programmed to drive the die edge clock lines for IOB use. An enhanced speed, CMOS threshold, offers direct access to this buffer and is available at the second pad from the top of the left die edge.

A buffer in the lower right corner of the array drives a horizontal long line that can drive programmed connections to a vertical long line in each interconnection column. This alternate buffer also has low skew and high fan-out. The network formed by this alternate buffer's long lines can be selected to drive the .k inputs of the logic blocks. CMOS threshold, high-speed access to this buffer is available from the third pad from the bottom of the right die edge.

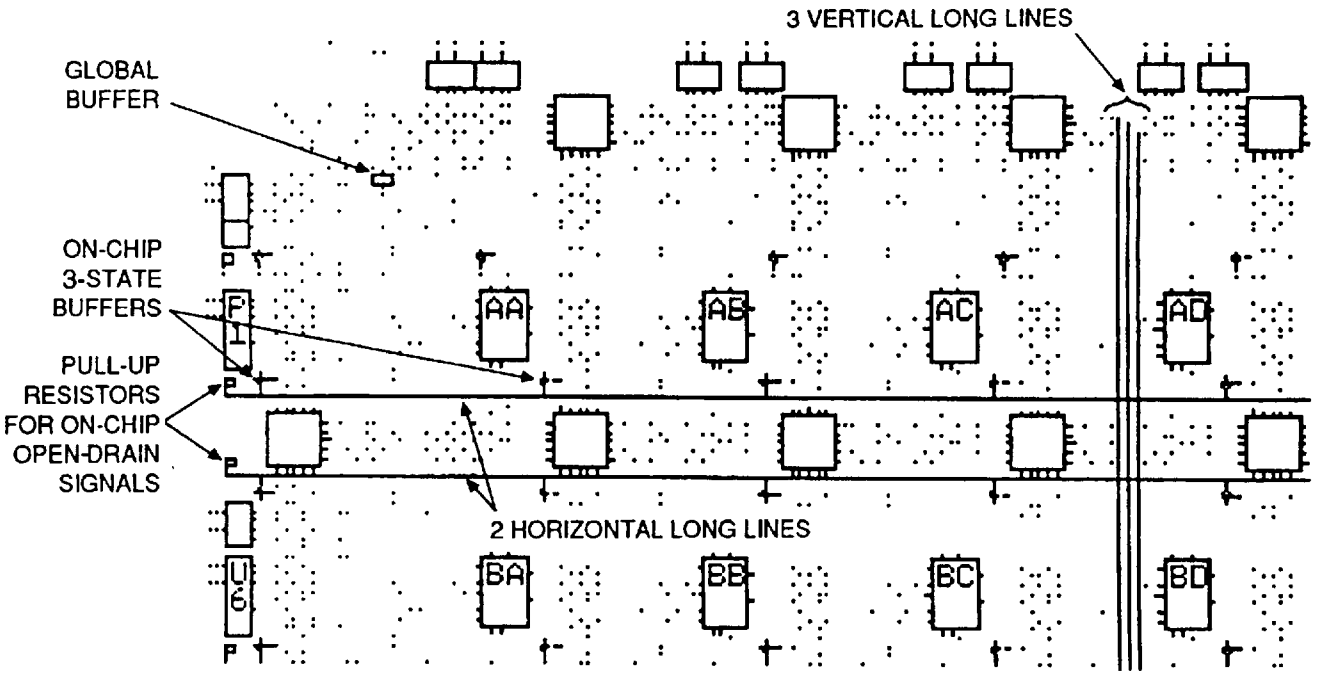



**Figure 13. Horizontal and Vertical Long Lines in the FPGA**

## Programmable Interconnect (continued)

### Internal Buses

A pair of 3-state buffers is located adjacent to each CLB. These buffers allow logic to drive the horizontal long lines. Logical operation of the 3-state buffer controls allows them to implement wide multiplexing functions. Any 3-state buffer input can be selected as drive for the horizontal long line bus by applying a low logic level on its 3-state control line (see Figure 15A on page 14). The user is required to avoid contention that can result from multiple drivers with opposing logic levels. Control of the 3-state input by the same signal that drives the buffer input creates an open-drain wired-AND function. A logical high on both buffer inputs creates a high impedance which represents no contention. A logical low enables the buffer to drive the long line low (see Figure 15B on page 14). Pull-up resistors are available at each end of the long line to provide a high output when all connected buffers are nonconducting. This forms fast, wide gating functions. When data drives the inputs and separate signals drive the 3-state control lines, these buffers form multiplexers (3-state buses). In this case, care must be used to prevent contention through multiple active buffers of conflicting levels on a common line. Figure 16 on page 14 shows 3-state buffers, long lines, and pull-up resistors.

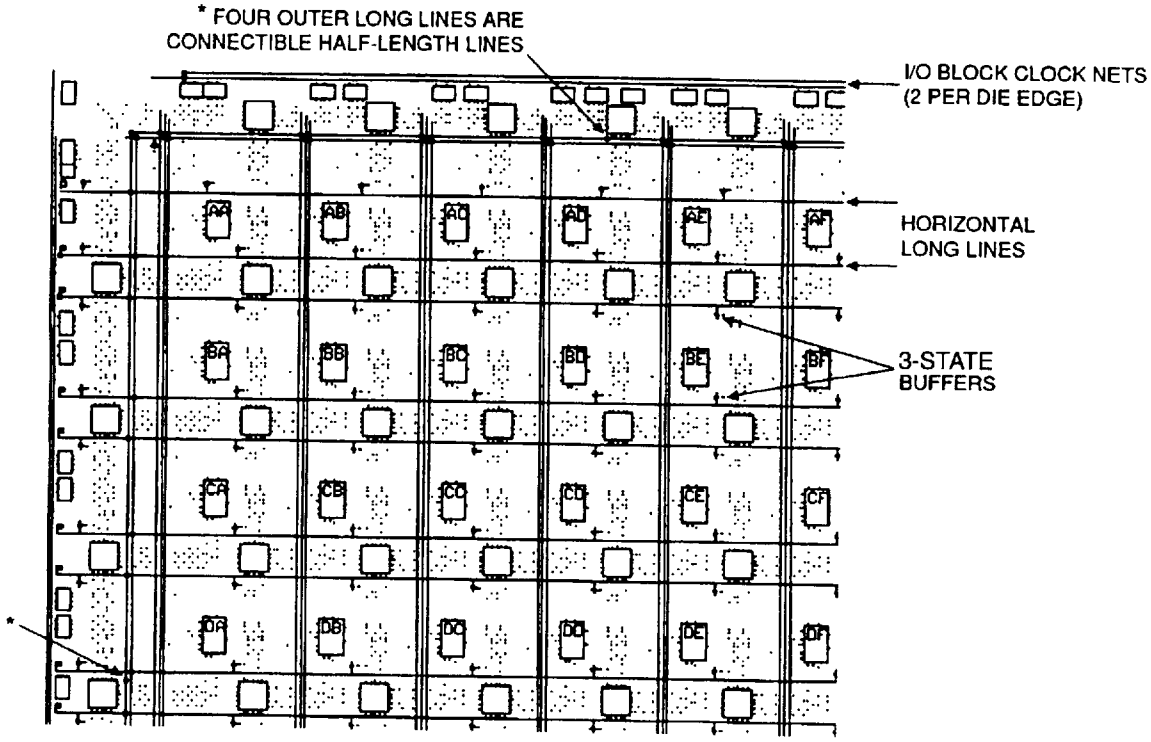



**Figure 14. Programmable Interconnection of Long Lines**

## Programmable Interconnect (continued)

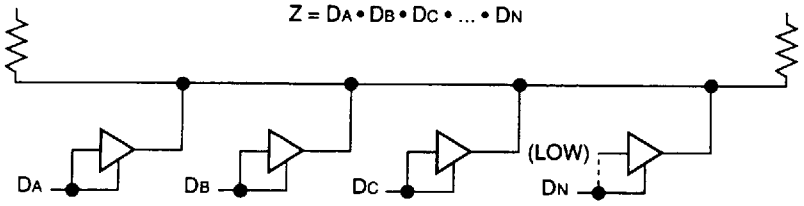



**Figure 15A. 3-State Buffers Implement a Wired-AND Function**

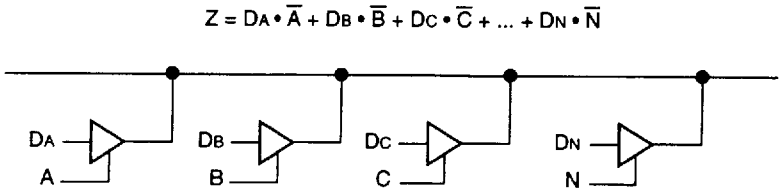



**Figure 15B. 3-State Buffers Implement a Multiplexer**

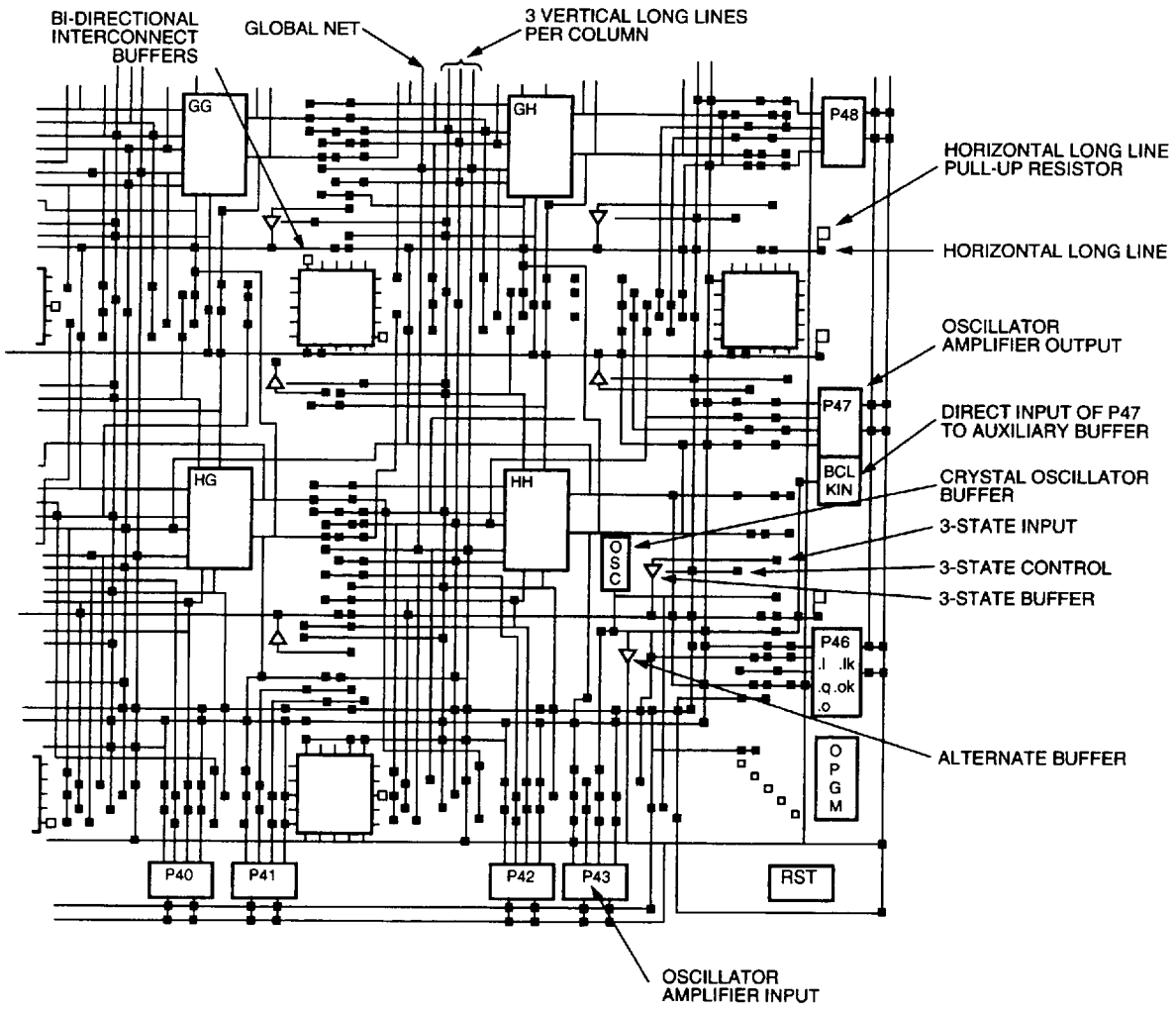
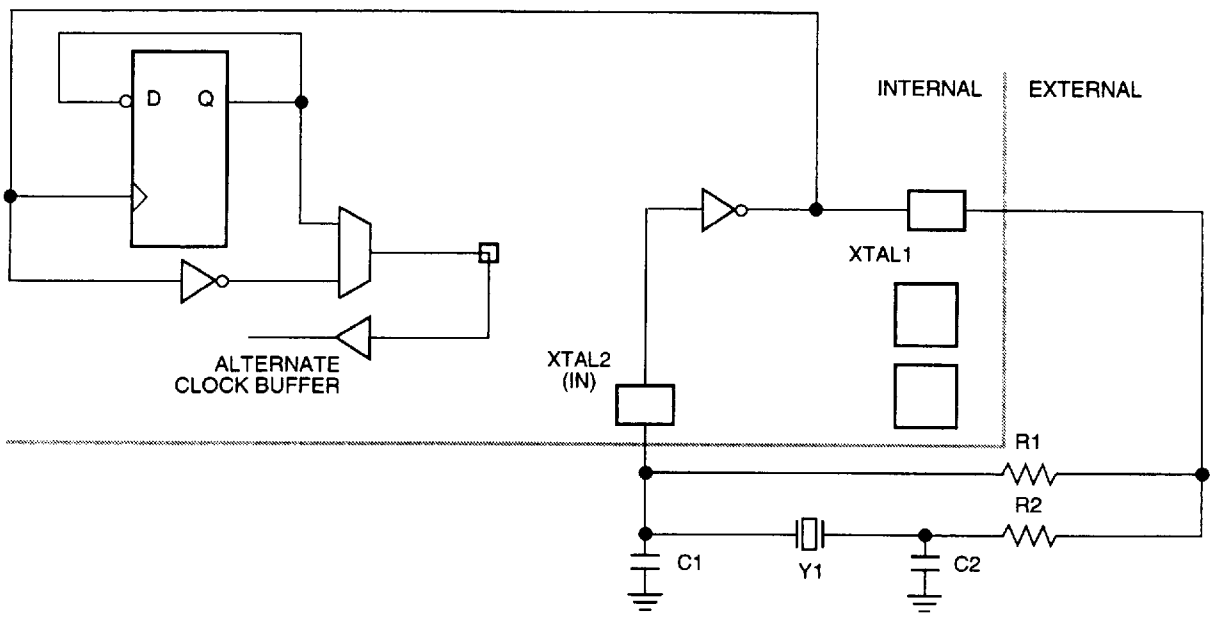



**Figure 16. *XACT* Development System Large View of Possible Interconnections (Lower Right Corner of ATT3020)**

## Programmable Interconnect (continued)

### Crystal Oscillator

Figure 16 on page 14 shows the location of an internal high-speed inverting amplifier which may be used to implement an on-chip crystal oscillator. It is associated with the auxiliary buffer in the lower right corner of the die. When the oscillator is configured by MAKEBITS and connected as a signal source, two special user IOBs are also configured to connect the oscillator amplifier with external crystal oscillator components as shown in Figure 17. A divide-by-two option is available to ensure symmetry. The oscillator circuit becomes active before configuration is complete in order to allow the oscillator to stabilize. Actual internal connection is delayed until completion of configuration. In Figure 17, the feedback resistor, R1, between output and input biases the amplifier at threshold. The value should be as large as practical to minimize loading of the crystal. The inversion of the amplifier, together with the R-C networks and an AT cut series resonant crystal, produces the 360-degree phase shift of the Pierce oscillator. A series resistor, R2, may be included to add to the amplifier output impedance when needed for phase shift control or crystal resistance matching, or to limit the amplifier input swing to control clipping at large amplitudes. Excess feedback voltage may be corrected by the ratio of C2/C1. The amplifier is designed to be used from 1 MHz to one-half the specified CLB toggle frequency. Use at frequencies below 1 MHz may require individual characterization with respect to a series resistance. Crystal oscillators above 20 MHz generally require a crystal which operates in a third overtone mode, where the fundamental frequency must be suppressed by the R-C networks. When the oscillator inverter is not used, these IOBs and their package pins are available for general user I/O.




Suggested component values:
R1—1 μΩ to 4 μΩ
R2—0 kΩ to 1 kΩ (may be required for low frequency, phase shift, and/or compensation level for Crystal Q)
C1, C2—10 pF to 40 pF
Y1—1 MHz to 20 MHz AT cut series resonant

| Pin | 44-Pin PLCC | 68-Pin PLCC | 84-Pin | | 100-Pin | | | 132-Pin PGA | 160-Pin PQFP | 164-Pin CQFP | 175-Pin PGA | 208-Pin SQFP |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | PLCC | PGA | CQFP | PQFP | TQFP | | | | | |
| XTAL1 (OUT) | 30 | 47 | 57 | J11 | 67 | 82 | 79 | P13 | 82 | 105 | T14 | 110 |
| XTAL2 (IN) | 26 | 43 | 53 | L11 | 61 | 76 | 73 | M13 | 76 | 99 | P15 | 100 |

**Figure 17. Crystal Oscillator Inverter**

# Programming

## Initialization Phase

An internal power-on-reset circuit is triggered when power is applied. When Vcc reaches the voltage where portions of the FPGA begin to operate (2.5 V to 3 V), the programmable I/O output buffers are disabled and a high-impedance pull-up resistor is provided for the user I/O pins. A time-out delay is initiated to allow the power supply voltage to stabilize. During this time, the powerdown mode is inhibited. The initialization state time-out (about 11 ms to 33 ms) is determined by a 14-bit counter driven by a self-generated, internal timer. This nominal 1 MHz timer is subject to variations with process, temperature, and power supply over the range of 0.5 MHz to 1.5 MHz. As shown in Table 2, five configuration mode choices are available, as determined by the input levels of three mode pins: M0, M1, and M2.

**Table 2. Configuration Modes**

| M0 | M1 | M2 | Clock | Mode | Data |
|---|---|---|---|---|---|
| 0 | 0 | 0 | Active | Master | Bit Serial |
| 0 | 0 | 1 | Active | Master | Byte Wide (Address = 0000 up) |
| 0 | 1 | 0 | — | Reserved | — |
| 0 | 1 | 1 | Active | Master | Byte Wide (Address = FFFF down) |
| 1 | 0 | 0 | — | Reserved | — |
| 1 | 0 | 1 | Passive | Peripheral | Byte Wide |
| 1 | 1 | 0 | — | Reserved | — |
| 1 | 1 | 1 | Passive | Slave | Bit Serial |

In master-configuration modes, the FPGA becomes the source of configuration clock (CCLK). Beginning configuration of devices using peripheral or slave modes must be delayed long enough for their initialization to be completed. An FPGA with mode lines selecting a master configuration mode extends its initialization state using four times the delay (43 ms to 130 ms) to ensure that all daisy-chained slave devices it may be driving will be ready, even if the master is very fast and the slave(s) very slow (see Figure 18). At the end of initialization, the FPGA enters the clear state where it clears configuration memory. The active-low, open-drain initialization signal $\overline{\text{INIT}}$ indicates when the initialization and clear states are complete. The FPGA tests for the absence of an external active-low $\overline{\text{RESET}}$ before it makes a final sample of the mode lines and enters the configuration state. An external wired-AND of one or more $\overline{\text{INIT}}$ pins can be used to control configuration by the assertion of the active-low $\overline{\text{RESET}}$ of a master mode device or to signal a processor that the FPGAs are not yet initialized.

If a configuration has begun, a reassertion of $\overline{\text{RESET}}$ for a minimum of three internal timer cycles will be recognized and the FPGA will initiate an abort, returning to the clear state to clear the partially loaded configuration memory words. The FPGA will then resample $\overline{\text{RESET}}$ and the mode lines before re-entering the configuration state. A reprogram is initiated when a configured FPGA senses a high-to-low transition on the DONE/$\overline{\text{PROG}}$ package pin. The FPGA returns to the clear state where the configuration memory is cleared and mode lines re-sampled, as for an aborted configuration. The complete configuration program is cleared and loaded during each configuration program cycle.

## Programming (continued)

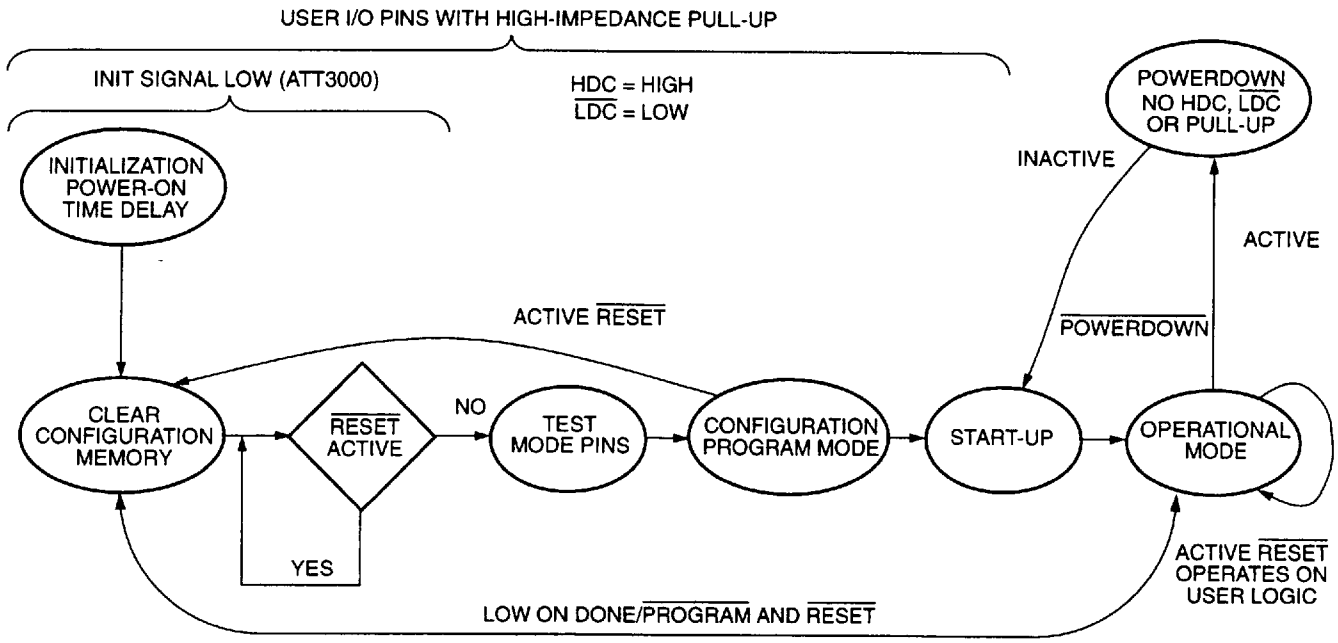



**Figure 18. State Diagram of Configuration Process for Powerup and Reprogram**

Length count control allows a system of multiple FPGAs in assorted sizes to begin operation in a synchronized fashion. The configuration program generated by the MakePROM program of the *XACT* development system begins with a preamble of 111111110010 (binary) followed by a 24-bit length count representing the total number of configuration clocks needed to complete loading of the configuration program(s). The data framing is shown in Figure 19. All FPGAs connected in series read and shift preamble and length count in (on positive) and out (on negative) CCLK edges. An FPGA which has received the preamble and length count then presents a HIGH data out until it has intercepted the appropriate number of data frames. When the configuration program memory of an FPGA is full and the length count does not compare, the FPGA shifts any additional data through, as it did for preamble and length count.

When the FPGA configuration memory is full and the length count compares, the FPGA will execute a synchronous start-up sequence and become operational (see Figure 20 on page 19). Three CCLK cycles after the completion of loading configuration data, the user I/O pins are enabled as configured. As selected in MAKEBITS, the internal user-logic reset is released either one clock cycle before or after the I/O pins become active. A similar timing selection is programmable for the DONE/$\overline{\text{PROG}}$ output signal. DONE/$\overline{\text{PROG}}$ may also be programmed to be an open drain or include a pull-up resistor to accommodate wired-ANDing. The high during configuration (HDC) and low during configuration ($\overline{\text{LDC}}$) are two user I/O pins which are driven active when an FPGA is in initialization, clear, or configure states. These signals and DONE/$\overline{\text{PROG}}$ provide for control of external logic signals such as reset, bus enable, or PROM enable during configuration.

For parallel master configuration modes, these signals provide PROM enable control and allow the data pins to be shared with user logic signals.

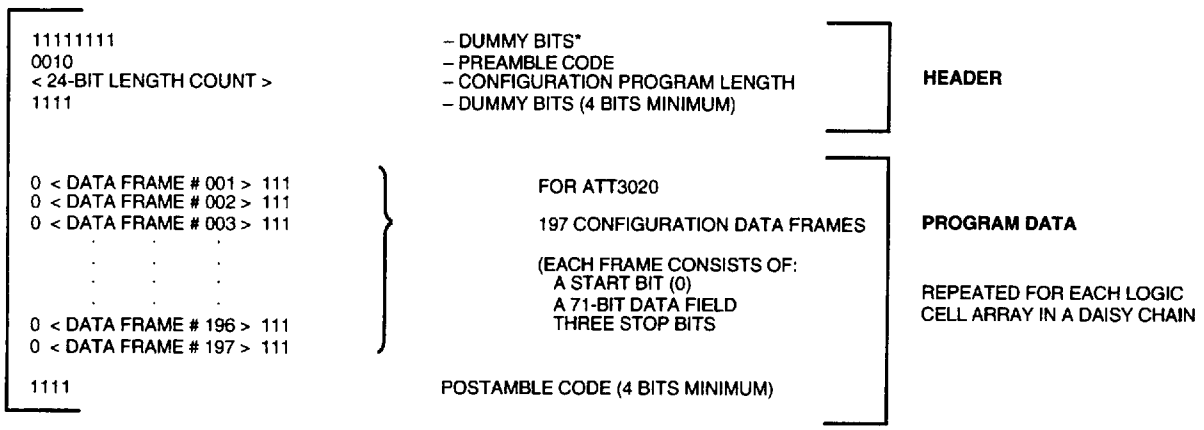
User I/O inputs can be programmed to be either TTL or CMOS compatible thresholds. At powerup, all inputs have TTL thresholds and can change to CMOS thresholds at the completion of configuration, if the user has selected CMOS thresholds. The threshold of $\overline{\text{PWRDWN}}$ and the direct clock inputs are fixed at a CMOS level.

If the crystal oscillator is used, it will begin operation before configuration is complete to allow time for stabilization before it is connected to the internal circuitry.

## Programming (continued)

### Configuration Data

Configuration data to define the function and interconnection within an FPGA are loaded from an external storage at powerup and on a reprogram signal. Several methods of automatic and controlled loading of the required data are available. Logic levels applied to mode selection pins at the start of configuration time determine the method to be used (see Table 2). The data may be either bit-serial or byte-parallel, depending on the configuration mode. Various AT&T programmable gate arrays have different sizes and numbers of data frames. For the ATT3020, configuration requires 14779 bits for each device, arranged in 197 data frames. An additional 40 bits are used in the header (see Figure 20 on page 19).




* The FPGA devices require four dummy bits minimum, *XACT* 3.0 generates eight dummy bits.

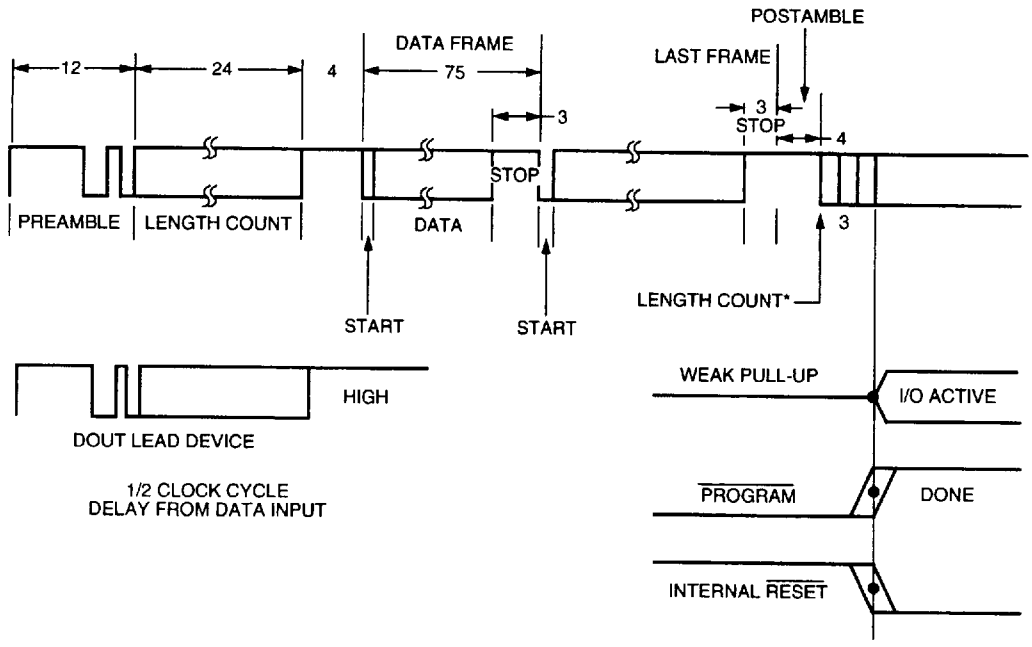
**Figure 19. Internal Configuration Data Structure**

## Programming (continued)

**Table 3. ATT3000 Device Configuration Data**

| Device | ATT3020 | ATT3030 | ATT3042 | ATT3064 | ATT3090 |
|---|---|---|---|---|---|
| Gates | 2000 | 3000 | 4200 | 6400 | 9000 |
| CLBs (Row x Column) | 64 (8 x 8) | 100 (10 x 10) | 144 (12 x 12) | 224 (16 x 14) | 320 (20 x 16) |
| IOBs | 64 | 80 | 96 | 120 | 144 |
| Flip-flops | 256 | 360 | 480 | 688 | 928 |
| Bits-per-frame (with 1 start/3 stop) | 75 | 92 | 108 | 140 | 172 |
| Frames | 197 | 241 | 285 | 329 | 373 |
| Program Data = Bits · Frames + 4 (excludes header) | 14779 | 22176 | 30784 | 46064 | 64160 |
| PROM Size (bits) = Program Data + 40-bit Headers | 14819 | 22216 | 30824 | 46104 | 64200 |

Note: The length count produced by the MAKEBITS program = [(40-bit preamble + sum of program data + 1 per daisy-chain device) rounded up to a multiple of 8] – (2 ≤ K ≤ 4), where K is a function of DONE and RESET timing selected. An additional 8 is added if the roundup increment is less than K. K additional clocks are needed to complete start-up after length count is reached.




* The configuration data consists of a composite 40-bit preamble/length count, followed by one or more concatenated LCA programs, separated by 4-bit postambles. An additional final postamble bit is added for each slave device, and the result rounded up to byte boundary. The length count is two less than the number of resulting bits. Timing of the assertion of DONE and termination of the internal RESET may each be programmed to occur one cycle before or after the I/O outputs become active.

**Figure 20. FPGA Configuration and Start-up**

## Programming (continued)

The specific data format for each device is produced by the MAKEBITS command of the development system, and one or more of these files can then be combined and appended to a length count preamble and be transformed into a PROM format file by the MAKE PROM command of the *XACT* development system. The tie option of the MAKEBITS program defines output levels of unused blocks of a design and connects these to unused routing resources. This prevents indeterminate levels which might produce parasitic supply currents. If unused blocks are not sufficient to complete the tie, the FLAGNET command of EDITFPGA can be used to indicate nets which must not be used to drive the remaining unused routing, since that might affect timing of user nets. NORESTORE will retain the results of TIE for timing analysis with QUERYNET before RESTORE returns the design to the untied condition. TIE can be omitted for quick breadboard iterations where a few additional mA of Icc are acceptable.

The configuration bit-stream begins with high preamble bits, a 4-bit preamble code, and a 24-bit length count. When configuration is initiated, a counter in the FPGA is set to 0 and begins to count the total number of configuration clock cycles applied to the device. As each configuration data frame is supplied to the FPGA, it is internally assembled into a data word. As each data word is completely assembled, it is loaded in parallel into one word of the internal configuration memory array. The configuration loading process is complete when the current length count equals the loaded length count and the required configuration program data frames have been written. Internal user flip-flops are held reset during configuration.

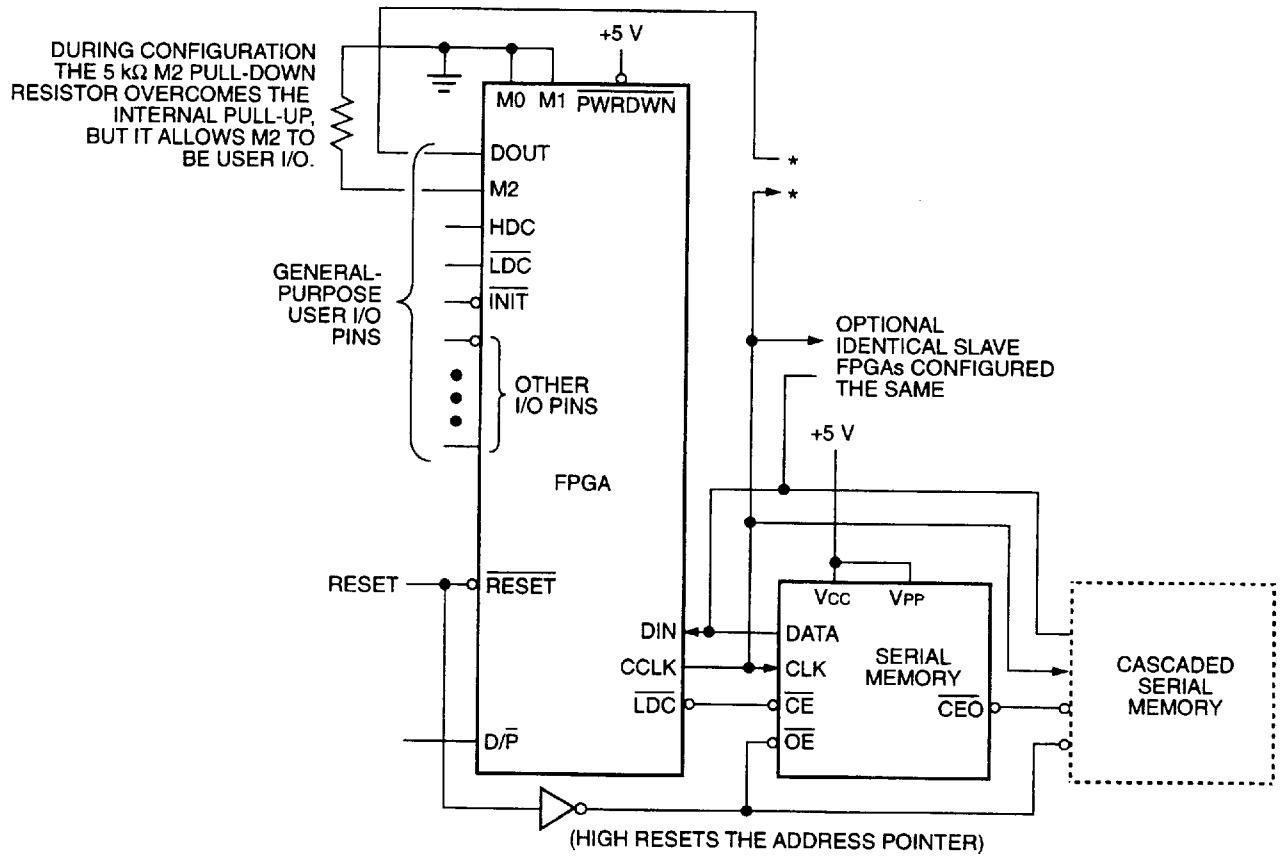
Two user-programmable pins are defined in the unconfigured FPGA: high during configuration (HDC) and low during configuration ($\overline{\text{LDC}}$), and DONE/$\overline{\text{PROG}}$ may be used as external control signals during configuration. In master mode configurations, it is convenient to use $\overline{\text{LDC}}$ as an active-low EPROM chip enable. After the last configuration data bit is loaded and the length count compares, the user I/O pins become active. Options in the MAKEBITS program allow timing choices of one clock earlier or later for the timing of the end of the internal logic reset and the assertion of the DONE signal. The open-drain DONE/$\overline{\text{PROG}}$ output can be AND-tied with multiple FPGAs and used as an active-high READY, an active-low PROM enable, or a RESET to other portions of the system. The state diagram of Figure 18 on page 17 illustrates the configuration process.

## Programming (continued)

### Master Mode

In master mode, the FPGA automatically loads configuration data from an external memory device. There are three master modes which use the internal timing source to supply the configuration clock (CCLK) to time the incoming data. Serial master mode uses serial configuration data supplied to data-in (DIN) from a synchronous serial source such as the serial configuration PROM shown in Figure 19 on page 18. Parallel master low and master high modes automatically use parallel data supplied to the D[7:0] pins in response to the 16-bit address generated by the FPGA. Figure 22 on page 22 shows an example of the parallel master mode connections required. The FPGA HEX starting address is 0000 and increments for master low mode, and it is FFFF and decrements for master high mode. These two modes provide address compatibility with microprocessors which begin execution from opposite ends of memory.

For master high or low, data bytes are read in parallel by each read clock ($\overline{RCLK}$) and internally serialized by the configuration clock. As each data byte is read, the least significant bit of the next byte, D0, becomes the next bit in the internal serial configuration word. One master mode FPGA can be used to interface the configuration program-store, and pass additional concatenated configuration data to additional FPGAs in a serial daisy-chain fashion. CCLK is provided for the slaved devices, and their serialized data is supplied from DOUT to DIN, DOUT to DIN, etc.




Note: The serial configuration PROM supports automatic loading of configuration programs up to 36/64/128 Kbits. Multiple devices can be cascaded to support additional FPGAs. An early DONE inhibits the data output one CCLK cycle before the FPGA I/O becomes active.

**Figure 21. Master Serial Mode**

## Programming (continued)

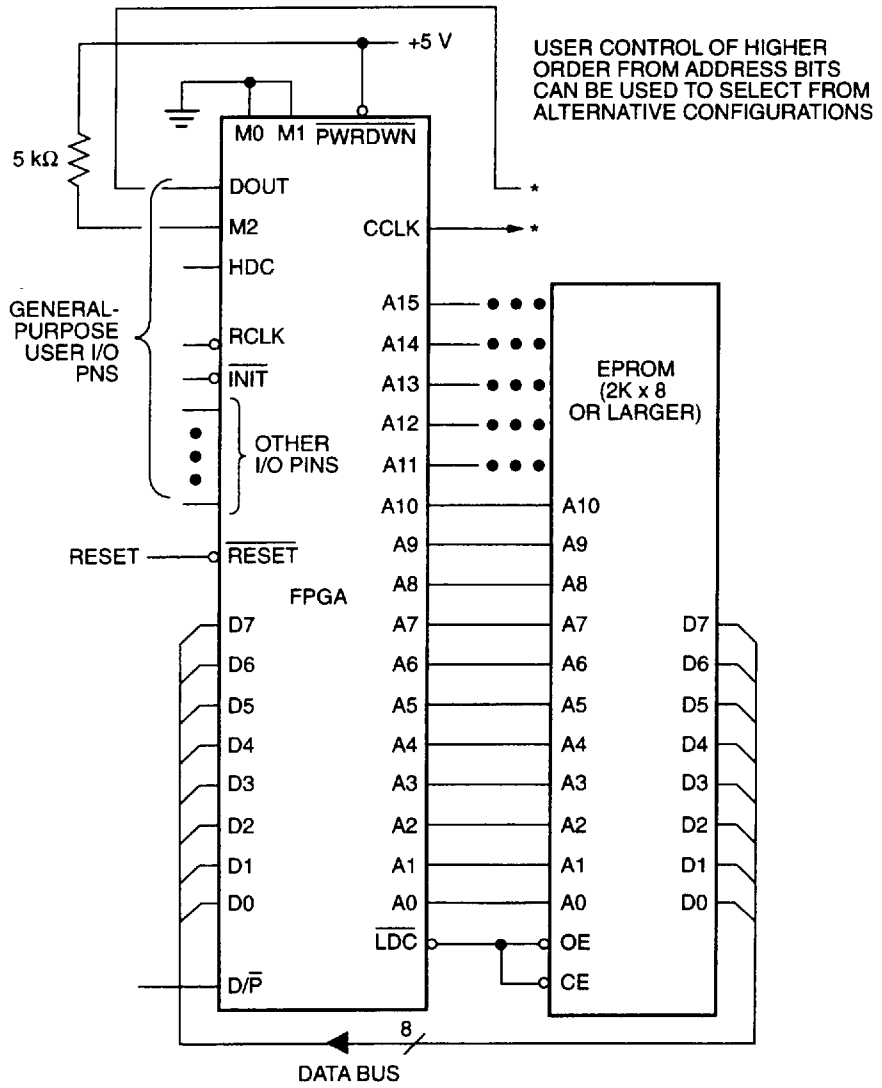



**Figure 22. Master Parallel Mode**

## Programming (continued)

### Peripheral Mode

Peripheral mode provides a simplified interface through which the device may be loaded byte-wide, as a processor peripheral. Figure 23 shows the peripheral mode connections. Processor write cycles are decoded from the common assertion of the active-low write strobe ($\overline{WS}$), and two active-low and one active-high chip selects ($\overline{CS0}$, $\overline{CS1}$, CS2). If all these signals are not available, the unused inputs should be driven to their respective active levels. The FPGA will accept 1 byte of configuration data on the D[7:0] inputs for each selected processor write cycle. Each byte of data is loaded into a buffer register. The FPGA generates a CCLK from the internal timing generator and serializes the parallel input data for internal framing or for succeeding slaves on data out (DOUT). An output HIGH on READY/$\overline{BUSY}$ pin indicates the completion of loading for each byte when the input register is ready for a new byte. As with master modes, peripheral mode may also be used as a lead device for a daisy-chain of slave devices.

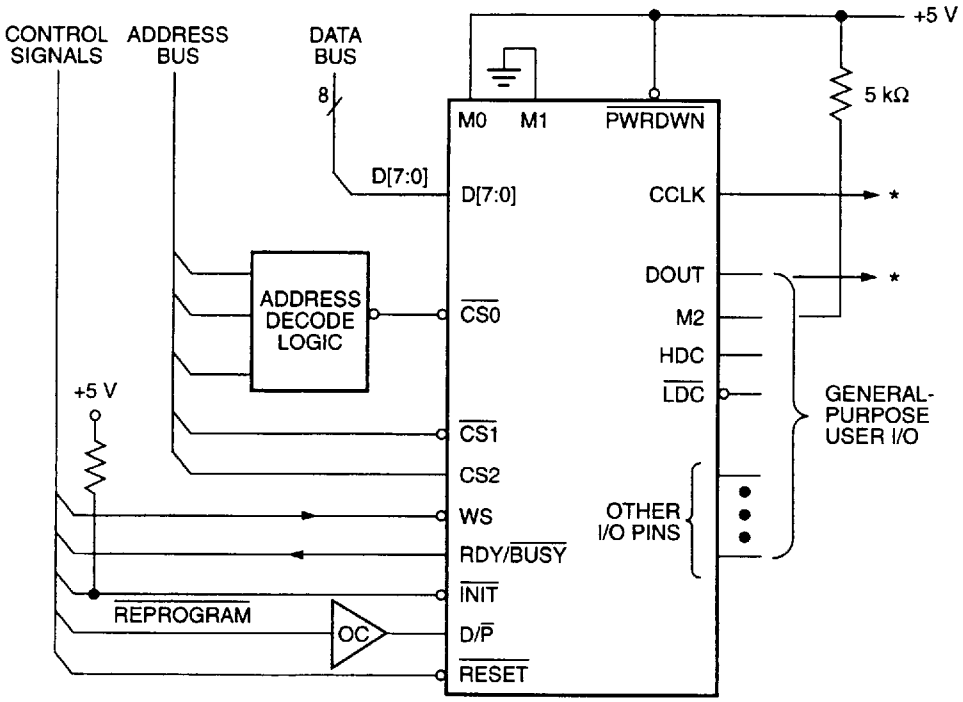



**Figure 23. Peripheral Mode**

## Programming (continued)

### Slave Mode

Slave mode provides a simple interface for loading the FPGA configuration as shown in Figure 24. Serial data are supplied in conjunction with a synchronizing input clock. Most slave mode applications are in daisy-chain configurations in which the data input are supplied by the previous FPGA's data out, while the clock is supplied by a lead device in master or peripheral mode. Data may also be supplied by a processor or other special circuits.

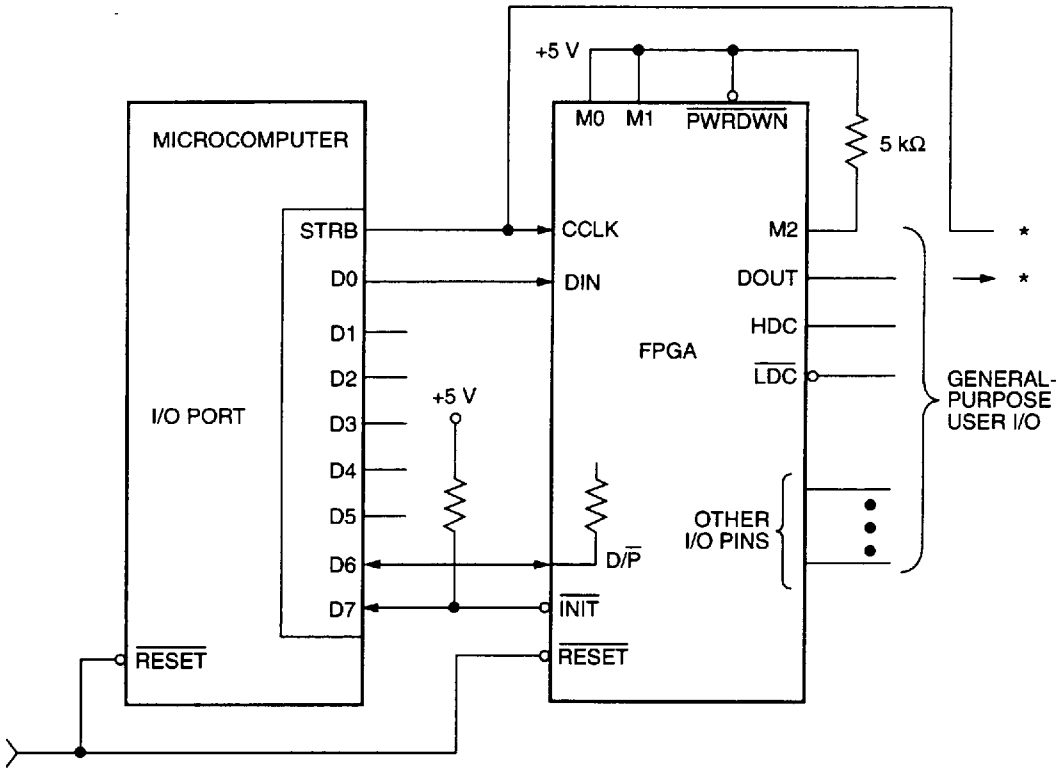



**Figure 24. Slave Mode**

## Programming (continued)

### Daisy-Chain

The *XACT* and *NeoCAD* development systems are used to create a composite configuration bit stream for selected FPGAs including: a preamble, a length count for the total bit stream, multiple concatenated data program, a postamble, plus an additional fill bit per device in the serial chain. After loading and passing-on the preamble and length count to a possible daisy-chain, a lead device will load its configuration data frames while providing a HIGH DOUT to possible downstream devices as shown in Figure 25. Loading continues while the lead device has received its configuration program and the current length count has not reached the full value. Additional data are passed through the lead device and appear on the data out (DOUT) pin in serial form. The lead device also generates the CCLK to synchronize the serial output data and data in of downstream FPGAs. Data is read in on DIN of slave devices by the positive edge of CCLK and shifted out the DOUT on the negative edge of CCLK. A parallel master mode device uses its internal timing generator to produce an internal CCLK of eight times its EPROM address rate, while a peripheral mode device produces a burst of eight CCLKs for each chip select and write-strobe cycle. The internal timing generator continues to operate for general timing and synchronization of inputs in all modes.

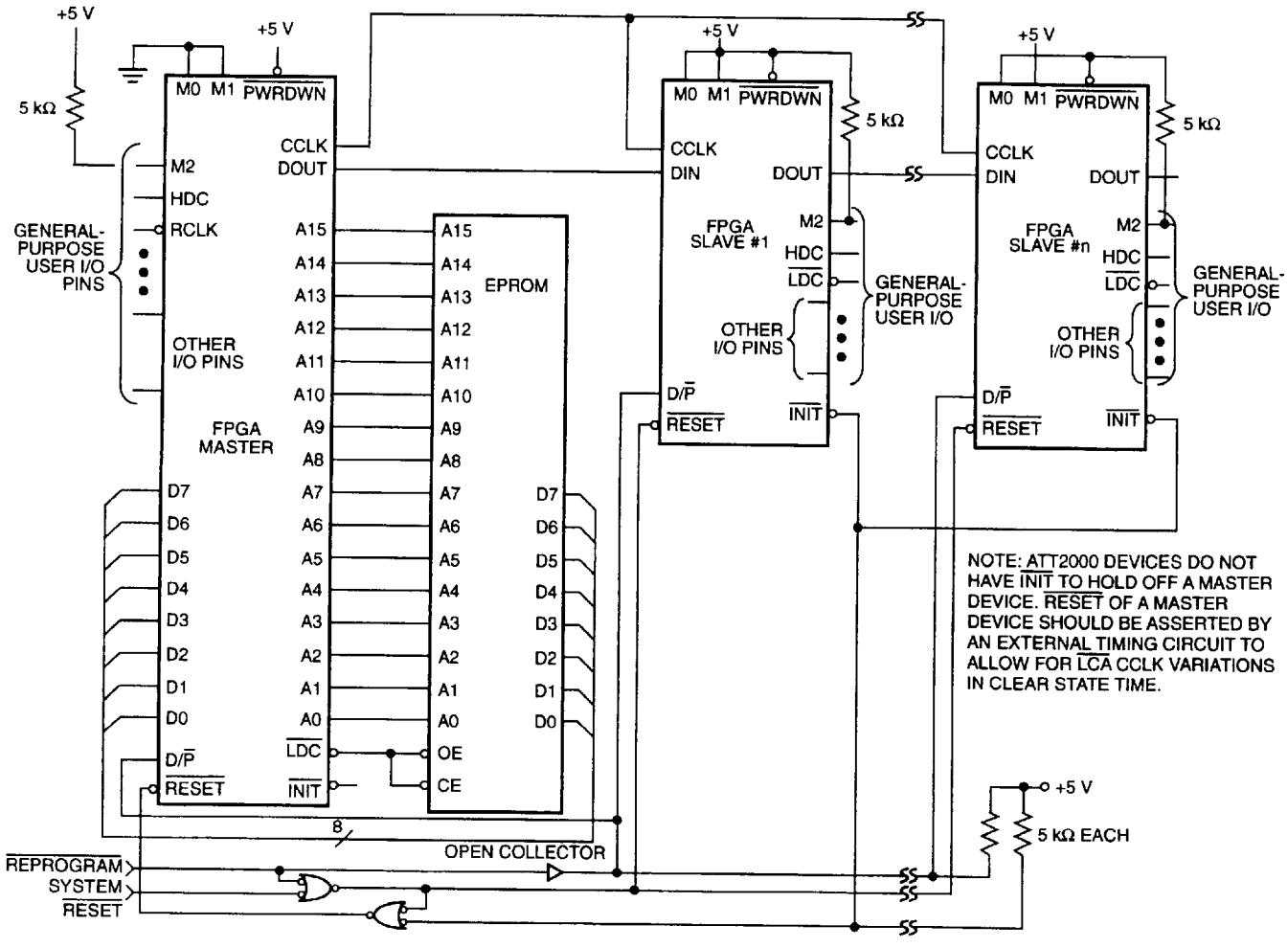



**Figure 25. Master Mode with Daisy-Chained Slave Mode Devices**

## Special Configuration Functions

The configuration data include control over several special functions in addition to the normal user logic functions and interconnect:

- Input thresholds
- Readback enable
- DONE pull-up resistor
- DONE timing
- RESET timing
- Oscillator frequency divided by two

Each of these functions is controlled by configuration data bits which are selected as part of the normal development system bit-stream generation process.

### Input Thresholds

Prior to the completion of configuration, all FPGA input thresholds are TTL compatible. Upon completion of configuration, the input thresholds become either TTL or CMOS compatible as programmed. The use of the TTL threshold option requires some additional supply current for threshold shifting. The exception is the threshold of the PWRDWN input and direct clocks which always have a CMOS input. Prior to the completion of configuration, the user I/O pins each have a high-impedance pull-up. The configuration program can be used to enable the IOB pull-up resistors in the operational mode to act either as an input load or to avoid a floating input on an otherwise unused pin.

### Readback

The contents of an FPGA may be read back if it has been programmed with a bit-stream in which the readback option has been enabled. Readback may be used for verification of configuration and as a method for determining the state of internal logic nodes. There are three options in generating the configuration bit-stream:

- **Never** will inhibit the readback capability.
- **One-time** will inhibit readback after one readback has been executed to verify the configuration.
- **On-command** will allow unrestricted use of readback.

Readback is accomplished without the use of any of the user I/O pins; only M0, M1, and CCLK are used. The initiation of readback is produced by a low-to-high transition of the M0/RTRIG (read trigger) pin. Once the readback command has been given, the input CCLK is driven by external logic to read back each data bit in a format similar to loading. After two dummy bits, the first data frame is shifted out, in inverted sense, on the M1/RDATA (read data) pin. All data frames must be read back to complete the process and return the mode select and CCLK pins to their normal functions.

The readback data includes the current state of each internal logic block storage element, and the state of the (.i and .ri) connection pins on each IOB. The data is imbedded into unused configuration bit positions during readback. This state information is used by the FPGA development system in-circuit verifier to provide visibility into the internal operation of the logic while the system is operating. To read back a uniform time sample of all storage elements, it may be necessary to inhibit the system clock.

### Reprogram

The FPGA configuration memory can be rewritten while the device is operating in the user's system. To initiate a reprogramming cycle, the dual function package pin DONE/PROG must be given a high-to-low transition. To reduce sensitivity to noise, the input signal is filtered for two cycles of the FPGA's internal timing generator. When reprogram begins, the user-programmable I/O output buffers are disabled and high-impedance pull-ups are provided for the package pins. The device returns to the clear state and clears the configuration memory before it prompts **initialized**. Since this clear operation uses chip-individual internal timing, the master might complete the clear operation and then start configuration before the slave has completed the clear operation. To avoid this, wire-AND the slave INIT pins and use them to force a RESET on the master (see Figure 25 on page 25). Reprogram control is often implemented by using an external open-collector driver which pulls DONE/PROG low. Once it recognizes a stable request, the FPGA will hold a low until the new configuration has been completed. Even if the reprogram request is externally held low beyond the configuration period, the FPGA will begin operation upon completion of configuration.

### DONE Pull-Up

DONE/PROG is an open-drain I/O pin that indicates the FPGA is in the operational state. An optional internal pull-up resistor can be enabled by the user of the development system when make bits is executed. The DONE/PROG pins of multiple FPGAs in a daisy-chain may be connected together to indicate that all are DONE or to direct them all to reprogram.

## Special Config. Functions (continued)

### DONE Timing

The timing of the DONE status signal can be controlled by a selection in the MAKEBITS program to occur a CCLK cycle before, or after, the timing of outputs being activated (see Figure 20 on page 19). This facilitates control of external functions, such as a PROM enable or holding a system in a wait-state.

### RESET Timing

As with DONE timing, the timing of the release of the internal $\overline{\text{RESET}}$ can be controlled by a selection in the MAKEBITS program to occur a CCLK cycle before, or after, the timing of outputs being enabled (see Figure 20 on page 19). This reset maintains all user programmable flip-flops and latches in a zero state during configuration.

### Crystal Oscillator Division

A selection in the MAKEBITS program allows the user to incorporate a dedicated divide-by-two flip-flop in the crystal oscillator function. This provides higher assurance of a symmetrical timing signal. Although the frequency stability of crystal oscillators is high, the symmetry of the waveform can be affected by bias or feedback drive.

## Performance

### Device Performance

The high performance of the FPGA is due in part to the manufacturing process, which is similar to that used for high-speed CMOS static memories. Performance can be measured in terms of minimum propagation times for logic elements. The parameter which traditionally describes the overall performance of a gate array is the toggle frequency of a flip-flop. The configuration for determining the toggle performance of the FPGA is shown in Figure 26. The flip-flop output Q is fed back through the combinatorial logic as Q to form the toggle flip-flop.

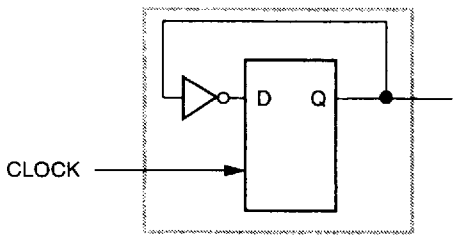



**Figure 26. Toggle Flip-Flop**

FPGA performance is determined by the timing of critical paths, including both the fixed timing for the logic and storage elements in that path, and the timing associated with the routing of the network. Examples of internal worst-case timing are included in the performance data to allow the user to make the best use of the capabilities of the device. The *XACT* development system timing calculator or *XACT* generated simulation models should be used to calculate worst-case paths by using actual impedance and loading information. Figure 27 on page 28 shows a variety of elements which are involved in determining system performance. Table 20 gives the parameter values for the different speed grades. Actual measurement of internal timing is not practical, and often only the sum of component timing is relevant as in the case of input to output. The relationship between input and output timing is arbitrary, and only the total determines performance.

Timing components of internal functions may be determined by measurement of differences at the pins of the package. A synchronous logic function which involves a clock to block-output and a block-input to clock set-up is capable of higher-speed operation than a logic configuration of two synchronous blocks with an extra combinatorial block level between them. System clock rates to 60% of the toggle frequency are practical for logic in which an extra combinatorial level is located between synchronized blocks. This allows implementation of functions of up to 25 variables. The use of the wired-AND is also available for wide, high-speed functions.

### Logic Block Performance

Logic block performance is expressed as the propagation time from the interconnect point at the input of the combinatorial logic to the output of the block in the interconnect area. Combinatorial performance is independent of the specific logic function because of the table look-up based implementation. Timing is different when the combinatorial logic is used in conjunction with the storage element. For the combinatorial logic function driving the data input of the storage element, the critical timing is data setup relative to the clock edge provided to the flip-flop element. The delay from the clock source to the output of the logic block is critical in the timing of signals produced by storage elements. Loading of a logic block output is limited only by the resulting propagation delay of the larger interconnect network. Speed performance of the logic block is a function of supply voltage and temperature (see Figures 28 and 29 on page 29).

## Performance (continued)

### Interconnect Performance

Interconnect performance depends on the routing resource used to implement the signal path. As discussed earlier, direct interconnect from block to block provides a fast path for a signal. The single metal segment used for long lines exhibits low resistance from end to end, but relatively high capacitance. Signals driven through a programmable switch will have the additional impedance of the switch added to their normal drive impedance.

General-purpose interconnect performance depends on the number of switches and segments used, the presence of the bidirectional repowering buffers, and the overall loading on the signal path at all points along the path. In calculating the worst-case timing for a general interconnect path, the timing calculator portion of the *XACT* development system accounts for all of these elements. As an approximation, interconnect timing is proportional to the summation of totals of local metal segments beyond each programmable switch. In effect, the time is a sum of R-C time each approximated by an R times the total C it drives. The R of the switch and the C of the interconnect are functions of the particular device performance grade. For a string of three local interconnects, the approximate time at the first segment after the first switch resistance would be three units—an additional two units after the next switch plus an additional unit after the last switch in the chain. The interconnect R-C chain terminates at each repowering buffer. The capacitance of the actual block inputs is not significant; the capacitance is in the interconnect metal and switches. Figure 30 on page 30 illustrates this.

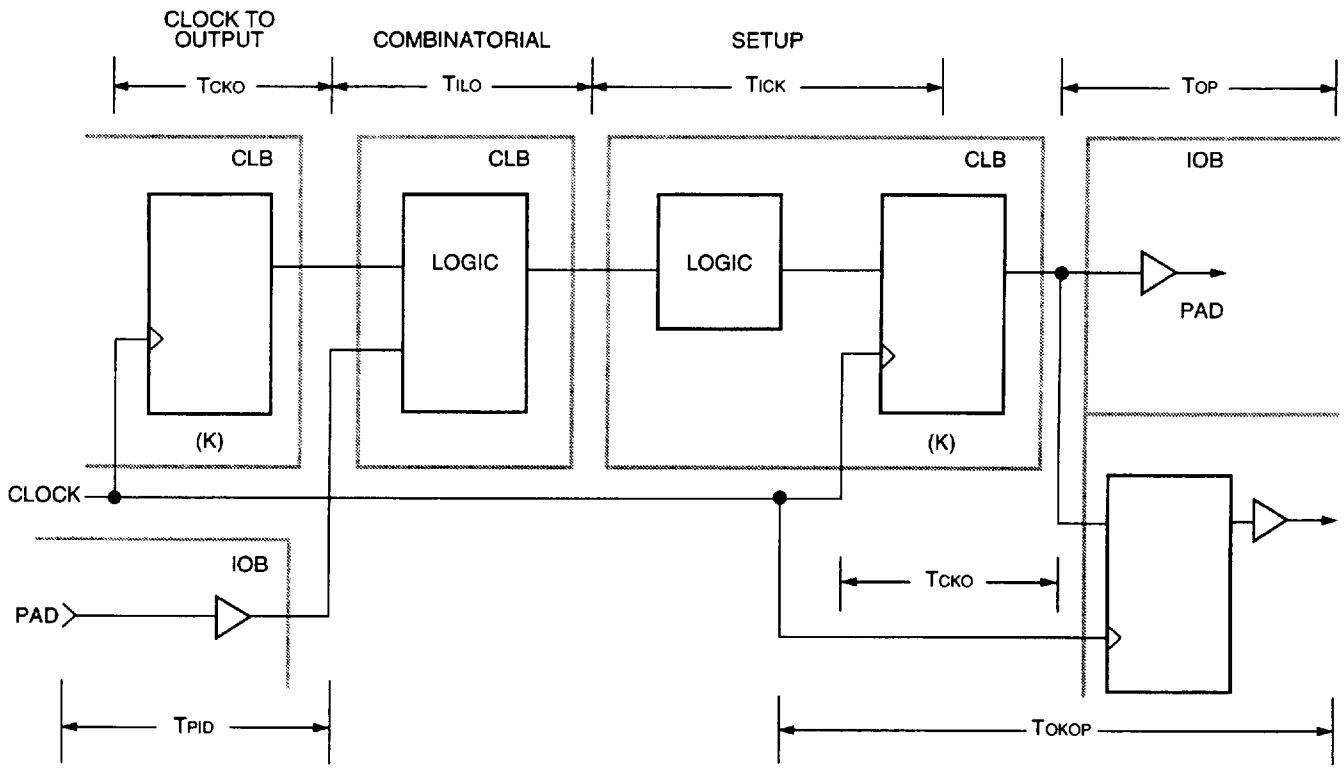



**Figure 27. Examples of Primary Block Speed Factors**

## Performance (continued)

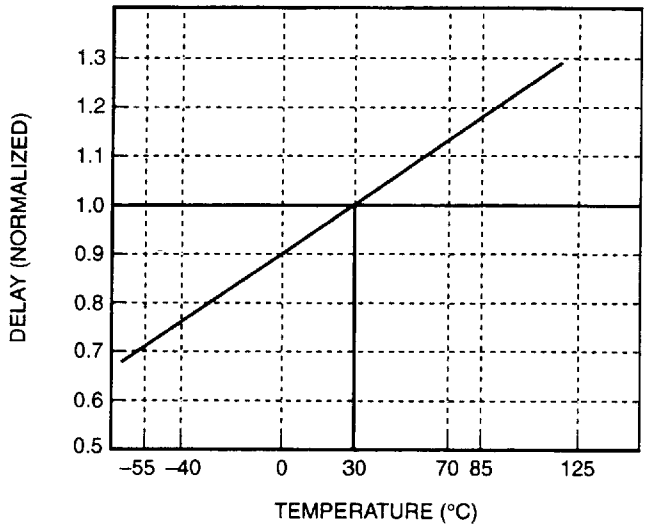



Figure 28. Change in Speed Performance

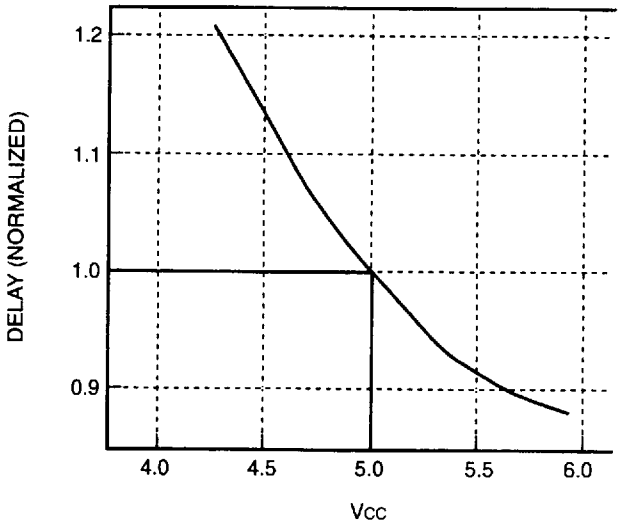



Figure 29. Speed Performance of a CMOS Device

# Power

## Power Distribution

Power for the FPGA is distributed through a grid to achieve high noise immunity and isolation between logic and I/O. Inside the FPGA, a dedicated Vcc and ground ring surrounding the logic array provides power to the I/O drivers (see Figure 31 on page 31). An independent matrix of Vcc and ground lines supplies the interior logic of the device. This power distribution grid provides a stable supply and ground for all internal logic, providing the external package power pins are all connected and appropriately decoupled. Typically a 0.1 µF capacitor connected near the Vcc and ground pins of the package will provide adequate decoupling.

Output buffers which drive the specified 4 mA loads under worst-case conditions may drive 25 to 30 times this amount under best-case process conditions. Noise can be reduced by minimizing external load capacitance and reducing simultaneous output transitions in the same direction. It may also be beneficial to locate heavily loaded output buffers near the ground pads. The IOB output buffers have a slew-limited mode which should be used where output rise and fall times are not speed critical.

Slew-limited outputs maintain their dc drive capability but generate less external reflections and internal noise. More than 32 fast outputs should not be switching in the same direction simultaneously.

## Power (continued)

### Power Dissipation

The FPGA exhibits the low power consumption characteristic of CMOS ICs. For any design, the user can use Figure 32 on page 32 to calculate the total power requirement based on the sum of the capacitive and dc loads both external and internal. The configuration option of TTL chip input threshold requires power for the threshold reference. The power required by the static memory cells which hold the configuration data is very low and may be maintained in a powerdown mode.

Typically, most of power dissipation is produced by external capacitive loads on the output buffers. This load and frequency dependent power is 25 µW/pF/MHz per output. Another component of I/O power is the dc loading on each output pin by devices driven by the FPGA.

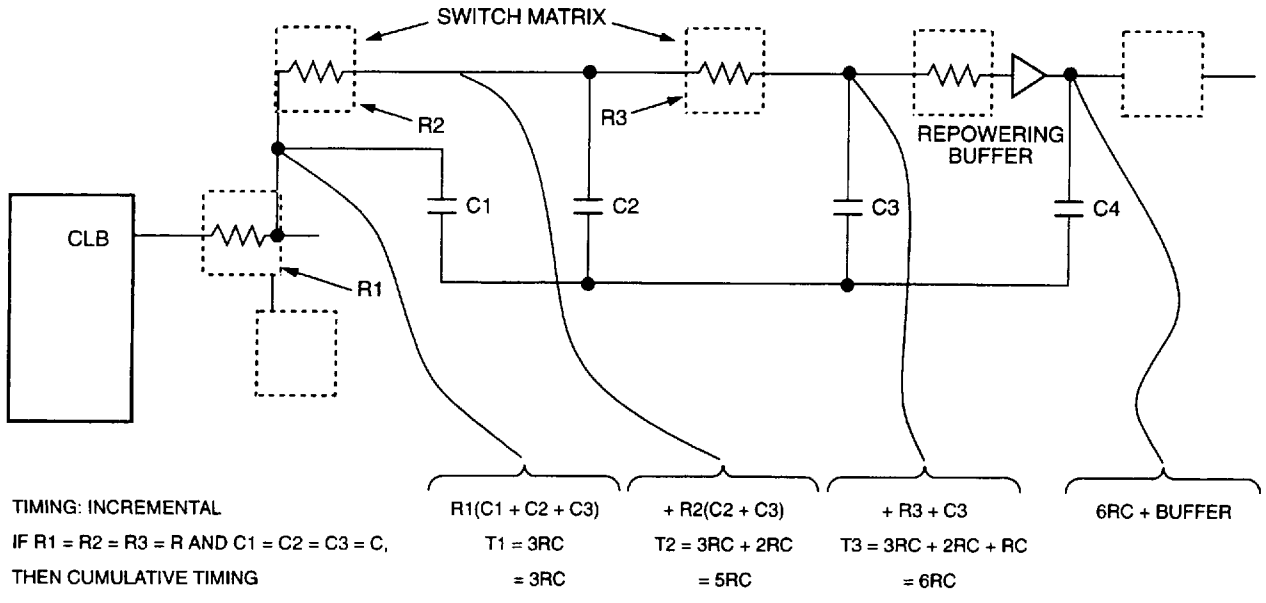



**Figure 30. Interconnection Timing Example**

## Power (continued)

Internal power dissipation is a function of the number and size of the nodes, and the frequency at which they change. In an FPGA, the fraction of nodes changing on a given clock is typically low (10% to 20%). For example, in a large binary counter, the average clock cycle produces changes equal to one CLB output at the clock frequency. Typical global clock buffer power is between 1.7 mW/MHz for the ATT3020 and 3.6 mW/MHz for the ATT3090. The internal capacitive load is more a function of interconnect than fan-out. With a typical load of three general interconnect segments, each configurable logic block output requires about 0.4 mW per MHz of its output frequency:

Total Power = VCC + ICCO + External (dc + Capacitive) + Internal (CLB + IOB + Long Line + Pull-up)

Because the control storage of the FPGA is CMOS static memory, its cells require a very low standby current for data retention. In some systems, this low data retention current characteristic can be used as a method of preserving configurations in the event of a primary power loss. The FPGA has built-in powerdown logic which, when activated, will disable normal operation of the device and retain only the configuration data. All internal operation is suspended and output buffers are placed in their high-impedance state with no pull-ups. Powerdown data retention is possible with a simple battery backup circuit, because the power requirement is extremely low. For retention at 2.4 V, the required current is typically on the order of 50 nA.

To force the FPGA into the powerdown state, the user must pull the $\overline{\text{PWRDWN}}$ pin low and continue to supply a retention voltage to the Vcc pins of the package. When normal power is restored, Vcc is elevated to its normal operating voltage and $\overline{\text{PWRDWN}}$ is returned to a high. The FPGA resumes operation with the same internal sequence that occurs at the conclusion of configuration. Internal I/O and logic block storage elements will be reset, the outputs will become enabled and the DONE/$\overline{\text{PROG}}$ pin will be released. No configuration programming is involved.

When the power supply is removed from a CMOS device, it is possible to supply some power from an input signal. The conventional electrostatic input protection is implemented with diodes to the supply and ground. A positive voltage applied to an I/O will cause the positive protection diode to conduct and drive the power pin. This condition can produce invalid power conditions and should be avoided. A large series resistor might be used to limit the current or a bipolar buffer may be used to isolate the input signal.

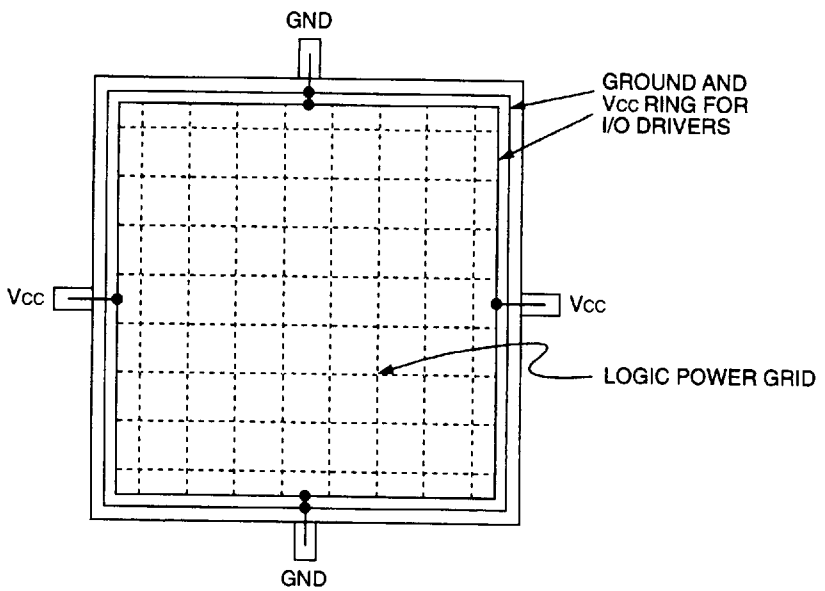
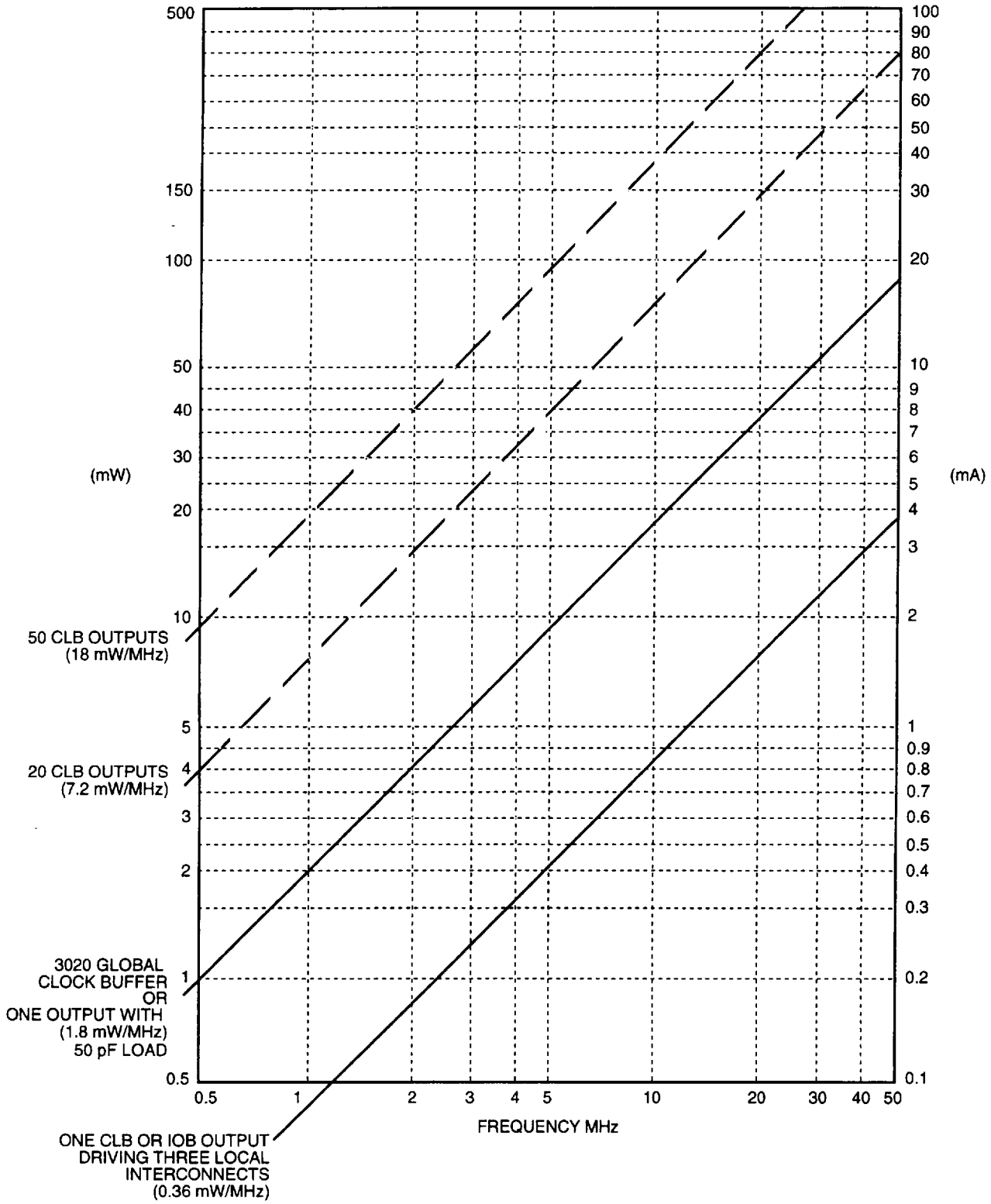



**Figure 31. FPGA Power Distribution**

## Power (continued)




Note: Total chip power is the sum of VCC x ICCO plus effective internal and external values of frequency-dependent capacitive charging currents and duty-factor-dependent resistive loads.

**Figure 32. FPGA Power Consumption by Element**

## Pin Information

**Table 4. Permanently Dedicated Pins**

| Symbol | Name/Description |
|---|---|
| VCC | Two to eight (depending on package type) connections to the nominal +5 V supply voltage. All must be connected. |
| GND | Two to eight (depending on package type) connections to ground. All must be connected. |
| $\overline{\text{PWRDWN}}$ | A low on this CMOS compatible input stops all internal activity to minimize VCC power, and puts all output buffers in a high-impedance state, configuration is retained. When the $\overline{\text{PWRDWN}}$ pin returns high, the device returns to operation with the same sequence of buffer enable and DONE/$\overline{\text{PROGRAM}}$ as at the completion of configuration. All internal storage elements are reset. If not used, $\overline{\text{PWRDWN}}$ must be tied to VCC. |
| $\overline{\text{RESET}}$ | This is an active-low input which has three functions:<br>■ Prior to the start of configuration, a LOW input will delay the start of the configuration process. An internal circuit senses the application of power and begins a minimal time-out cycle. When the time-out and $\overline{\text{RESET}}$ are complete, the levels of the "M" lines are sampled and configuration begins.<br>■ If $\overline{\text{RESET}}$ is asserted during a configuration, the FPGA is reinitialized and will restart the configuration at the termination of $\overline{\text{RESET}}$.<br>■ If $\overline{\text{RESET}}$ is asserted after configuration is complete, it will provide an asynchronous reset of all IOB and CLB storage elements of the FPGA. |
| CCLK | **Configuration Clock.** During configuration, this is an output of an FPGA in master mode or peripheral mode. FPGAs in slave mode use it as a clock input. During a readback operation, it is a clock input for the configuration data being filtered out. |
| DONE/ $\overline{\text{PROG}}$ | **DONE Output.** Configurable as open drain with or without an internal pull-up resistor. At the completion of configuration, the circuitry of the FPGA becomes active in a synchronous order, and DONE may be programmed to occur one cycle before or after that occurs. Once configuration is done, a high-to-low transition of this pin will cause an initialization of the FPGA and start a reconfiguration. |
| M0 | **Mode 0.** This input, M1, and M2 are sampled before the start of configuration to establish the configuration mode to be used. |
| RTRIG | **Read Trigger.** A low-to-high input transition after configuration is complete will initiate a readback of configuration and storage element data by CCLK. This operation may be limited to a single request (or be inhibited altogether) by selecting the appropriate readback option when generating the bit stream. |
| M1 | **Mode 1.** This input, M0, and M2 are sampled before the start of configuration to establish the configuration mode to be used. If readback is to be used, a 5 kΩ resistor should be used to define mode level inputs. |
| $\overline{\text{RDATA}}$ | **Read Data (Active-Low).** This pin is the output of the readback data. |

## Pin Information (continued)

**Table 5. I/O Pins with Special Functions**

| Symbol | Name/Description |
|---|---|
| M2 | **Mode 2.** This input has a passive pull-up during configuration. Together with M0 and M1, it is sampled before the start of configuration to establish the configuration mode to be used. After configuration, this pin becomes a user-programmable I/O pin. |
| HDC | **High During Configuration.** HDC is held at a high level by the FPGA until after configuration. It is available as a control output indicating that configuration is not yet completed. After configuration, this pin is a user I/O pin. |
| $\overline{\text{LDC}}$ | **Low During Configuration (Active-Low).** This signal is held at a low level by the FPGA until after configuration. It is available as a control output indicating that configuration is not yet completed. It is particularly useful in master mode as a low enable for an EPROM. After configuration, this pin is a user I/O pin. If used as a low EPROM enable, it must be programmed as a high after configuration. |
| $\overline{\text{INIT}}$ | This is an active-low open drain output which is held low during the power stabilization and internal clearing of the configuration memory. It can be used to indicate status to a configuring microprocessor or, as a wired-AND of several slave mode devices, a hold-off signal for a master mode device. After configuration, this pin becomes a user-programmable I/O pin. |
| BCLKIN | This is a direct CMOS level input to the alternate clock buffer (auxiliary buffer) in the lower right corner. |
| XTL1 | This user I/O pin can be used to operate as the output of an amplifier driving an external crystal and bias circuitry. |
| XTL2 | This user I/O pin can be used as the input of an amplifier connected to an external crystal and bias circuitry. The I/O block is left unconfigured. The oscillator configuration is activated by routing a net from the oscillator buffer symbol output and by the MAKEBITS program. |
| $\overline{\text{CS0}}$, $\overline{\text{CS1}}$, CS2, $\overline{\text{WS}}$ | These four inputs represent a set of signals, three active-low and one active-high, which are used in the peripheral mode to control configuration data entry. The assertion of all four generates a write to the internal data buffer. The removal of any assertion clocks in the D[7:0] data present. In the master parallel mode, $\overline{\text{WS}}$ and CS2 are the A0 and A1 outputs. After configuration, the pins are user-programmable I/O pins. |
| $\overline{\text{RCLK}}$ | During master parallel mode configuration, $\overline{\text{RCLK}}$ represents a read of an external dynamic memory device (normally not used). |
| RDY/$\overline{\text{BUSY}}$ | During peripheral parallel mode configuration, this pin indicates when the chip is ready for another byte of data to be written to it. After configuration is complete, this pin becomes a user-programmed I/O pin. |
| D[7:0] | This set of eight pins represents the parallel configuration byte for the parallel master and peripheral modes. After configuration is complete, they are user-programmed I/O pins. |
| A[15:0] | This set of 16 pins presents an address output for a configuration EPROM during master parallel mode. After configuration is complete, they are user-programmed I/O pins. |
| DIN | This user I/O pin is used as serial data input during slave or master serial configuration. This pin is data 0 input in master or peripheral configuration mode. |
| DOUT | This user I/O pin is used during configuration to output serial configuration data for daisy-chained slaves' data in. |
| TCLKIN | This is a direct CMOS level input to the global clock buffer. |
| I/O | **Input/Output (Unrestricted).** May be programmed by the user to be input and/or output pin following configuration. Some of these pins present a high-impedance pull-up (see next page) or perform other functions before configuration is complete (see above). |

## Pin Information (continued)

### Table 6A. ATT3000 Family Configuration (44-, 68-, and 84-PLCC; 84-PGA; 100-PQFP; and 100-CQFP)

| Configuration Mode (M2:M1:M0) | | | | | 44 PLCC* | 68 PLCC | 84 PLCC† | 84 PGA | 100 PQFP | 100 CQFP | User Operation |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Slave (1:1:1) | Master-Serial (0:0:0) | Peripheral (1:0:1) | Master-High (1:1:0) | Master-Low (1:0:0) | | | | | | | |
| PWRDWN | PWRDWN | PWRDWN | PWRDWN | PWRDWN | 7 | 10 | 12 | B2 | 29 | 14 | PWRDWN |
| VCC | VCC | VCC | VCC | VCC | 12 | 18 | 22 | F3 | 41 | 26 | VCC |
| M1 (High) | M1 (Low) | M1 (Low) | M1 (High) | M1 (Low) | 16 | 25 | 31 | J2 | 52 | 37 | RDATA |
| M0 (High) | M0 (Low) | M0 (Low) | M0 (High) | M0 (Low) | 17 | 26 | 32 | L1 | 54 | 39 | RTRIG |
| M2 (High) | M2 (Low) | M2 (High) | M2 (High) | M2 (Low) | 18 | 27 | 33 | K2 | 56 | 41 | I/O |
| HDC (High) | HDC (High) | HDC (High) | HDC (High) | HDC (High) | 19 | 28 | 34 | K3 | 57 | 42 | I/O |
| LDC (Low) | LDC (Low) | LDC (Low) | LDC (Low) | LDC (Low) | 20 | 30 | 36 | L3 | 59 | 44 | I/O |
| INIT ‡ | INIT ‡ | INIT ‡ | INIT ‡ | INIT ‡ | 22 | 34 | 42 | K6 | 65 | 50 | I/O |
| GND | GND | GND | GND | GND | 23 | 35 | 43 | J6 | 66 | 51 | GND |
| | | | | | 26 | 43 | 53 | L11 | 76 | 61 | XTL2–I/O |
| RESET | RESET | RESET | RESET | RESET | 27 | 44 | 54 | K10 | 78 | 63 | RESET |
| DONE | DONE | DONE | DONE | DONE | 28 | 45 | 55 | J10 | 80 | 65 | PROG |
| | | D7 | D7 | D7 | — | 46 | 56 | K11 | 81 | 66 | I/O |
| | | | | | 30 | 47 | 57 | J11 | 82 | 67 | XTL1–I/O |
| | | D6 | D6 | D6 | — | 48 | 58 | H10 | 83 | 68 | I/O |
| | | D5 | D5 | D5 | — | 49 | 60 | F10 | 87 | 72 | I/O |
| | | CS0 | — | — | — | 50 | 61 | G10 | 88 | 73 | I/O |
| | | D4 | D4 | D4 | — | 51 | 62 | G11 | 89 | 74 | I/O |
| VCC | VCC | VCC | VCC | VCC | 34 | 52 | 64 | G9 | 91 | 76 | VCC |
| | | D3 | D3 | D3 | — | 53 | 65 | F11 | 92 | 77 | I/O |
| | | CS1 | — | — | — | 54 | 66 | E11 | 93 | 78 | I/O |
| | | D2 | D2 | D2 | — | 55 | 67 | E10 | 94 | 79 | I/O |
| | | D1 | D1 | D1 | — | 56 | 70 | D10 | 98 | 83 | I/O |
| | | RDY/BUSY | RCLK | RCLK | — | 57 | 71 | C11 | 99 | 84 | I/O |
| DIN | DIN | D0 | D0 | D0 | 38 | 58 | 72 | B11 | 100 | 85 | I/O |
| DOUT | DOUT | DOUT | DOUT | DOUT | 39 | 59 | 73 | C10 | 1 | 86 | I/O |
| CCLK | CCLK | CCLK | CCLK | CCLK | 40 | 60 | 74 | A11 | 2 | 87 | CCLK |
| | | WS | A0 | A0 | — | 61 | 75 | B10 | 5 | 90 | I/O |
| | | CS2 | A1 | A1 | — | 62 | 76 | B9 | 6 | 91 | I/O |
| | | | A2 | A2 | — | 63 | 77 | A10 | 8 | 93 | I/O |
| | | | A3 | A3 | — | 64 | 78 | A9 | 9 | 94 | I/O |
| | | | A15 | A15 | — | 65 | 81 | B6 | 12 | 97 | I/O |
| | | | A4 | A4 | — | 66 | 82 | B7 | 13 | 98 | I/O |
| | | | A14 | A14 | — | 67 | 83 | A7 | 14 | 99 | I/O |
| | | | A5 | A5 | — | 68 | 84 | C7 | 15 | 100 | I/O |
| GND | GND | GND | GND | GND | 1 | 1 | 1 | C6 | 16 | 1 | GND |
| | | | A13 | A13 | — | 2 | 2 | A6 | 17 | 2 | I/O |
| | | | A6 | A6 | — | 3 | 3 | A5 | 18 | 3 | I/O |
| | | | A12 | A12 | — | 4 | 4 | B5 | 19 | 4 | I/O |
| | | | A7 | A7 | — | 5 | 5 | C5 | 20 | 5 | I/O |
| | | | A11 | A11 | — | 6 | 8 | A3 | 23 | 8 | I/O |
| | | | A8 | A8 | — | 7 | 9 | A2 | 24 | 9 | I/O |
| | | | A10 | A10 | — | 8 | 10 | B3 | 25 | 10 | I/O |
| | | | A9 | A9 | — | 9 | 11 | A1 | 26 | 11 | I/O |

☐ Represents a 50 kΩ to 100 kΩ pull-up.

* Peripheral mode and master parallel mode are not supported in the 44-PLCC package; see page 36.

† Pin assignments for the ATT3064/ATT3090 differ from those shown; see page 39.

‡ INIT is an open-drain output during configuration.

## Pin Information (continued)

### Table 6B. ATT3000 Family Configuration (100-TQFP, 132-PGA, 160-PQFP, 164-CQFP, 175-PGA, 208-SQFP)

| Configuration Mode (M2:M1:M0) | | | | | 100 TQFP | 132 PGA | 160 PQFP | 164 CQFP | 175 PGA | 208 SQFP | User Operation |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Slave (1:1:1) | Master-Serial (0:0:0) | Peripheral (1:0:1) | Master-High (1:1:0) | Master-Low (1:0:0) | | | | | | | |
| PWRDWN | PWRDWN | PWRDWN | PWRDWN | PWRDWN | 26 | A1 | 159 | 20 | B2 | 3 | PWRDWN |
| VCC | VCC | VCC | VCC | VCC | 38 | C8 | 20 | 42 | D9 | 26 | VCC |
| M1 (High) | M1 (Low) | M1 (Low) | M1 (High) | M1 (Low) | 49 | B13 | 40 | 62 | B14 | 48 | RDATA |
| M0 (High) | M0 (Low) | M0 (Low) | M0 (High) | M0 (Low) | 51 | A14 | 42 | 64 | B15 | 50 | RTRIG |
| M2 (High) | M2 (Low) | M2 (High) | M2 (High) | M2 (Low) | 53 | C13 | 44 | 66 | C15 | 56 | I/O |
| HDC (High) | HDC (High) | HDC (High) | HDC (High) | HDC (High) | 54 | B14 | 45 | 67 | E14 | 57 | I/O |
| LDC (Low) | LDC (Low) | LDC (Low) | LDC (Low) | LDC (Low) | 56 | D14 | 49 | 71 | D16 | 61 | I/O |
| INIT * | INIT * | INIT * | INIT * | INIT * | 62 | G14 | 59 | 81 | H15 | 77 | I/O |
| GND | GND | GND | GND | GND | 63 | H12 | 19 | 83 | J14 | 25 | GND |
| | | | | | 73 | M13 | 76 | 99 | P15 | 100 | XTL2–I/O |
| RESET | RESET | RESET | RESET | RESET | 75 | P14 | 78 | 101 | R15 | 102 | RESET |
| DONE | DONE | DONE | DONE | DONE | 77 | N13 | 80 | 103 | R14 | 107 | PROG |
| | | D7 | D7 | D7 | 78 | M12 | 81 | 104 | N13 | 109 | I/O |
| | | | | | 79 | P13 | 82 | 105 | T14 | 110 | XTL1–I/O |
| | | D6 | D6 | D6 | 80 | N11 | 86 | 109 | P12 | 115 | I/O |
| | | D5 | D5 | D5 | 84 | M9 | 92 | 115 | T11 | 122 | I/O |
| | | CS0 | — | — | 85 | N9 | 93 | 116 | R10 | 123 | I/O |
| | | D4 | D4 | D4 | 86 | N8 | 98 | 121 | R9 | 128 | I/O |
| VCC | VCC | VCC | VCC | VCC | 88 | M8 | 100 | 123 | N9 | 130 | VCC |
| | | D3 | D3 | D3 | 89 | N7 | 102 | 125 | P8 | 132 | I/O |
| | | CST | — | — | 90 | P6 | 103 | 126 | R8 | 133 | I/O |
| | | D2 | D2 | D2 | 91 | M6 | 108 | 131 | R7 | 138 | I/O |
| | | D1 | D1 | D1 | 95 | M5 | 114 | 137 | R5 | 145 | I/O |
| | | RDY/BUSY | RCLK | RCLK | 96 | N4 | 115 | 138 | P5 | 146 | I/O |
| DIN | DIN | D0 | D0 | D0 | 97 | N2 | 119 | 143 | R3 | 151 | I/O |
| DOUT | DOUT | DOUT | DOUT | DOUT | 98 | M3 | 120 | 144 | N4 | 152 | I/O |
| CCLK | CCLK | CCLK | CCLK | CCLK | 99 | P1 | 121 | 145 | R2 | 153 | CCLK |
| | | WS | A0 | A0 | 2 | M2 | 124 | 148 | P2 | 161 | I/O |
| | | CS2 | A1 | A1 | 3 | N1 | 125 | 149 | M3 | 162 | I/O |
| | | | A2 | A2 | 5 | L2 | 128 | 152 | P1 | 165 | I/O |
| | | | A3 | A3 | 6 | L1 | 129 | 153 | N1 | 166 | I/O |
| | | | A15 | A15 | 9 | K1 | 132 | 156 | M1 | 172 | I/O |
| | | | A4 | A4 | 10 | J2 | 133 | 157 | L2 | 173 | I/O |
| | | | A14 | A14 | 11 | H1 | 136 | 160 | K2 | 178 | I/O |
| | | | A5 | A5 | 12 | H2 | 137 | 161 | K1 | 179 | I/O |
| GND | GND | GND | GND | GND | 13 | H3 | 139 | 164 | J3 | 182 | GND |
| | | | A13 | A13 | 14 | G2 | 141 | 2 | H2 | 184 | I/O |
| | | | A6 | A6 | 15 | G1 | 142 | 3 | H1 | 185 | I/O |
| | | | A12 | A12 | 16 | F2 | 147 | 8 | F2 | 192 | I/O |
| | | | A7 | A7 | 17 | E1 | 148 | 9 | E1 | 193 | I/O |
| | | | A11 | A11 | 20 | D1 | 151 | 12 | D1 | 199 | I/O |
| | | | A8 | A8 | 21 | D2 | 152 | 13 | C1 | 200 | I/O |
| | | | A10 | A10 | 22 | B1 | 155 | 16 | E3 | 203 | I/O |
| | | | A9 | A9 | 23 | C2 | 156 | 17 | C2 | 204 | I/O |

☐ Represents a 50 kΩ to 100 kΩ pull-up.

* INIT is an open-drain output during configuration.

## Pin Assignments

**Table 7. ATT3030 44-Pin PLCC Pinout**

| Pin No. | Function | Pin No. | Function |
|---|---|---|---|
| 1 | GND | 23 | GND |
| 2 | I/O | 24 | I/O |
| 3 | I/O | 25 | I/O |
| 4 | I/O | 26 | XTL2(IN)–I/O |
| 5 | I/O | 27 | $\overline{\text{RESET}}$ |
| 6 | I/O | 28 | DONE–$\overline{\text{PROG}}$ |
| 7 | $\overline{\text{PWRDWN}}$ | 29 | I/O |
| 8 | TCLKIN–I/O | 30 | XTL1(OUT)–BCLKIN |
| 9 | I/O | 31 | I/O |
| 10 | I/O | 32 | I/O |
| 11 | I/O | 33 | I/O |
| 12 | Vcc | 34 | Vcc |
| 13 | I/O | 35 | I/O |
| 14 | I/O | 36 | I/O |
| 15 | I/O | 37 | I/O |
| 16 | M1–$\overline{\text{RDATA}}$ | 38 | DIN–I/O |
| 17 | M0–RTRIG | 39 | DOUT–I/O |
| 18 | M2–I/O | 40 | CCLK |
| 19 | HDC–I/O | 41 | I/O |
| 20 | $\overline{\text{LDC}}$–I/O | 42 | I/O |
| 21 | I/O | 43 | I/O |
| 22 | $\overline{\text{INIT}}$–I/O | 44 | I/O |

Notes:
Peripheral mode and master parallel mode are not supported in the M44 package.
Parallel address and data pins are not assigned.

## Pin Assignments (continued)

*Table 8. ATT3020, ATT3030, and ATT3042; 68-PLCC, 84-PLCC, and 84-PGA Pinout†*

| Pin Numbers | | | Function | Pin Numbers | | | Function |
|---|---|---|---|---|---|---|---|
| 68 PLCC | 84 PLCC | 84 PGA | | 68 PLCC | 84 PLCC | 84 PGA | |
| 10 | 12 | B2 | $\overline{\text{PWRDWN}}$ | 38 | 46 | K7 | I/O |
| 11 | 13 | C2 | TCLKIN–I/O | 39 | 47 | L6 | I/O |
| — | 14 | B1 | I/O* | 40 | 48 | L8 | I/O |
| 12 | 15 | C1 | I/O | 41 | 49 | K8 | I/O |
| 13 | 16 | D2 | I/O | — | 50 | L9 | I/O* |
| — | 17 | D1 | I/O | — | 51 | L10 | I/O* |
| 14 | 18 | E3 | I/O | 42 | 52 | K9 | I/O |
| 15 | 19 | E2 | I/O | 43 | 53 | L11 | XTL2(IN)–I/O |
| 16 | 20 | E1 | I/O | 44 | 54 | K10 | $\overline{\text{RESET}}$ |
| 17 | 21 | F2 | I/O | 45 | 55 | J10 | DONE–$\overline{\text{PROG}}$ |
| 18 | 22 | F3 | Vcc | 46 | 56 | K11 | D7–I/O |
| 19 | 23 | G3 | I/O | 47 | 57 | J11 | XTL1(OUT)–BCLKIN–I/O |
| — | 24 | G1 | I/O | 48 | 58 | H10 | D6–I/O |
| 20 | 25 | G2 | I/O | — | 59 | H11 | I/O |
| 21 | 26 | F1 | I/O | 49 | 60 | F10 | D5–I/O |
| 22 | 27 | H1 | I/O | 50 | 61 | G10 | $\overline{\text{CS0}}$–I/O |
| — | 28 | H2 | I/O | 51 | 62 | G11 | D4–I/O |
| 23 | 29 | J1 | I/O | — | 63 | G9 | I/O |
| 24 | 30 | K1 | I/O | 52 | 64 | F9 | Vcc |
| 25 | 31 | J2 | M1–$\overline{\text{RDATA}}$ | 53 | 65 | F11 | D3–I/O |
| 26 | 32 | L1 | M0–RTRIG | 54 | 66 | E11 | $\overline{\text{CS1}}$–I/O |
| 27 | 33 | K2 | M2–I/O | 55 | 67 | E10 | D2–I/O |
| 28 | 34 | K3 | HDC–I/O | — | 68 | E9 | I/O |
| 29 | 35 | L2 | I/O | — | 69 | D11 | I/O* |
| 30 | 36 | L3 | $\overline{\text{LDC}}$–I/O | 56 | 70 | D10 | D1–I/O |
| 31 | 37 | K4 | I/O | 57 | 71 | C11 | RDY/$\overline{\text{BUSY}}$–$\overline{\text{RCLK}}$–I/O |
| — | 38 | L4 | I/O* | 58 | 72 | B11 | D0–DIN–I/O |
| 32 | 39 | J5 | I/O | 59 | 73 | C10 | DOUT–I/O |
| 33 | 40 | K5 | I/O | 60 | 74 | A11 | CCLK |
| — | 41 | L5 | I/O* | 61 | 75 | B10 | A0–$\overline{\text{WS}}$–I/O |
| 34 | 42 | K6 | $\overline{\text{INIT}}$–I/O | 62 | 76 | B9 | A1–CS2–I/O |
| 35 | 43 | J6 | GND | 63 | 77 | A10 | A2–I/O |
| 36 | 44 | J7 | I/O | 64 | 78 | A9 | A3–I/O |
| 37 | 45 | L7 | I/O | — | 79 | B8 | I/O* |
| — | 80 | A8 | I/O* | 4 | 4 | B5 | A12–I/O |
| 65 | 81 | B6 | A15–I/O | 5 | 5 | C5 | A7–I/O |
| 66 | 82 | B7 | A4–I/O | — | 6 | A4 | I/O* |
| 67 | 83 | A7 | A14–I/O | — | 7 | B4 | I/O* |
| 68 | 84 | C7 | A5–I/O | 6 | 8 | A3 | A11–I/O |

* Indicates unconnected package pins for the ATT3020.

† Unprogrammed IOBs have a default pull-up; this prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-limited.

## Pin Assignments (continued)

**Table 8. ATT3020, ATT3030, and ATT3042; 68-PLCC, 84-PLCC, and 84-PGA Pinout† (continued)**

| Pin Numbers | | | Function | Pin Numbers | | | Function |
|---|---|---|---|---|---|---|---|
| 68 PLCC | 84 PLCC | 84 PGA | | 68 PLCC | 84 PLCC | 84 PGA | |
| 1 | 1 | C6 | GND | 7 | 9 | A2 | A8–I/O |
| 2 | 2 | A6 | A13–I/O | 8 | 10 | B3 | A10–I/O |
| 3 | 3 | A5 | A6–I/O | 9 | 11 | A1 | A9–I/O |

* Indicates unconnected package pins for the ATT3020.

† Unprogrammed IOBs have a default pull-up; this prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-limited.

Table 8 describes the pin assignments for three different chips in three different packages. The function column lists 84 of the 118 pads on the ATT3042 and 84 of the 98 pads on the ATT3030. Ten pads (indicated by an asterisk) do not exist on the ATT3020, which has 74 pads; therefore, the corresponding pins on the 84-pin packages have no connections to an ATT3020.

## Pin Assignments (continued)

**Table 9. ATT3064 and ATT3090 84-PLCC Pinout**

| 84 PLCC | Function | 84 PLCC | Function | 84 PLCC | Function |
|---|---|---|---|---|---|
| 12 | $\overline{\text{PWRDWN}}$ | 41 | $\overline{\text{INIT}}$–I/O* | 70 | D1–I/O |
| 13 | TCLKIN–I/O | 42 | Vcc* | 71 | RDY/$\overline{\text{BUSY}}$–RCLK–I/O |
| 14 | I/O | 43 | GND | 72 | D0–DIN–I/O |
| 15 | I/O | 44 | I/O | 73 | DOUT–I/O |
| 16 | I/O | 45 | I/O | 74 | CCLK |
| 17 | I/O | 46 | I/O | 75 | A0–$\overline{\text{WS}}$–I/O |
| 18 | I/O | 47 | I/O | 76 | A1–CS2–I/O |
| 19 | I/O | 48 | I/O | 77 | A2–I/O |
| 20 | I/O | 49 | I/O | 78 | A3–I/O |
| 21 | GND* | 50 | I/O | 79 | I/O* |
| 22 | Vcc | 51 | I/O | 80 | I/O* |
| 23 | I/O | 52 | I/O | 81 | A15–I/O |
| 24 | I/O | 53 | XTL2(IN)–I/O | 82 | A4–I/O |
| 25 | I/O | 54 | $\overline{\text{RESET}}$ | 83 | A14–I/O |
| 26 | I/O | 55 | DONE–$\overline{\text{PROG}}$ | 84 | A5–I/O |
| 27 | I/O | 56 | D7–I/O | 1 | GND |
| 28 | I/O | 57 | XTL1(OUT)–BCLKIN–I/O | 2 | Vcc* |
| 29 | I/O | 58 | D6–I/O | 3 | A13–I/O* |
| 30 | I/O | 59 | I/O | 4 | A6–I/O* |
| 31 | M1–$\overline{\text{RDATA}}$ | 60 | D5–I/O | 5 | A12–I/O* |
| 32 | M0–RTRIG | 61 | $\overline{\text{CS0}}$–I/O | 6 | A7–I/O* |
| 33 | M2–I/O | 62 | D4–I/O | 7 | I/O |
| 34 | HDC–I/O | 63 | I/O | 8 | A11–I/O |
| 35 | I/O | 64 | Vcc | 9 | A8–I/O |
| 36 | $\overline{\text{LDC}}$–I/O | 65 | GND* | 10 | A10–I/O |
| 37 | I/O | 66 | D3–I/O* | 11 | A9–I/O |
| 38 | I/O | 67 | $\overline{\text{CS1}}$–I/O* | — | — |
| 39 | I/O | 68 | D2–I/O* | — | — |
| 40 | I/O | 69 | I/O | — | — |

* Different pin definition than ATT3020/ATT3030/ATT3042 PC84 package.

Notes: Unprogrammed IOBs have a default pull-up; this prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-limited. DEVICE POWER MUST BE LESS THAN 1 WATT.

## Pin Assignments (continued)

**Table 10. ATT3020, ATT3030, and ATT3042; 100-CQFP and 100-PQFP Pinout**

| Pin Number | | Function | Pin Number | | Function | Pin Number | | Function |
|---|---|---|---|---|---|---|---|---|
| 100 CQFP | 100 PQFP | | 100 CQFP | 100 PQFP | | 100 CQFP | 100 PQFP | |
| 1 | 16 | GND | 35 | 50 | I/O* | 69 | 84 | I/O* |
| 2 | 17 | A13–I/O | 36 | 51 | I/O* | 70 | 85 | I/O* |
| 3 | 18 | A6–I/O | 37 | 52 | M1–$\overline{\text{RDATA}}$ | 71 | 86 | I/O |
| 4 | 19 | A12–I/O | 38 | 53 | GND* | 72 | 87 | D5–I/O |
| 5 | 20 | A7–I/O | 39 | 54 | M0–RTRIG | 73 | 88 | $\overline{\text{CS0}}$–I/O |
| 6 | 21 | I/O* | 40 | 55 | Vcc* | 74 | 89 | D4–I/O |
| 7 | 22 | I/O* | 41 | 56 | M2–I/O | 75 | 90 | I/O |
| 8 | 23 | A11–I/O | 42 | 57 | HDC–I/O | 76 | 91 | Vcc |
| 9 | 24 | A8–I/O | 43 | 58 | I/O | 77 | 92 | D3–I/O |
| 10 | 25 | A10–I/O | 44 | 59 | $\overline{\text{LDC}}$–I/O | 78 | 93 | $\overline{\text{CS1}}$–I/O |
| 11 | 26 | A9–I/O | 45 | 60 | I/O* | 79 | 94 | D2–I/O |
| 12 | 27* | Vcc | 46 | 61 | I/O* | 80 | 95 | I/O |
| 13 | 28* | GND | 47 | 62 | I/O | 81 | 96 | I/O* |
| 14 | 29 | $\overline{\text{PWRDWN}}$ | 48 | 63 | I/O | 82 | 97 | I/O* |
| 15 | 30 | TCLKIN–I/O | 49 | 64 | I/O | 83 | 98 | D1–I/O |
| 16 | 31 | I/O** | 50 | 65 | $\overline{\text{INIT}}$–I/O | 84 | 99 | $\overline{\text{RCLK}}$–RDY/$\overline{\text{BUSY}}$–I/O |
| 17 | 32 | I/O* | 51 | 66 | GND | 85 | 100 | D0–DIN–I/O |
| 18 | 33 | I/O* | 52 | 67 | I/O | 86 | 1 | DOUT–I/O |
| 19 | 34 | I/O | 53 | 68 | I/O | 87 | 2 | CCLK |
| 20 | 35 | I/O | 54 | 69 | I/O | 88 | 3 | Vcc* |
| 21 | 36 | I/O | 55 | 70 | I/O | 89 | 4 | GND* |
| 22 | 37 | I/O | 56 | 71 | I/O | 90 | 5 | A0–$\overline{\text{WS}}$–I/O |
| 23 | 38 | I/O | 57 | 72 | I/O | 91 | 6 | A1–CS2–I/O |
| 24 | 39 | I/O | 58 | 73 | I/O | 92 | 7 | I/O** |
| 25 | 40 | I/O | 59 | 74 | I/O* | 93 | 8 | A2–I/O |
| 26 | 41 | Vcc | 60 | 75 | I/O* | 94 | 9 | A3–I/O |
| 27 | 42 | I/O | 61 | 76 | XTAL2–I/O | 95 | 10 | I/O* |
| 28 | 43 | I/O | 62 | 77* | GND | 96 | 11 | I/O* |
| 29 | 44 | I/O | 63 | 78 | $\overline{\text{RESET}}$ | 97 | 12 | A15–I/O |
| 30 | 45 | I/O | 64 | 79 | Vcc* | 98 | 13 | A4–I/O |
| 31 | 46 | I/O | 65 | 80 | DONE–$\overline{\text{PROG}}$ | 99 | 14 | A14–I/O |
| 32 | 47 | I/O | 66 | 81 | D7–I/O | 100 | 15 | A5–I/O |
| 33 | 48 | I/O | 67 | 82 | XTAL1–BCLKIN–I/O | — | — | — |
| 34 | 49 | I/O | 68 | 83 | D6–I/O | — | — | — |

* The third column lists 100 of the 118 pads on the ATT3042 connected to the 100 package pins. Two pads, indicated by double asterisks, do not exist on the ATT3030, which has 98 pads; therefore, the corresponding pins have no connections. Twenty-six pads, indicated by single or double asterisks, do not exist on the ATT3020, which has 74 pads; therefore, the corresponding pins have no connections. (See Table 9.)

Notes: Unprogrammed IOBs have a default pull-up; this prevents an undefined pad level for unbonded or unused IOBs.
Programmed outputs are default slew-limited. The ATT3030 is **not** available in a 100-pin CQFP.

## Pin Assignments (continued)

**Table 11. ATT3030 and ATT3042 100-TQFP Pinout**

| 100 TQFP | Function | 100 TQFP | Function | 100 TQFP | Function |
|---|---|---|---|---|---|
| 13 | GND | 47 | I/O | 81 | I/O |
| 14 | A13–I/O | 48 | I/O | 82 | I/O |
| 15 | A6–I/O | 49 | M1–$\overline{\text{RDATA}}$ | 83 | I/O |
| 16 | A12–I/O | 50 | GND | 84 | D5–I/O |
| 17 | A7–I/O | 51 | M0–RTRIG | 85 | $\overline{\text{CS0}}$–I/O |
| 18 | I/O | 52 | Vcc | 86 | D4–I/O |
| 19 | I/O | 53 | M2–I/O | 87 | I/O |
| 20 | A11–I/O | 54 | HDC–I/O | 88 | Vcc |
| 21 | A8–I/O | 55 | I/O | 89 | D3–I/O |
| 22 | A10–I/O | 56 | $\overline{\text{LDC}}$–I/O | 90 | $\overline{\text{CS1}}$–I/O |
| 23 | A9–I/O | 57 | I/O | 91 | D2–I/O |
| 24 | Vcc | 58 | I/O | 92 | I/O |
| 25 | GND | 59 | I/O | 93 | I/O |
| 26 | $\overline{\text{PWRDWN}}$ | 60 | I/O | 94 | I/O |
| 26 | TCLKIN–I/O | 61 | I/O | 95 | D1–I/O |
| 28 | I/O | 62 | $\overline{\text{INIT}}$–I/O | 96 | $\overline{\text{RCLK}}$–RDY/$\overline{\text{BUSY}}$–I/O* |
| 29 | I/O | 63 | GND | 97 | D0–DIN–I/O |
| 30 | I/O | 64 | I/O | 98 | DOUT–I/O |
| 31 | I/O | 65 | I/O | 99 | CCLK |
| 32 | I/O | 66 | I/O | 100 | Vcc |
| 33 | I/O | 67 | I/O | 1 | GND |
| 34 | I/O | 68 | I/O | 2 | A0–$\overline{\text{WS}}$–I/O |
| 35 | I/O | 69 | I/O | 3 | A1–CS2–I/O |
| 36 | I/O | 70 | I/O | 4 | I/O* |
| 37 | I/O | 71 | I/O | 5 | A2–I/O |
| 38 | Vcc | 72 | I/O | 6 | A3–I/O |
| 39 | I/O | 73 | XTAL2–I/O | 7 | I/O |
| 40 | I/O | 74 | GND | 8 | I/O |
| 41 | I/O | 75 | $\overline{\text{RESET}}$ | 9 | A15–I/O |
| 42 | I/O | 76 | Vcc | 10 | A4–I/O |
| 43 | I/O | 77 | DONE–$\overline{\text{PROG}}$ | 11 | A14–I/O |
| 44 | I/O | 78 | D7–I/O | 12 | A5–I/O |
| 45 | I/O | 79 | XTAL1–BCLKIN–I/O | — | — |
| 46 | I/O | 80 | D6–I/O | — | — |

* Indicates unconnected package pins for the ATT3030.

Notes: Unprogrammed IOBs have a default pull-up; this prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-limited. DEVICE POWER MUST BE LESS THAN 1 WATT FOR COMMERCIAL TEMPERATURE RANGE AND LESS THAN 0.8 WATTS FOR INDUSTRIAL TEMPERATURE RANGE.

## Pin Assignments (continued)

**Table 12. ATT3042 and ATT3064 132-PGA Pinout**

| 132 PGA | Function | 132 PGA | Function | 132 PGA | Function |
|---|---|---|---|---|---|
| C4 | GND | F12 | I/O | N6 | I/O* |
| A1 | PWRDWN | E14 | I/O | P5 | I/O* |
| C3 | TCLKIN–I/O | F13 | I/O | M6 | D2–I/O |
| B2 | I/O | F14 | I/O | N5 | I/O |
| B3 | I/O | G13 | I/O | P4 | I/O |
| A2 | I/O* | G14 | INIT–I/O | P3 | I/O |
| B4 | I/O | G12 | VCC | M5 | D1–I/O |
| C5 | I/O | H12 | GND | N4 | RCLK–RDY/BUSY–I/O |
| A3 | I/O* | H14 | I/O | P2 | I/O |
| A4 | I/O | H13 | I/O | N3 | I/O |
| B5 | I/O | J14 | I/O | N2 | D0–DIN–I/O |
| C6 | I/O | J13 | I/O | M3 | DOUT–I/O |
| A5 | I/O | K14 | I/O | P1 | CCLK |
| B6 | I/O | J12 | I/O | M4 | VCC |
| A6 | I/O | K13 | I/O | L3 | GND |
| B7 | I/O | L14 | I/O* | M2 | A0–WS–I/O |
| C7 | GND | L13 | I/O | N1 | A1–CS2–I/O |
| C8 | VCC | K12 | I/O | M1 | I/O |
| A7 | I/O | M14 | I/O | K3 | I/O |
| B8 | I/O | N14 | I/O | L2 | A2–I/O |
| A8 | I/O | M13 | XTAL2(IN)–I/O | L1 | A3–I/O |
| A9 | I/O | L12 | GND | K2 | I/O |
| B9 | I/O | P14 | RESET | J3 | I/O |
| C9 | I/O | M11 | VCC | K1 | A15–I/O |
| A10 | I/O | N13 | DONE–PROG | J2 | A4–I/O |
| B10 | I/O | M12 | D7–I/O | J1 | I/O* |
| A11 | I/O* | P13 | XTAL1–BCLKIN–I/O | H1 | A14–I/O |
| C10 | I/O | N12 | I/O | H2 | A5–I/O |
| B11 | I/O | P12 | I/O | H3 | GND |
| A12 | I/O* | N11 | D6–I/O | G3 | VCC |
| B12 | I/O | M10 | I/O | G2 | A13–I/O |
| A13 | I/O* | P11 | I/O* | G1 | A6–I/O |
| C12 | I/O | N10 | I/O | F1 | I/O* |
| B13 | M1–RDATA | P10 | I/O | F2 | A12–I/O |
| C11 | GND | M9 | D5–I/O | E1 | A7–I/O |
| A14 | M0–RTRIG | N9 | CS0–I/O | F3 | I/O |
| D12 | VCC | P9 | I/O* | E2 | I/O |
| C13 | M2–I/O | P8 | I/O* | D1 | A11–I/O |
| B14 | HDC–I/O | N8 | D4–I/O | D2 | A8–I/O |
| C14 | I/O | P7 | I/O | E3 | I/O |
| E12 | I/O | M8 | VCC | C1 | I/O |
| D13 | I/O | M7 | GND | B1 | A10–I/O |
| D14 | LDC–I/O | N7 | D3–I/O | C2 | A9–I/O |
| E13 | I/O* | P6 | CS1–I/O | D3 | VCC |

* Indicates unconnected package pins for the ATT3030.

Notes: Unprogrammed IOBs have a default pull-up; this prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-limited.

## Pin Assignments (continued)

**Table 13. ATT3064 and ATT3090 160-PQFP Pinout**

| 160 PQFP | Function | 160 PQFP | Function | 160 PQFP | Function | 160 PQFP | Function |
|---|---|---|---|---|---|---|---|
| 1 | I/O* | 41 | GND | 81 | D7–I/O | 121 | CCLK |
| 2 | I/O* | 42 | M0–RTRIG | 82 | XTAL1–BCLKIN–I/O | 122 | Vcc |
| 3 | I/O* | 43 | Vcc | 83 | I/O* | 123 | GND |
| 4 | I/O | 44 | M2–I/O | 84 | I/O | 124 | A0–$\overline{WS}$–I/O |
| 5 | I/O | 45 | HDC–I/O | 85 | I/O | 125 | A1–CS2–I/O |
| 6 | I/O | 46 | I/O | 86 | D6–I/O | 126 | I/O |
| 7 | I/O | 47 | I/O | 87 | I/O | 127 | I/O |
| 8 | I/O | 48 | I/O | 88 | I/O | 128 | A2–I/O |
| 9 | I/O | 49 | $\overline{LDC}$–I/O | 89 | I/O | 129 | A3–I/O |
| 10 | I/O | 50 | I/O* | 90 | I/O | 130 | I/O |
| 11 | I/O | 51 | I/O* | 91 | I/O | 131 | I/O |
| 12 | I/O | 52 | I/O | 92 | D5–I/O | 132 | A15–I/O |
| 13 | I/O | 53 | I/O | 93 | $\overline{CS0}$–I/O | 133 | A4–I/O |
| 14 | I/O | 54 | I/O | 94 | I/O* | 134 | I/O |
| 15 | I/O | 55 | I/O | 95 | I/O* | 135 | I/O |
| 16 | I/O | 56 | I/O | 96 | I/O | 136 | A14–I/O |
| 17 | I/O | 57 | I/O | 97 | I/O | 137 | A5–I/O |
| 18 | I/O | 58 | I/O | 98 | D4–I/O | 138 | I/O* |
| 19 | GND | 59 | $\overline{INIT}$–I/O | 99 | I/O | 139 | GND |
| 20 | Vcc | 60 | Vcc | 100 | Vcc | 140 | Vcc |
| 21 | I/O* | 61 | GND | 101 | GND | 141 | A13–I/O |
| 22 | I/O | 62 | I/O | 102 | D3–I/O | 142 | A6–I/O |
| 23 | I/O | 63 | I/O | 103 | $\overline{CST}$–I/O | 143 | I/O* |
| 24 | I/O | 64 | I/O | 104 | I/O | 144 | I/O* |
| 25 | I/O | 65 | I/O | 105 | I/O | 145 | I/O |
| 26 | I/O | 66 | I/O | 106 | I/O* | 146 | I/O |
| 27 | I/O | 67 | I/O | 107 | I/O* | 147 | A12–I/O |
| 28 | I/O | 68 | I/O | 108 | D2–I/O | 148 | A7–I/O |
| 29 | I/O | 69 | I/O | 109 | I/O | 149 | I/O |
| 30 | I/O | 70 | I/O | 110 | I/O | 150 | I/O |
| 31 | I/O | 71 | I/O | 111 | I/O | 151 | A11–I/O |
| 32 | I/O | 72 | I/O | 112 | I/O | 152 | A8–I/O |
| 33 | I/O | 73 | I/O | 113 | I/O | 153 | I/O |
| 34 | I/O | 74 | I/O | 114 | D1–I/O | 154 | I/O |
| 35 | I/O | 75 | I/O* | 115 | $\overline{RCLK}$–RDY/$\overline{BUSY}$–I/O | 155 | A10–I/O |
| 36 | I/O | 76 | XTAL2–I/O | 116 | I/O | 156 | A9–I/O |
| 37 | I/O | 77 | GND | 117 | I/O | 157 | Vcc |
| 38 | I/O* | 78 | $\overline{RESET}$ | 118 | I/O* | 158 | GND |
| 39 | I/O* | 79 | Vcc | 119 | D0–DIN–I/O | 159 | $\overline{PWRDWN}$ |
| 40 | M1–$\overline{RDATA}$ | 80 | DONE–$\overline{PROG}$ | 120 | DOUT–I/O | 160 | TCLKIN–I/O |

* Not connected on ATT3064.

Notes: Unprogrammed IOBs have a default pull-up; this prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-limited. DEVICE POWER MUST BE LESS THAN 1 WATT FOR COMMERCIAL TEMPERATURE RANGE AND LESS THAN 0.8 WATTS FOR INDUSTRIAL TEMPERATURE RANGE.

## Pin Assignments (continued)

**Table 14. ATT3000 Family 164-CQFP Pinout**

| 164 CQFP | Function | 164 CQFP | Function | 164 CQFP | Function | 164 CQFP | Function |
|---|---|---|---|---|---|---|---|
| 20 | $\overline{\text{PWRDWN}}$ | 61 | I/O | 102 | Vcc | 143 | D0–DIN–I/O |
| 21 | TCLKIN–I/O | 62 | M1–$\overline{\text{RDATA}}$ | 103 | DONE–$\overline{\text{PROG}}$ | 144 | DOUT–I/O |
| 22 | I/O | 63 | GND | 104 | D7–I/O | 145 | CCLK |
| 23 | I/O | 64 | M0–RTRIG | 105 | XTAL1(OUT)-BCLKIN-I/O | 146 | Vcc |
| 24 | I/O | 65 | Vcc | 106 | I/O | 147 | GND |
| 25 | I/O | 66 | M2–I/O | 107 | I/O | 148 | A0–$\overline{\text{WS}}$–I/O |
| 26 | I/O | 67 | HDC–I/O | 108 | I/O | 149 | A1–CS2–I/O |
| 27 | I/O | 68 | I/O | 109 | D6–I/O | 150 | I/O |
| 28 | I/O | 69 | I/O | 110 | I/O | 151 | I/O |
| 29 | I/O | 70 | I/O | 111 | I/O | 152 | A2–I/O |
| 30 | I/O | 71 | $\overline{\text{LDC}}$–I/O | 112 | I/O | 153 | A3–I/O |
| 31 | I/O | 72 | I/O | 113 | I/O | 154 | I/O |
| 32 | I/O | 73 | I/O | 114 | I/O | 155 | I/O |
| 33 | I/O | 74 | I/O | 115 | D5–I/O | 156 | A15–I/O |
| 34 | I/O | 75 | I/O | 116 | $\overline{\text{CS0}}$–I/O | 157 | A4–I/O |
| 35 | I/O | 76 | I/O | 117 | I/O | 158 | I/O |
| 36 | I/O | 77 | I/O | 118 | I/O | 159 | I/O |
| 37 | I/O | 78 | I/O | 119 | I/O | 160 | A14–I/O |
| 38 | I/O | 79 | I/O | 120 | I/O | 161 | A5–I/O |
| 39 | I/O | 80 | I/O | 121 | D4–I/O | 162 | I/O |
| 40 | I/O | 81 | $\overline{\text{INIT}}$–I/O | 122 | I/O | 163 | I/O |
| 41 | GND | 82 | Vcc | 123 | Vcc | 164 | GND |
| 42 | Vcc | 83 | GND | 124 | GND | 1 | Vcc |
| 43 | I/O | 84 | I/O | 125 | D3–I/O | 2 | A13–I/O |
| 44 | I/O | 85 | I/O | 126 | $\overline{\text{CS1}}$–I/O | 3 | A6–I/O |
| 45 | I/O | 86 | I/O | 127 | I/O | 4 | I/O |
| 46 | I/O | 87 | I/O | 128 | I/O | 5 | I/O |
| 47 | I/O | 88 | I/O | 129 | I/O | 6 | I/O |
| 48 | I/O | 89 | I/O | 130 | I/O | 7 | I/O |
| 49 | I/O | 90 | I/O | 131 | D2–I/O | 8 | A12–I/O |
| 50 | I/O | 91 | I/O | 132 | I/O | 9 | A7–I/O |
| 51 | I/O | 92 | I/O | 133 | I/O | 10 | I/O |
| 52 | I/O | 93 | I/O | 134 | I/O | 11 | I/O |
| 53 | I/O | 94 | I/O | 135 | I/O | 12 | A11–I/O |
| 54 | I/O | 95 | I/O | 136 | I/O | 13 | A8–I/O |
| 55 | I/O | 96 | I/O | 137 | D1–I/O | 14 | I/O |
| 56 | I/O | 97 | I/O | 138 | RDY/$\overline{\text{BUSY}}$–RCLK–I/O | 15 | I/O |
| 57 | I/O | 98 | I/O | 139 | I/O | 16 | A10–I/O |
| 58 | I/O | 99 | XTAL2(IN)–I/O | 140 | I/O | 17 | A9–I/O |
| 59 | I/O | 100 | GND | 141 | I/O | 18 | Vcc |
| 60 | I/O | 101 | $\overline{\text{RESET}}$ | 142 | I/O | 19 | GND |

Notes: Unprogrammed IOBs have a default pull-up; this prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-limited.

## Pin Assignments (continued)

**Table 15. ATT3000 Family 175-PGA Pinout**

| 175 PGA | Function | 175 PGA | Function | 175 PGA | Function | 175 PGA | Function |
|---|---|---|---|---|---|---|---|
| B2 | $\overline{\text{PWRDWN}}$ | D13 | I/O | R14 | DONE–$\overline{\text{PROG}}$ | R3 | D0–DIN–I/O |
| D4 | TCLKIN–I/O | B14 | M1–$\overline{\text{RDATA}}$ | N13 | D7–I/O | N4 | DOUT–I/O |
| B3 | I/O | C14 | GND | T14 | XTAL1(OUT)-BCLKIN-I/O | R2 | CCLK |
| C4 | I/O | B15 | M0–RTRIG | P13 | I/O | P3 | Vcc |
| B4 | I/O | D14 | Vcc | R13 | I/O | N3 | GND |
| A4 | I/O | C15 | M2–I/O | T13 | I/O | P2 | A0–$\overline{\text{WS}}$–I/O |
| D5 | I/O | E14 | HDC–I/O | N12 | I/O | M3 | A1–CS2–I/O |
| C5 | I/O | B16 | I/O | P12 | D6–I/O | R1 | I/O |
| B5 | I/O | D15 | I/O | R12 | I/O | N2 | I/O |
| A5 | I/O | C16 | I/O | T12 | I/O | P1 | A2–I/O |
| C6 | I/O | D16 | $\overline{\text{LDC}}$–I/O | P11 | I/O | N1 | A3–I/O |
| D6 | I/O | F14 | I/O | N11 | I/O | L3 | I/O |
| B6 | I/O | E15 | I/O | R11 | I/O | M2 | I/O |
| A6 | I/O | E16 | I/O | T11 | D5–I/O | M1 | A15–I/O |
| B7 | I/O | F15 | I/O | R10 | $\overline{\text{CS0}}$–I/O | L2 | A4–I/O |
| C7 | I/O | F16 | I/O | P10 | I/O | L1 | I/O |
| D7 | I/O | G14 | I/O | N10 | I/O | K3 | I/O |
| A7 | I/O | G15 | I/O | T10 | I/O | K2 | A14–I/O |
| A8 | I/O | G16 | I/O | T9 | I/O | K1 | A5–I/O |
| B8 | I/O | H16 | I/O | R9 | D4–I/O | J1 | I/O |
| C8 | I/O | H15 | $\overline{\text{INIT}}$–I/O | P9 | I/O | J2 | I/O |
| D8 | GND | H14 | Vcc | N9 | Vcc | J3 | GND |
| D9 | Vcc | J14 | GND | N8 | GND | H3 | Vcc |
| C9 | I/O | J15 | I/O | P8 | D3–I/O | H2 | A13–I/O |
| B9 | I/O | J16 | I/O | R8 | $\overline{\text{CST}}$–I/O | H1 | A6–I/O |
| A9 | I/O | K16 | I/O | T8 | I/O | G1 | I/O |
| A10 | I/O | K15 | I/O | T7 | I/O | G2 | I/O |
| D10 | I/O | K14 | I/O | N7 | I/O | G3 | I/O |
| C10 | I/O | L16 | I/O | P7 | I/O | F1 | I/O |
| B10 | I/O | L15 | I/O | R7 | D2–I/O | F2 | A12–I/O |
| A11 | I/O | M16 | I/O | T6 | I/O | E1 | A7–I/O |
| B11 | I/O | M15 | I/O | R6 | I/O | E2 | I/O |
| D11 | I/O | L14 | I/O | N6 | I/O | F3 | I/O |
| C11 | I/O | N16 | I/O | P6 | I/O | D1 | A11–I/O |
| A12 | I/O | P16 | I/O | T5 | I/O | C1 | A8–I/O |
| B12 | I/O | N15 | I/O | R5 | D1–I/O | D2 | I/O |
| C12 | I/O | R16 | I/O | P5 | RDY/$\overline{\text{BUSY}}$–$\overline{\text{RCLK}}$–I/O | B1 | I/O |
| D12 | I/O | M14 | I/O | N5 | I/O | E3 | A10–I/O |
| A13 | I/O | P15 | XTAL2(IN)–I/O | T4 | I/O | C2 | A9–I/O |
| B13 | I/O | N14 | GND | R4 | I/O | D3 | Vcc |
| C13 | I/O | R15 | $\overline{\text{RESET}}$ | P4 | I/O | C3 | GND |
| A14 | I/O | P14 | Vcc | — | — | — | — |

Notes: Unprogrammed IOBs have a default pull-up; this prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-limited. Pins A2, A3, A15, A16, T1, T2, T3, T15, and T16 are not connected. Pin A1 does not exist.

## Pin Assignments (continued)

**Table 16. ATT3000 Family 208-SQFP Pinout**

| 208 QFP | Function | 208 QFP | Function | 208 QFP | Function | 208 QFP | Function |
|---|---|---|---|---|---|---|---|
| 1 | — | 53 | — | 105 | — | 157 | — |
| 2 | GND | 54 | — | 106 | VCC | 158 | — |
| 3 | PWRDWN | 55 | VCC | 107 | DONE–PROG | 159 | — |
| 4 | TCLKIN–I/O | 56 | M2–I/O | 108 | — | 160 | GND |
| 5 | I/O | 57 | HDC–I/O | 109 | D7–I/O | 161 | A0–WS–I/O |
| 6 | I/O | 58 | I/O | 110 | XTAL–BCLKIN–I/O | 162 | A1–CS2–I/O |
| 7 | I/O | 59 | I/O | 111 | I/O | 163 | I/O |
| 8 | I/O | 60 | I/O | 112 | I/O | 164 | I/O |
| 9 | I/O | 61 | LDC–I/O | 113 | I/O | 165 | A2–I/O |
| 10 | I/O | 62 | I/O | 114 | I/O | 166 | A3–I/O |
| 11 | I/O | 63 | I/O | 115 | D6–I/O | 167 | I/O |
| 12 | I/O | 64 | — | 116 | I/O | 168 | I/O |
| 13 | I/O | 65 | — | 117 | I/O | 169 | — |
| 14 | I/O | 66 | — | 118 | I/O | 170 | — |
| 15 | I/O | 67 | — | 119 | — | 171 | — |
| 16 | I/O | 68 | I/O | 120 | I/O | 172 | A15–I/O |
| 17 | I/O | 69 | I/O | 121 | I/O | 173 | A4–I/O |
| 18 | I/O | 70 | I/O | 122 | D5–I/O | 174 | I/O |
| 19 | I/O | 71 | I/O | 123 | CS0–I/O | 175 | I/O |
| 20 | I/O | 72 | — | 124 | I/O | 176 | — |
| 21 | I/O | 73 | — | 125 | I/O | 177 | — |
| 22 | I/O | 74 | I/O | 126 | I/O | 178 | A14–I/O |
| 23 | I/O | 75 | I/O | 127 | I/O | 179 | A5–I/O |
| 24 | I/O | 76 | I/O | 128 | D4–I/O | 180 | I/O |
| 25 | GND | 77 | INIT–I/O | 129 | I/O | 181 | I/O |
| 26 | VCC | 78 | VCC | 130 | VCC | 182 | GND |
| 27 | I/O | 79 | GND | 131 | GND | 183 | VCC |
| 28 | I/O | 80 | I/O | 132 | D3–I/O | 184 | A13–I/O |
| 29 | I/O | 81 | I/O | 133 | CS1–I/O | 185 | A6–I/O |
| 30 | I/O | 82 | I/O | 134 | I/O | 186 | I/O |
| 31 | I/O | 83 | — | 135 | I/O | 187 | I/O |
| 32 | I/O | 84 | — | 136 | I/O | 188 | — |
| 33 | I/O | 85 | I/O | 137 | I/O | 189 | — |
| 34 | I/O | 86 | I/O | 138 | D2–I/O | 190 | I/O |
| 35 | I/O | 87 | I/O | 139 | I/O | 191 | I/O |
| 36 | I/O | 88 | I/O | 140 | I/O | 192 | A12–I/O |
| 37 | — | 89 | I/O | 141 | I/O | 193 | A7–I/O |
| 38 | I/O | 90 | — | 142 | — | 194 | — |
| 39 | I/O | 91 | — | 143 | I/O | 195 | — |
| 40 | I/O | 92 | — | 144 | I/O | 196 | — |
| 41 | I/O | 93 | I/O | 145 | D1–I/O | 197 | I/O |
| 42 | I/O | 94 | I/O | 146 | RDY/BUSY–RCLK–I/O | 198 | I/O |
| 43 | I/O | 95 | I/O | 147 | I/O | 199 | A11–I/O |
| 44 | I/O | 96 | I/O | 148 | I/O | 200 | A8–I/O |
| 45 | I/O | 97 | I/O | 149 | I/O | 201 | I/O |
| 46 | I/O | 98 | I/O | 150 | I/O | 202 | I/O |
| 47 | I/O | 99 | I/O | 151 | D0–DIN–I/O | 203 | A10–I/O |
| 48 | M1–RDATA | 100 | XTAL2(IN)–I/O | 152 | DOUT–I/O | 204 | A9–I/O |
| 49 | GND | 101 | GND | 153 | CCLK | 205 | VCC |
| 50 | M0–RTRIG | 102 | RESET | 154 | VCC | 206 | — |
| 51 | — | 103 | — | 155 | — | 207 | — |
| 52 | — | 104 | — | 156 | — | 208 | — |

Notes: Unprogrammed IOBs have a default pull-up; this prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-limited.

## Absolute Maximum Ratings

*Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability.*

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Supply Voltage Relative to GND | $V_{CC}$ | –0.5 | 7.0 | V |
| Input Voltage Relative to GND | $V_{IN}$ | –0.5 | 0.5 | V |
| Voltage Applied to 3-state Output | $V_{TS}$ | –0.5 | 0.5 | V |
| Storage Temperature (ambient) | $T_{stg}$ | –65 | 150 | °C |
| Maximum Soldering Temperature (10 seconds at 1/16 in.) | $T_{SOL}$ | — | 260 | °C |
| Junction Temperature | | | | |
| Plastic | $T_J$ | — | 125 | °C |
| Ceramic | $T_J$ | — | 150 | °C |

# Electrical Characteristics

### Table 17. dc Electrical Characteristics Over Operating Conditions

Commercial: $V_{CC}$ = 5.0 V ± 5%; 0 °C ≤ $T_A$ ≤ 70 °C; Industrial: $V_{CC}$ = 5.0 ± 10%, –40 °C ≤ $T_A$ ≤ 85 °C;
Military: $V_{CC}$ = 5.0 V ± 10%, –55 °C ≤ $T_A$ ≤ 125 °C.

| Parameter/Conditions | Symbol | Commercial | | Industrial | | Military | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| High-level Input Voltage | | | | | | | | |
| CMOS Level | $V_{IHC}$ | 70% | 100% | 70% | 100% | 3.76 | — | V |
| TTL Level | $V_{IHT}$ | 2.0 | $V_{CC}$ | 2.0 | $V_{CC}$ | 2.0 | $V_{CC}$ | V |
| Low-level Input Voltage | | | | | | | | |
| CMOS Level | $V_{ILC}$ | 0 | 20% | 0 | 20% | — | 0.37 | V |
| TTL Level | $V_{ILT}$ | 0 | 0.8 | 0 | 0.8 | 0 | 0.8 | V |
| Input Signal Transition Time | $T_{IN}$ | — | 250 | — | 250 | — | 250 | ns |
| Powerdown Supply Current | | | | | | | | |
| ATT3020 | $I_{CCPD}$ | — | 50 | — | 50 | — | 500 | µA |
| ATT3030 | | — | 80 | — | 80 | — | — | µA |
| ATT3042 | | — | 120 | — | 120 | — | 1150 | µA |
| ATT3064 | | — | 170 | — | 170 | — | — | µA |
| ATT3090 | | — | 250 | — | 250 | — | 2500 | µA |
| Quiescent FPGA Supply Current (in addition to $I_{CCPD}$) | | | | | | | | |
| CMOS Inputs | | | | | | | | |
| ATT3020 | $I_{CCO}$ | — | 500 | — | 500 | — | 1000 | µA |
| ATT3030 | | — | 500 | — | 500 | — | — | µA |
| ATT3042 | | — | 500 | — | 500 | — | 1650 | µA |
| ATT3064 | | — | 500 | — | 500 | — | — | µA |
| ATT3090 | | — | 500 | — | 500 | — | 3000 | µA |
| TTL Inputs | | — | 10 | — | 10 | — | 15 | mA |
| Leakage Current | $I_{IL}$ | –10 | 10 | –10 | 10 | –20 | 20 | µA |
| Input Capacitance* | | | | | | | | |
| All Packages (except 175-PGA) | | | | | | | | |
| All Pins Except XTL1 and XTL2 | $C_{IN}$ | — | 10 | — | 10 | — | 10 | pF |
| XTL1 and XTL2 | | — | 15 | — | 15 | — | 15 | pF |
| 175-PGA Package | | | | | | | | |
| All Pins Except XTL1 and XTL2 | | — | 15 | — | 15 | — | 15 | pF |
| XTL1 and XTL2 | | — | 20 | — | 20 | — | 20 | pF |
| Pad Pull-up* (when selected) (at $V_{IN}$ = 0 V) | $I_{RIN}$ | 0.02 | 0.17 | 0.02 | 0.17 | 0.02 | 0.17 | mA |
| Horizontal Long Line Pull-up (when selected) at logic LOW | $I_{RLL}$ | 0.2 | 2.5 | 0.2 | 2.5 | 0.2 | 2.5 | mA |

* Sample tested.

Note: With no output current loads, no active input or long line pull-up resistors, all package pins at $V_{CC}$ or GND, and the FPGA configured with a MAKEBITS tie option. See FPGA power chart for additional activity-dependent operating components.

## Electrical Characteristics (continued)

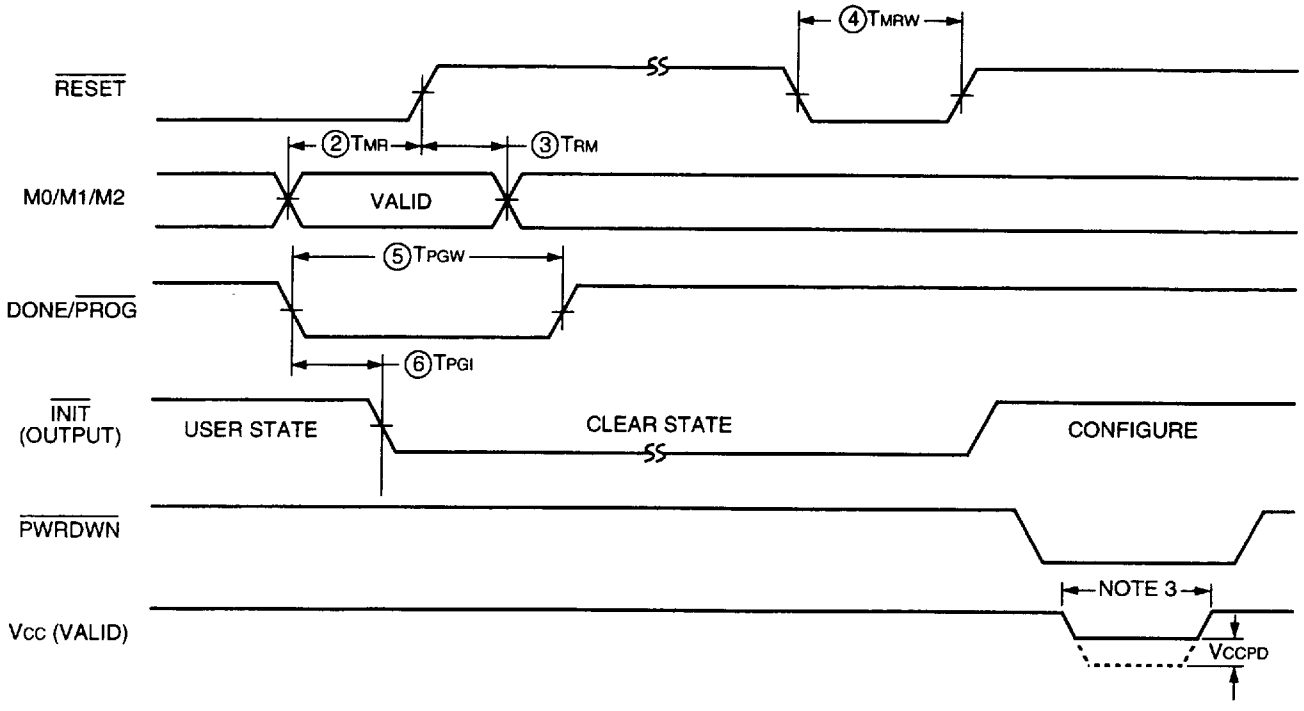



**Figure 33. General FPGA Switching Characteristics**

Testing of the switching characteristics is modeled after testing specified by MIL-M-38510/605. Devices are 100% functionally tested. Actual worst-case timing is provided by the timing calculator or simulation.

**Table 18. General FPGA Switching Characteristics**

| Signal | Description | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| RESET[1] | M0, M1, and M2 Setup Time | TMR (2) | 1 | — | µs |
| | M0, M1, and M2 Hold Time | TRM (3) | 1 | — | µs |
| | RESET Width (LOW) Required for Abort | TMRW (4) | 6 | — | µs |
| DONE/PROG | Width low Required for Reconfiguration | TPGW (5) | 6 | — | µs |
| | INIT Response after DONE/PROG Is Pulled low | TPGI (6) | — | 7 | µs |
| VCC[2] | Powerdown VCC | | | | |
| | Commercial/Industrial | VCCPD | 2.3 | — | V |
| | Military | | 3.5 | — | V |

Notes:
1. RESET timing relative to valid mode lines (M0, M1, M2) is relevant when RESET is used to delay configuration.
2. PWRDWN transitions must occur while VCC > 4 V.
3. At powerup, VCC must rise from 2 V to VCC minimum in less than 25 ms. If this is not possible, configuration can be delayed by holding RESET low until VCC has reached 4 V. A very long VCC rise time of >100 ms or a nonmonotonically rising VCC may require a >1 µs high level on RESET, followed by a >6 µs low level on RESET and DONE/PROG after VCC has reached 4 V.

## Electrical Characteristics (continued)

### Table 19. Buffer (Internal) Switching Characteristics

Commercial: $V_{CC}$ = 5.0 V ± 5%; 0 °C ≤ $T_A$ ≤ 70 °C; Industrial: $V_{CC}$ = 5.0 ± 10%, –40 °C ≤ $T_A$ ≤ 85 °C;
Military: $V_{CC}$ = 5.0 V ± 10%, –55 °C ≤ $T_A$ ≤ 125 °C.

| Description | Symbol | –50 | –70 | –100 | –125 | –150 | Unit |
|---|---|---|---|---|---|---|---|
| | | Max | Max | Max | Max | Max | |
| Global and Alternate Clock Distribution*: | | | | | | | |
| Either Normal IOB Input Pad to Clock Buffer Input | $T_{PID}$ | 10.0 | 8.0 | 7.5 | 7.0 | 6.8 | ns |
| Or Fast (CMOS only) Input Pad to Clock Buffer Input | $T_{PIDC}$ | 8.0 | 6.5 | 8.0 | 5.7 | 5.5 | ns |
| TBUF Driving a Horizontal Long Line (LL)*: | | | | | | | |
| I to LL While T is Low (buffer active) | $T_{IO}$ | 8.0 | 5.0 | 4.7 | 4.5 | 4.1 | ns |
| T↓ to LL Active and Valid with Single Pull-up Resistor | $T_{ON}$ | 12.0 | 11.0 | 10.0 | 9.0 | 5.6 | ns |
| T↓ to LL Active and Valid with Pair of Pull-up Resistors | $T_{ON}$ | 14.0 | 12.0 | 11.0 | 10.0 | 7.1 | ns |
| T↑ to LL High with Single Pull-up Resistor | $T_{PUS}$ | 42.0 | 24.0 | 22.0 | 17.0 | 15.6 | ns |
| T↑ to LL High with Pair of Pull-up Resistors | $T_{PUF}$ | 22.0 | 17.0 | 15.0 | 12.0 | 12.0 | ns |
| Bidirectional Buffer Delay | $T_{BIDI}$ | 6.0 | 2.0 | 1.8 | 1.7 | 1.4 | ns |

* Timing is based on the ATT3042; for other devices, see timing calculator.

## Electrical Characteristics (continued)

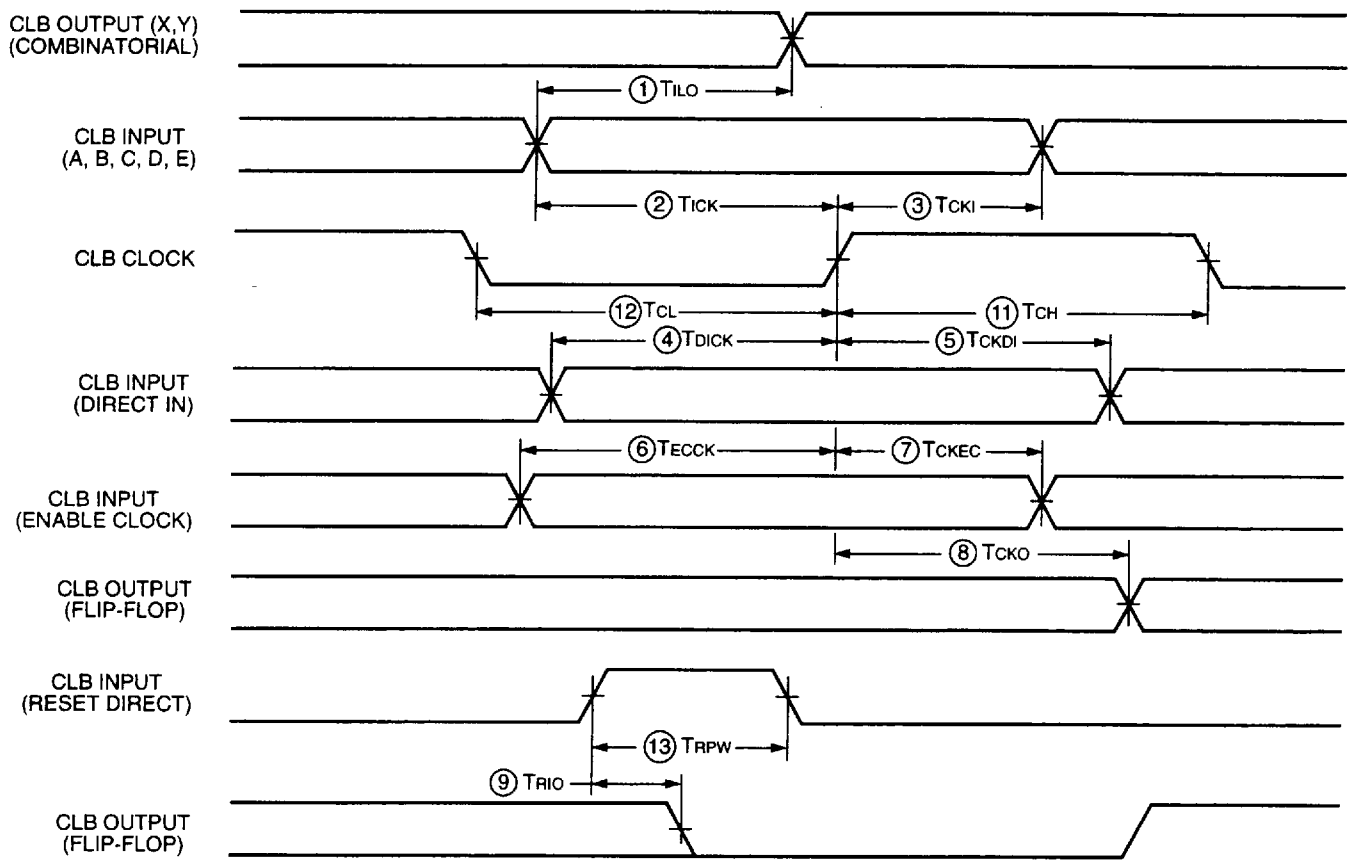



**Figure 34. CLB Switching Characteristics**

## Electrical Characteristics (continued)

### Table 20. CLB Switching Characteristics

Commercial: VCC = 5.0 V ± 5%; 0 °C ≤ TA ≤ 70 °C; Industrial: VCC = 5.0 ± 10%, –40 °C ≤ TA ≤ 85 °C;
Military: VCC = 5.0 V ± 10%, –55 °C ≤ TA ≤ 125 °C.

| Description | Symbol | | –50 | | –70 | | –100 | | –125 | | –150 | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| Combinatorial Delay | 1 | TILO | — | 14.0 | — | 9.0 | — | 7.0 | — | 5.5 | — | 4.6 | ns |
| Sequential Delay | | | | | | | | | | | | | |
| Clock K to Outputs x or y | 8 | TCKO | — | 12.0 | — | 6.0 | — | 5.0 | — | 4.5 | — | 4.0 | ns |
| Clock K to Outputs x or y when Q Returned Through Function Generators F or G to Drives x or y | — | TQLO | — | 23.0 | — | 13.0 | — | 10.0 | — | 8.0 | — | 6.7 | ns |
| Setup Time | | | | | | | | | | | | | |
| Logic Variables | 2 | TICK | 12.0 | — | 8.0 | — | 7.0 | — | 5.5 | — | 4.6 | — | ns |
| Data In | 4 | TDICK | 8.0 | — | 5.0 | — | 4.0 | — | 3.0 | — | 2.0 | — | ns |
| Enable Clock | 6 | TECCK | 10.0 | — | 7.0 | — | 5.0 | — | 4.5 | — | 4.0 | — | ns |
| Reset Direct Active | — | TRDCK | 1.0 | — | 1.0 | — | 1.0 | — | 1.0 | — | 1.0 | — | ns |
| Hold Time | | | | | | | | | | | | | |
| Logic Variables | 3 | TCKI | 1.0 | — | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| Data In | 5 | TCKDI | 6.0 | — | 4.0 | — | 2.0 | — | 1.5 | — | 1.2 | — | ns |
| Enable Clock | 7 | TCKEC | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| Clock | | | | | | | | | | | | | |
| High Time* | 11 | TCH | 9.0 | — | 5.0 | — | 4.0 | — | 3.0 | — | 2.5 | — | ns |
| Low Time* | 12 | TCL | 9.0 | — | 5.0 | — | 4.0 | — | 3.0 | — | 2.5 | — | ns |
| Flip-flop Toggle Rate* | — | FCLK | 50 | — | 70 | — | 100 | — | 125 | — | 150 | — | MHz |
| Reset Direct (rd) | | | | | | | | | | | | | |
| rd Width | 13 | TRPW | 12.0 | — | 8.0 | — | 7.0 | — | 6.0 | — | 5.0 | — | ns |
| Delay from rd to Outputs x, y | 9 | TRIO | — | 12.0 | — | 8.0 | — | 7.0 | — | 6.0 | — | 5.0 | ns |
| Master Reset (MR) | | | | | | | | | | | | | |
| MR Width | — | TMRW | 30 | — | 25 | — | 21 | — | 20 | — | 19 | — | ns |
| Delay from MR to Outputs x, y | — | TMRQ | — | 27 | — | 23 | — | 19 | — | 17 | — | 17 | ns |

* These parameters are for clock pulses within an FPGA device. For externally applied clock, increase values by 20%.

Notes: The CLKB K to Q output delay (TCKO—#8) of any CLB, plus the shortest possible interconnect delay, is always longer than the data in hold time requirement (TCKDI—#5) of any CLB on the same die.

## Electrical Characteristics (continued)

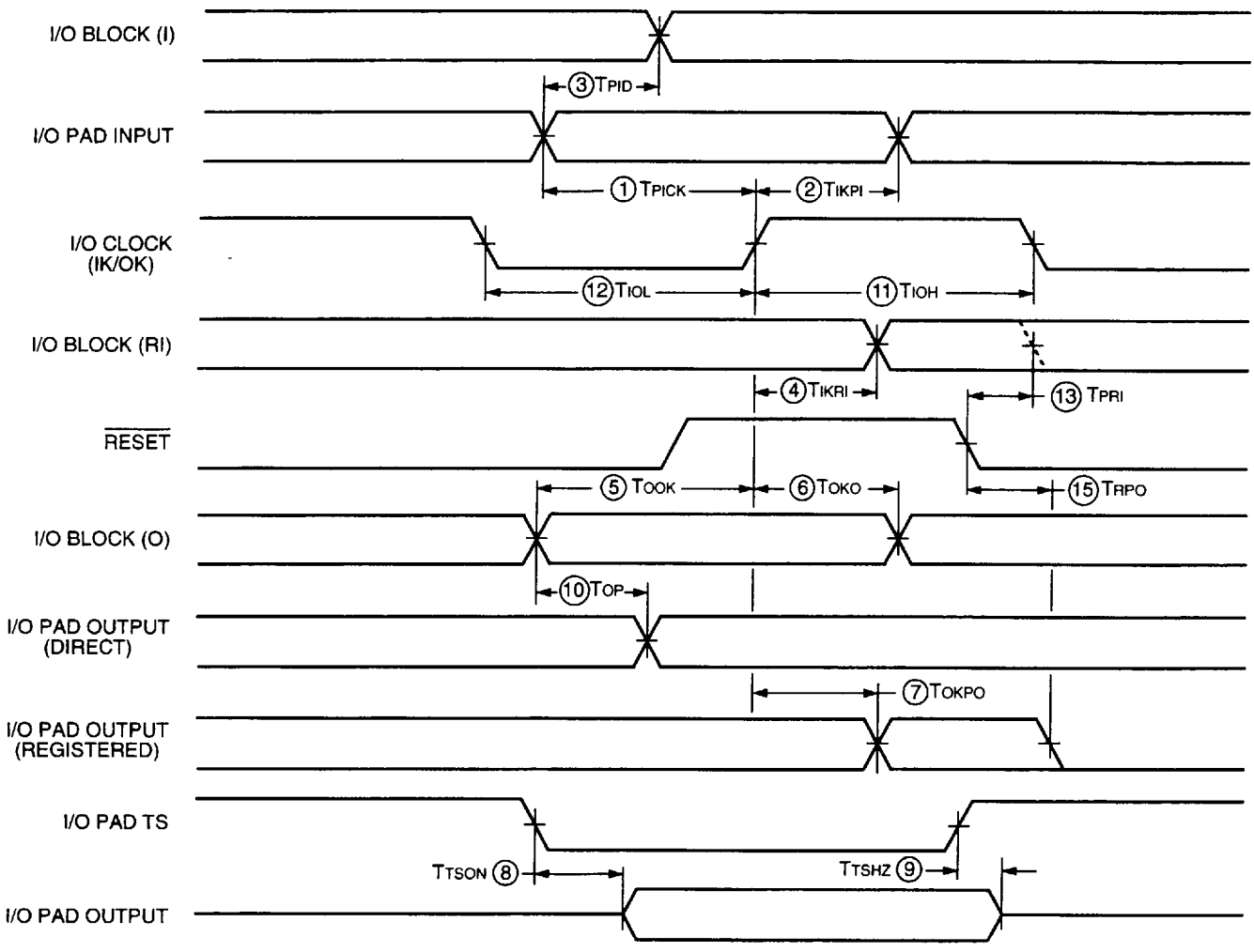



**Figure 35. IOB Switching Characteristics**

# Electrical Characteristics (continued)

## Table 21. IOB Switching Characteristics

Commercial: VCC = 5.0 V ± 5%; 0 °C ≤ TA ≤ 70 °C; Industrial: VCC = 5.0 ± 10%, –40 °C ≤ TA ≤ 85 °C;
Military: VCC = 5.0 V ± 10%, –55 °C ≤ TA ≤ 125 °C.

| Description | Symbol | | –50 | | –70 | | –100 | | –125 | | –150 | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| Input Delays | | | | | | | | | | | | | |
| Pad to Direct In | 3 | TPID | — | 9.0 | — | 6.0 | — | 4.0 | — | 3.0 | — | 2.8 | ns |
| Pad to Registered In | — | TPTG | — | 34.0 | — | 21.0 | — | 17.0 | — | 16.0 | — | 15.0 | ns |
| Clock to Registered In | 4 | TIKRI | — | 11.0 | — | 5.5 | — | 4.0 | — | 3.0 | — | 2.8 | ns |
| Setup Time (Input): | | | | | | | | | | | | | |
| Clock Setup Time | 1 | TPICK | 30.0 | — | 20.0 | — | 17.0 | — | 16.0 | — | 14.5 | — | ns |
| Output Delays | | | | | | | | | | | | | |
| Clock to Pad | | | | | | | | | | | | | |
| Fast | 7 | TOKPO | — | 18.0 | — | 13.0 | — | 10.0 | — | 9.0 | — | 7.0 | ns |
| Slew-rate Limited | 7 | TOKPO | — | 43.0 | — | 33.0 | — | 27.0 | — | 24.0 | — | 22.0 | ns |
| Output to Pad | | | | | | | | | | | | | |
| Fast | 10 | TOPF | — | 15.0 | — | 9.0 | — | 6.0 | — | 5.0 | — | 4.5 | ns |
| Slew-rate Limited | 10 | TOPS | — | 40.0 | — | 29.0 | — | 23.0 | — | 20.0 | — | 15.0 | ns |
| 3-state to Pad Hi-Z | | | | | | | | | | | | | |
| Fast | 9 | TTSHZ | — | 10.0 | — | 8.0 | — | 8.0 | — | 7.0 | — | 7.0 | ns |
| Slew-rate Limited | 9 | TTSHZ | — | 37.0 | — | 28.0 | — | 25.0 | — | 24.0 | — | 22.0 | ns |
| 3-state to Pad Valid | | | | | | | | | | | | | |
| Fast | 8 | TTSON | — | 20.0 | — | 14.0 | — | 12.0 | — | 11.0 | — | 11.0 | ns |
| Slew-rate Limited | 8 | TTSON | — | 45.0 | — | 34.0 | — | 29.0 | — | 27.0 | — | 26.0 | ns |
| Setup and Hold Times (Output) | | | | | | | | | | | | | |
| Clock Setup Time | 5 | TOCK | 15.0 | — | 10.0 | — | 9.0 | — | 8.0 | — | 7.0 | — | ns |
| Clock Hold Time | 6 | TOKO | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| Clock | | | | | | | | | | | | | |
| High Time* | 11 | TCH | 9.0 | — | 5.0 | — | 4.0 | — | 3.0 | — | 2.5 | — | ns |
| Low Time* | 12 | TCL | 9.0 | — | 5.0 | — | 4.0 | — | 3.0 | — | 2.5 | — | ns |
| Max. Flip-flop Toggle* | — | FCLK | — | 50 | — | 70 | — | 100 | — | 125 | — | 150 | MHz |
| Master Reset Delays | | | | | | | | | | | | | |
| $\overline{\text{RESET}}$ to: | | | | | | | | | | | | | |
| Registered In | 13 | TRRI | — | 35 | — | 25 | — | 24 | — | 23 | — | 20 | ns |
| Output Pad (Fast) | 15 | TRPO | — | 50 | — | 35 | — | 33 | — | 29 | — | 25 | ns |
| Output Pad (Slew-rate Limited) | 15 | TRPO | — | 68 | — | 53 | — | 45 | — | 42 | — | 40 | ns |

* These parameters are for clock pulses within an FPGA device. For externally applied clock, increase values by 20%.

Notes:

Timing is measured at pin threshold with 50 pF external capacitive loads (including test fixture).

Typical fast mode output rise/fall times are 2 ns and will increase approximately 2%/pF of additional load.

Typical slew-rate limited output rise/fall times are approximately 4 times longer.

A maximum total external capacitive load for simultaneous fast mode switching in the same direction is 200 pF per power/ground pin pair. For slew-rate limited outputs, this total is 4 times larger. Exceeding this maximum capacitive load can result in ground bounce of >1.5 V amplitude and <5 ns duration, which may cause problems when the $\overline{\text{LCA}}$ drives clocks and other asynchronous signals.

Voltage levels of unused (bonded and unbonded) pads must be valid logic levels. Each can be configured with the internal pull-up resistor or alternatively configured as a driven output or driven from an external source.

Input pad setup time is specified with respect to the internal clock (ik).

To calculate system setup time, subtract clock delay (pad to ik) from the input pad setup time value. Input pad hold time with respect to the internal clock (ik) is negative. This means that pad levels changed immediately before the internal clock edge (ik) will not be recognized.

## Electrical Characteristics (continued)

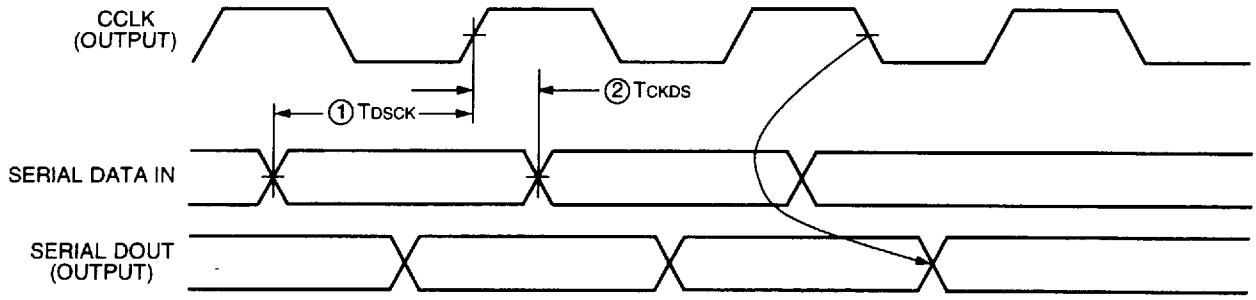



**Figure 36. Master Serial Mode Switching Characteristics**

**Table 22. Master Serial Mode Switching Characteristics**

| Signal | Description | Symbol | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| CCLK | Data-In Setup | 1 | TDSCK | 60 | — | ns |
| | Data-In Hold | 2 | TCKDS | 0 | — | ns |

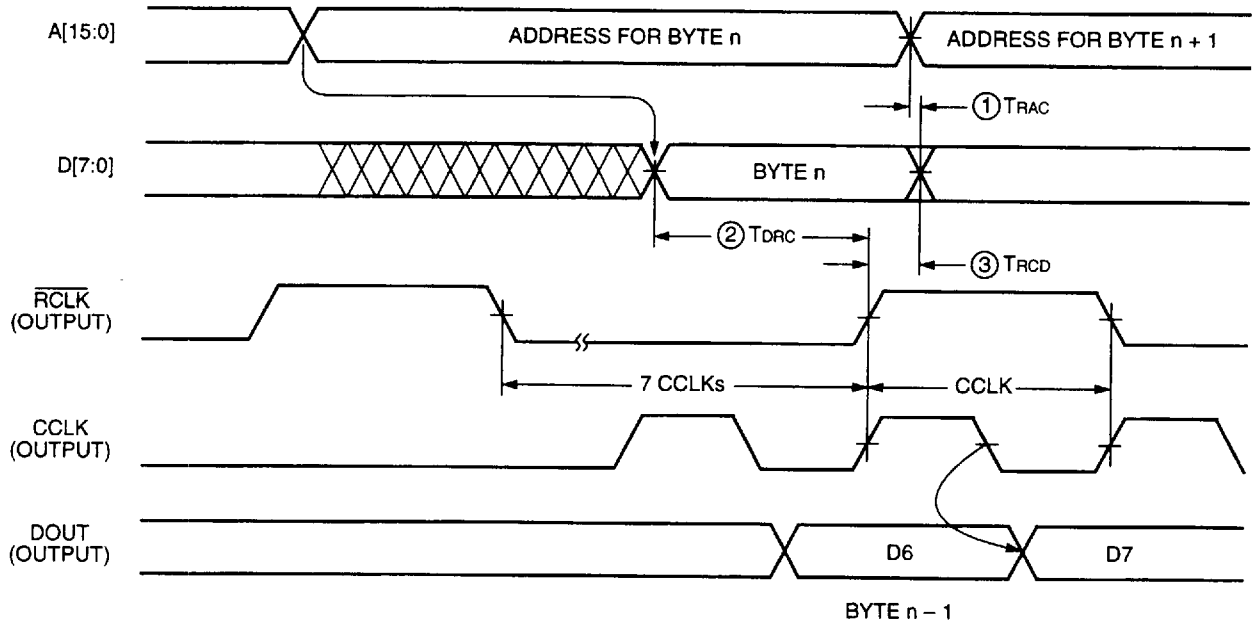
Notes:

At powerup, VCC must rise from 2.0 V to VCC minimum in less than 25 ms. If this is not possible, configuration can be delayed by holding RESET low until VCC has reached 4.0 V. A very long VCC rise time of >100 ms, or a nonmonotonically rising VCC may require a >1 µs high level on RESET, followed by >6 µs low level on RESET and D/P after VCC has reached 4.0 V.

Configuration can be controlled by holding RESET low with or until after the INIT of all daisy-chain slave mode devices is high.

Master serial mode timing is based on slave mode testing.

## Electrical Characteristics (continued)




Note: The EPROM requirements in this timing diagram are extremely relaxed; EPROM access time can be longer than 4000 ns. EPROM data output has no hold time requirements.

**Figure 37. Master Parallel Mode Switching Characteristics**

**Table 23. Master Parallel Mode Switching Characteristics**

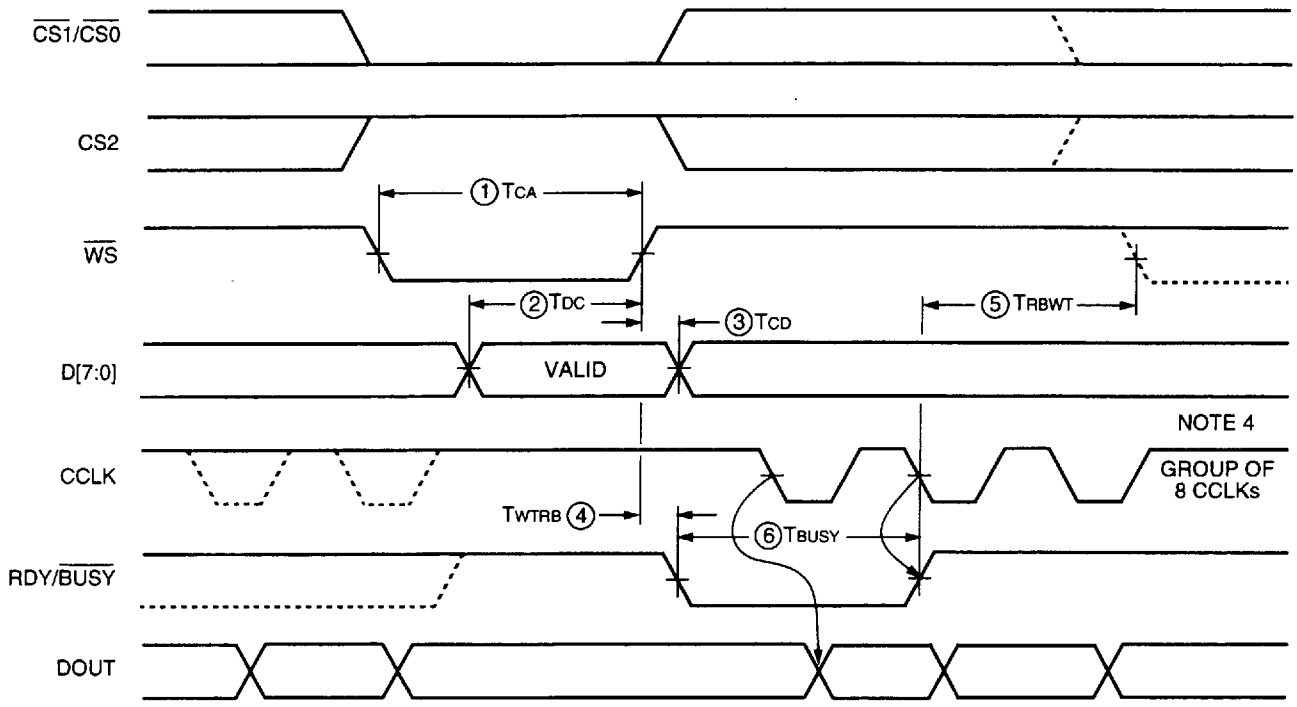
| Signal | Description | Symbol | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| RCLK | To Address Valid | 1 | TRAC | 0 | 200 | ns |
| | To Data Setup | 2 | TDRC | 60 | — | ns |
| | To Data Hold | 3 | TRCD | 0 | — | ns |
| | RCLK High | — | TRCH | 600 | — | ns |
| | RCLK Low | — | TRCL | 4.0 | — | µs |

Notes:

At powerup, VCC must rise from 2.0 V to VCC minimum in less than 25 ms. If this is not possible, configuration can be delayed by holding RESET low until VCC has reached 4.0 V. A very long VCC rise time of >100 ms, or a non-monotonically rising VCC may require a >1 µs high level on RESET, followed by >6 µs low level on RESET and D/P after VCC has reached 4.0 V.

Configuration can be controlled by holding RESET low with or until after the INIT of all daisy-chain slave mode devices is high.

## Electrical Characteristics (continued)




Note: The requirements in this timing diagram are extremely relaxed; data need not be held beyond the rising edge of WS. BUSY will go active within 60 ns after the end of WS. BUSY will stay active for several microseconds. WS may be asserted immediately after the end of BUSY.

**Figure 38. Peripheral Mode Switching Characteristics**

**Table 24. Peripheral Mode Programming Switching Characteristics**

| Signal | Description | Symbol | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| Write Signal | Effective Write Time Required ($\overline{CS0}$ x $\overline{CS1}$ x CS2 x $\overline{WS}$) | 1 | TCA | 100 | — | ns |
| D[7:0] | DIN Setup Time Required | 2 | TDC | 60 | — | ns |
| | DIN Hold TIme Required | 3 | TCD | 0 | — | ns |
| RDY/BUSY | RDY/BUSY Delay after End of WS | 4 | TWTRB | — | — | ns |
| | Earliest Next WS after End of BUSY | 5 | TRBWT | 0 | 60 | ns |
| | BUSY Low Time Generated | 6 | TBUSY | 2 | 9 | CCLK Periods |

Notes:

At powerup, VCC must rise from 2.0 V to VCC minimum in less than 25 ms. If this is not possible, configuration can be delayed by holding RESET low until VCC has reached 4.0 V. A very long VCC rise time of >100 ms, or a nonmonotonically rising VCC may require a >1 µs high level on RESET, followed by >6 µs low level on RESET and D/P after VCC has reached 4.0 V.

Configuration must be delayed until the INIT of all LCAs is high.

Time from end of WS to CCLK cycle for the new byte of data depends on completion of previous byte processing and the phase of the internal timing generator for CCLK.

CCLK and DOUT timing is tested in slave mode.

## Electrical Characteristics (continued)

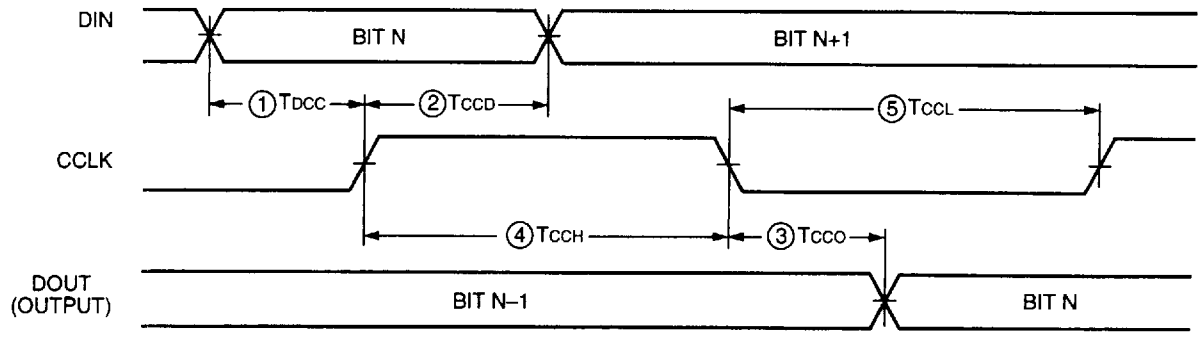



**Figure 39. Slave Mode Switching Characteristics**

### Table 25. Slave Mode Switching Characteristics

Commercial: $V_{CC}$ = 5.0 V ± 5%; 0 °C ≤ $T_A$ ≤ 70 °C; Industrial: $V_{CC}$ = 5.0 ± 10%, –40 °C ≤ $T_A$ ≤ 85 °C;
Military: $V_{CC}$ = 5.0 V ± 10%, –55 °C ≤ $T_A$ ≤ 125 °C.

| Signal | Description | Symbol | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| CCLK | To DOUT | 3 | $T_{CCO}$ | — | 100 | ns |
| | DIN Setup | 1 | $T_{DCC}$ | 60 | — | ns |
| | DIN Hold | 2 | $T_{CCD}$ | 0 | — | ns |
| | HIGH Time | 4 | $T_{CCH}$ | 0.05 | — | µs |
| | LOW Time | 5 | $T_{CCL}$ | 0.05 | 5.0 | µs |
| | Frequency | — | $F_{CC}$ | — | 10.0 | MHz |

Notes:

The maximum limit of CCLK LOW time is caused by dynamic circuitry inside the LCA device.

Configuration must be delayed until the $\overline{INIT}$ of all LCAs is high.

At powerup, $V_{CC}$ must rise from 2.0 V to $V_{CC}$ minimum in less than 25 ms. If this is not possible, configuration can be delayed by holding $\overline{RESET}$ low until $V_{CC}$ has reached 4.0 V. A very long $V_{CC}$ rise time of >100 ms, or a nonmonotonically rising $V_{CC}$, may require a >1 µs high level on $\overline{RESET}$, followed by >6 µs low level on $\overline{RESET}$ and D/$\overline{P}$ after $V_{CC}$ has reached 4.0 V.

## Electrical Characteristics (continued)

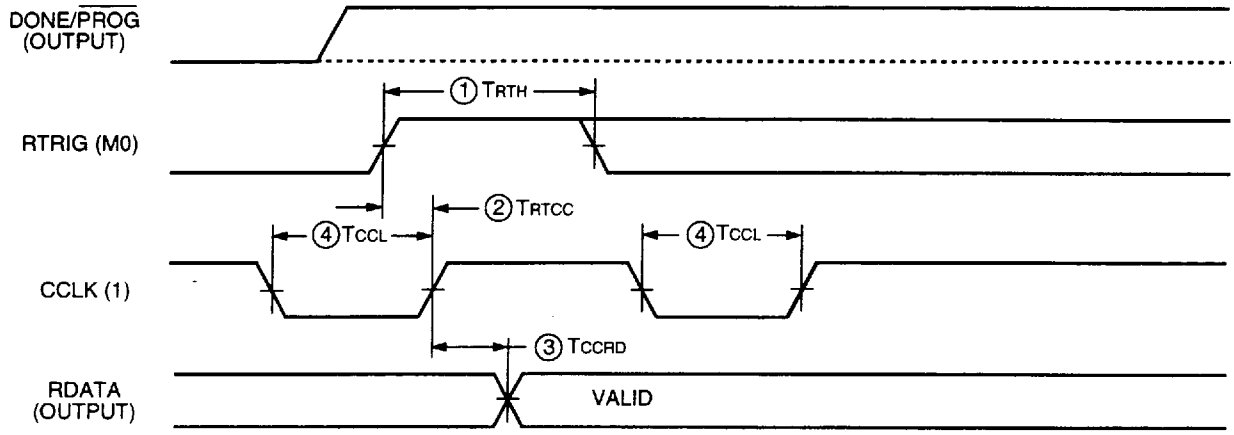



**Figure 40. Program Readback Switching Characteristics**

### Table 26. Program Readback Switching Characteristics

Commercial: $V_{CC}$ = 5.0 V ± 5%; 0 °C ≤ $T_A$ ≤ 70 °C; Industrial: $V_{CC}$ = 5.0 ± 10%, –40 °C ≤ $T_A$ ≤ 85 °C;
Military: $V_{CC}$ = 5.0 V ± 10%, –55 °C ≤ $T_A$ ≤ 125 °C.

| Signal | Description | Symbol | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| RTRIG | RTRIG HIGH | 1 | TRTH | 250 | — | ns |
| CCLK | RTRIG Setup | 2 | TRTCC | 200 | — | ns |
| | $\overline{\text{RDATA}}$ Delay | 3 | TCCRD | — | 100 | ns |
| | HIGH Time | 5 | TCCH | 0.05 | — | µs |
| | LOW Time | 4 | TCCL | 0.05 | 5.0 | µs |

Notes:

During readback, CCLK frequency may not exceed 1 MHz.

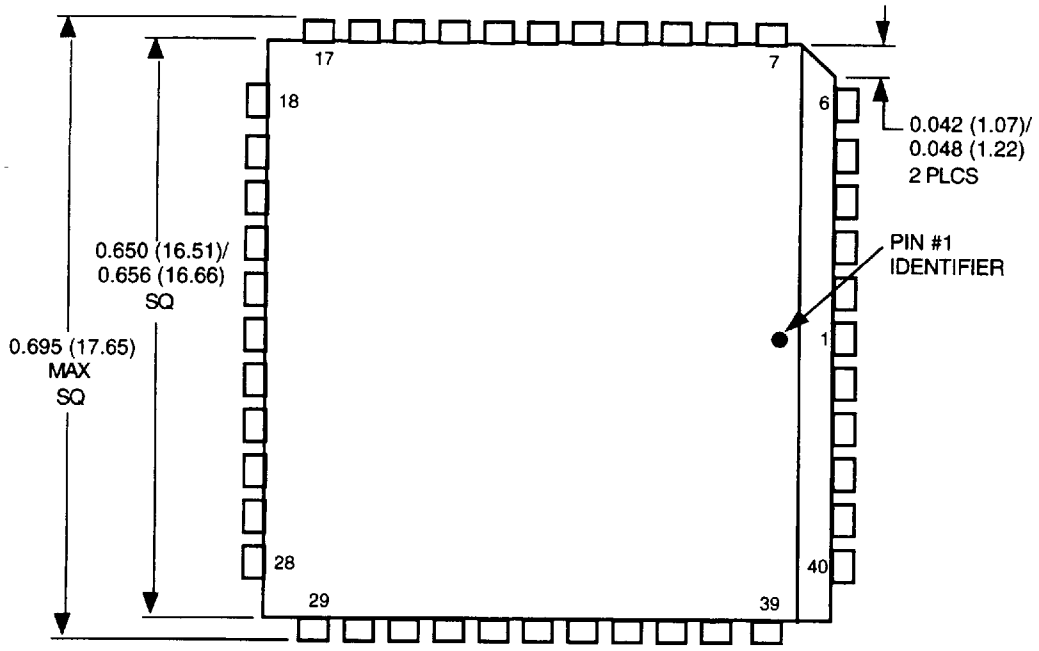
RTRIG (M0 positive transition) must not be done until after one clock following active I/O pins.

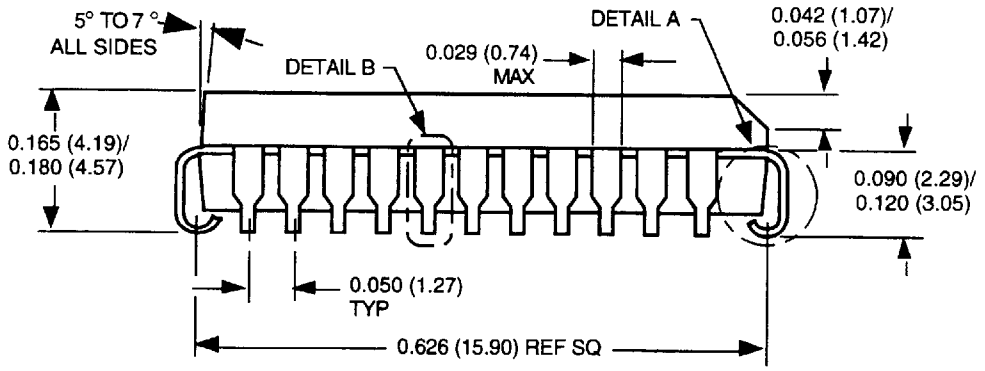
Readback should not be initiated until after configuration is complete.

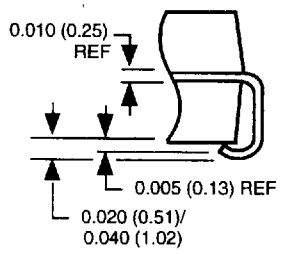
## Outline Diagrams

Dimensions are in inches and (millimeters).

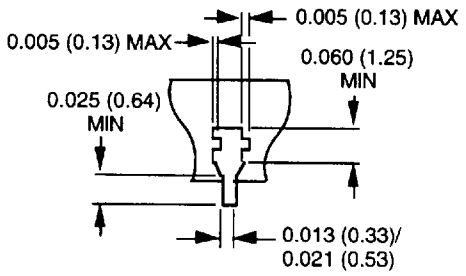
### 44-Pin PLCC Package



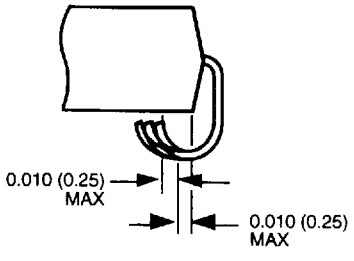




DETAIL A




DETAIL B

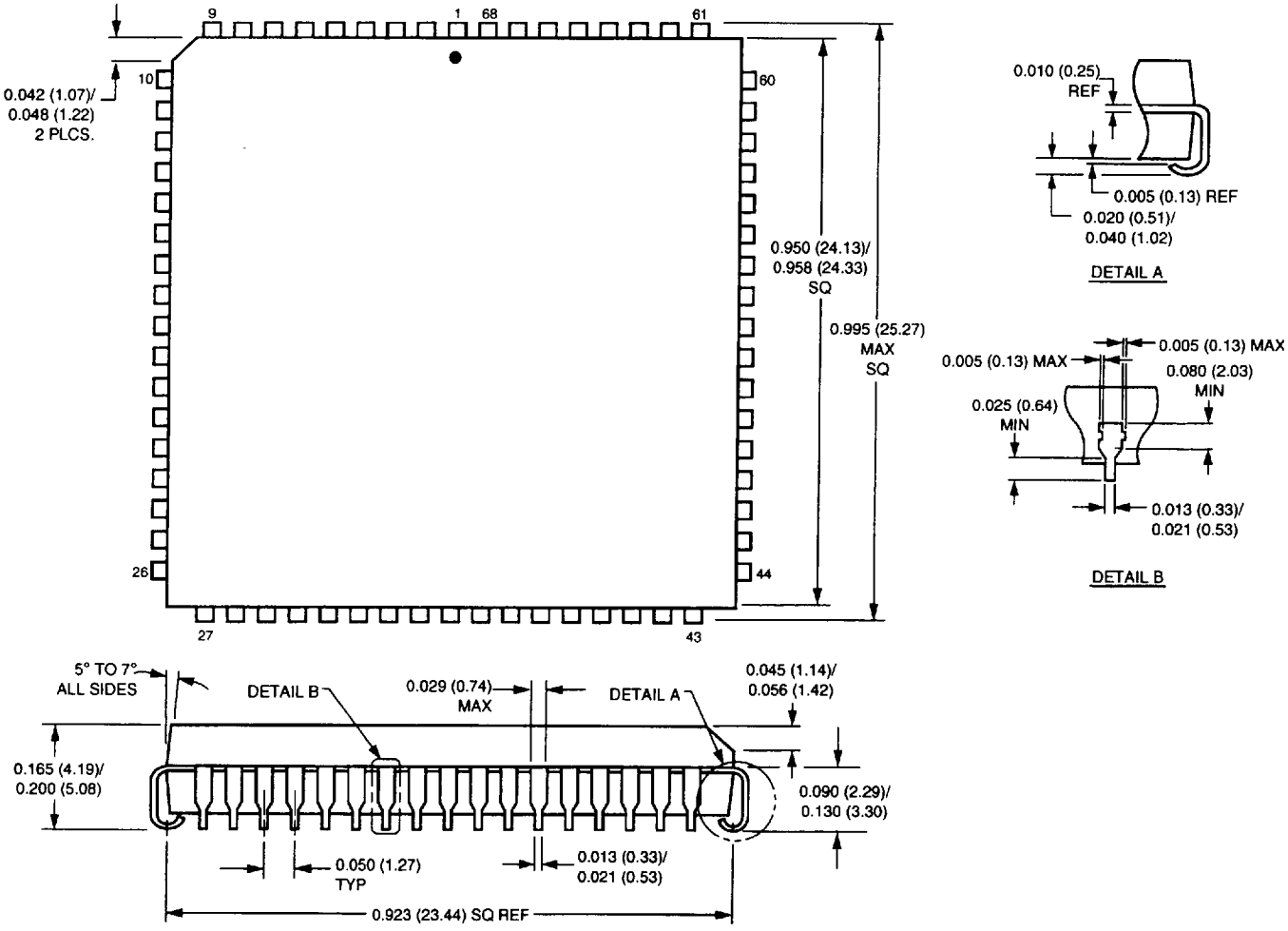



ALLOWABLE LEAD
POSITION SHIFT DETAIL

## Outline Diagrams (continued)

Dimensions are in inches and (millimeters).

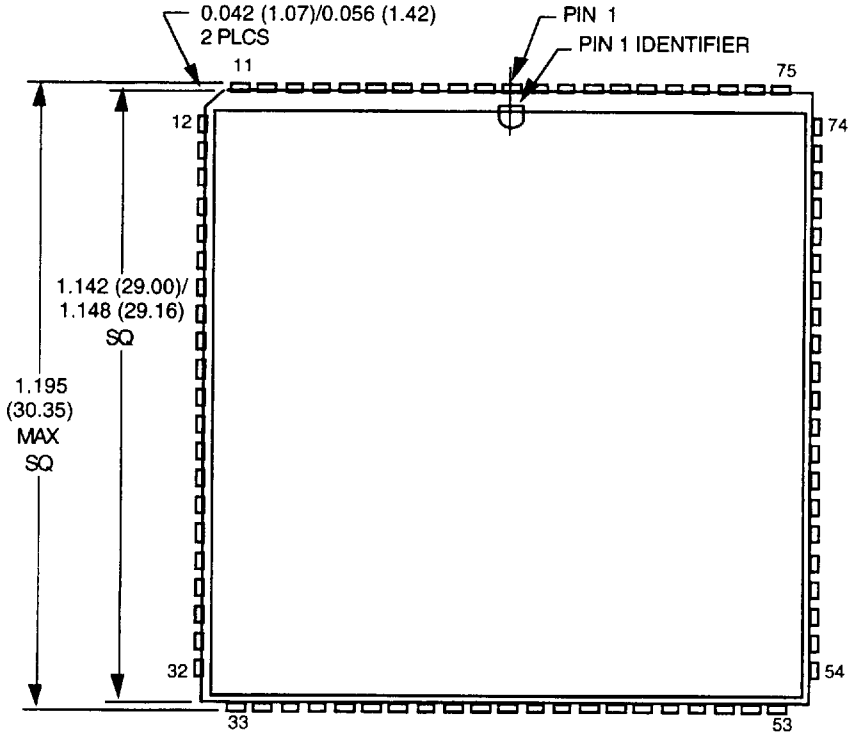
### 68-Pin PLCC Package

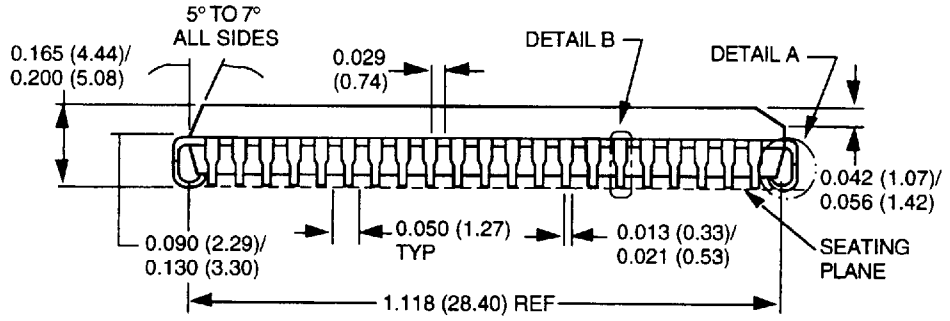


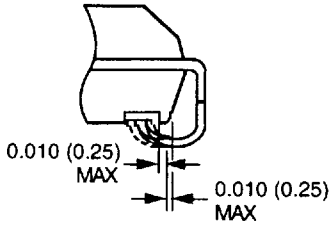
## Outline Diagrams (continued)

Dimensions are in inches and (millimeters).

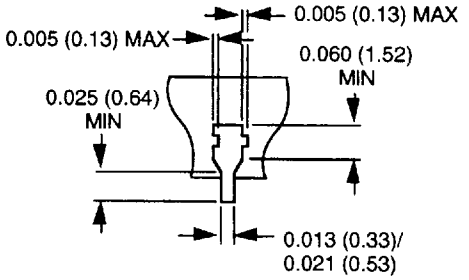
### 84-Pin PLCC Package




ALLOWABLE LEAD
POSITION SHIFT DETAIL

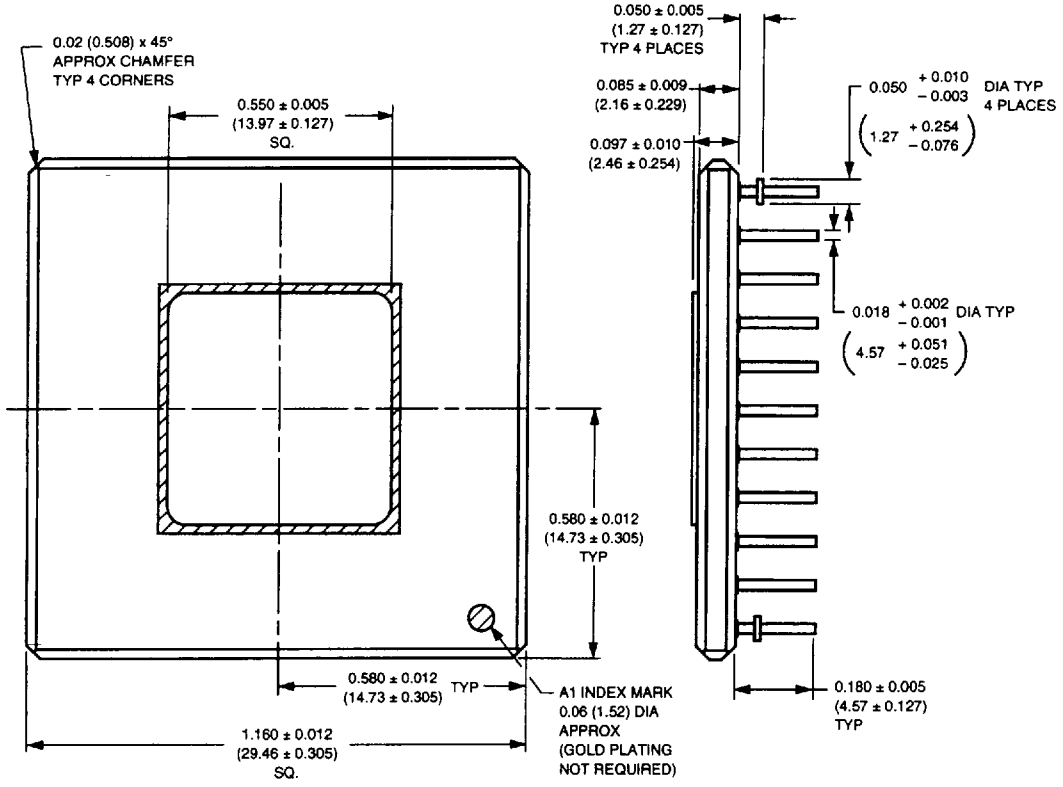


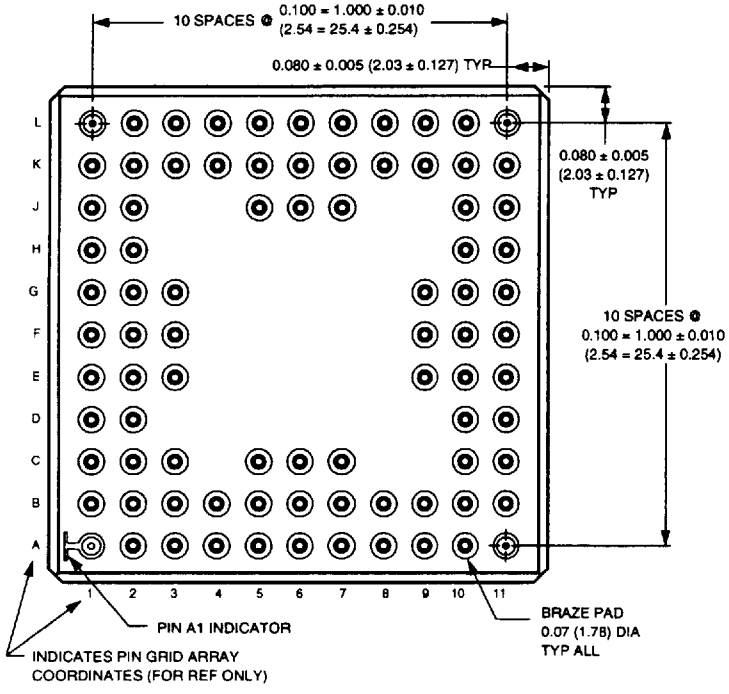

DETAIL B

## Outline Diagrams (continued)

Dimensions are in inches and (millimeters).

### 84-Pin Ceramic PGA Package

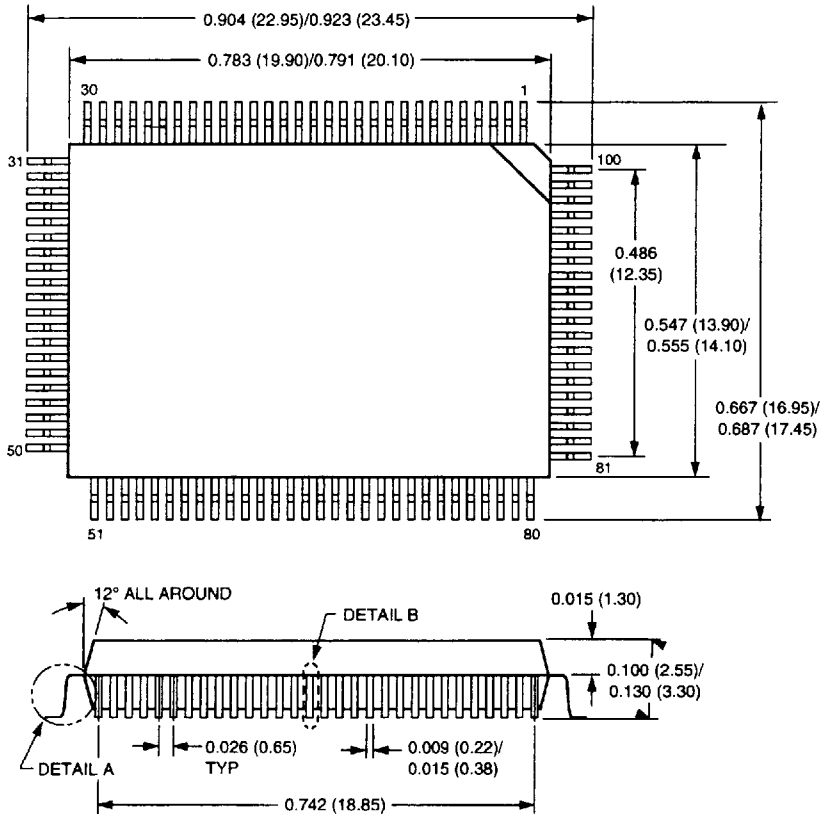


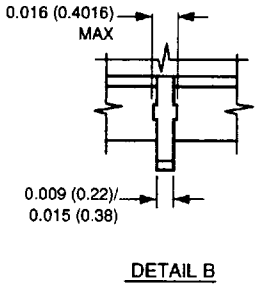



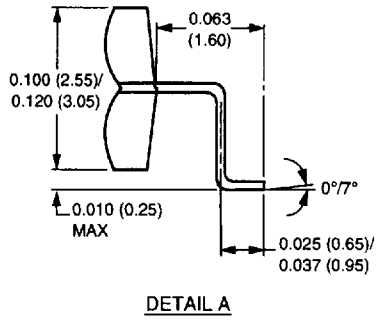
## Outline Diagrams (continued)

Dimensions are in inches and (millimeters).

### 100-Pin EIAJ QFP Package



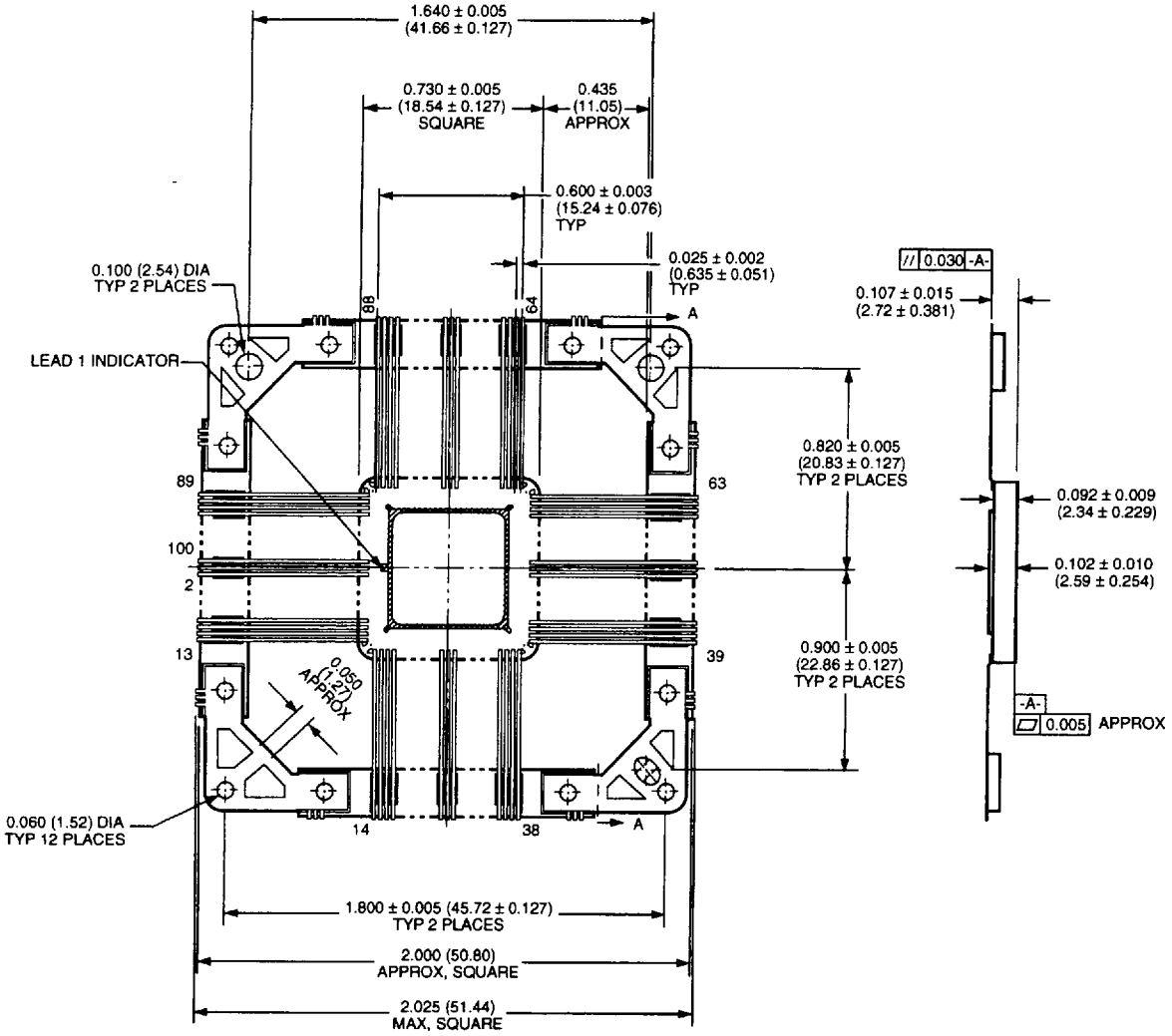



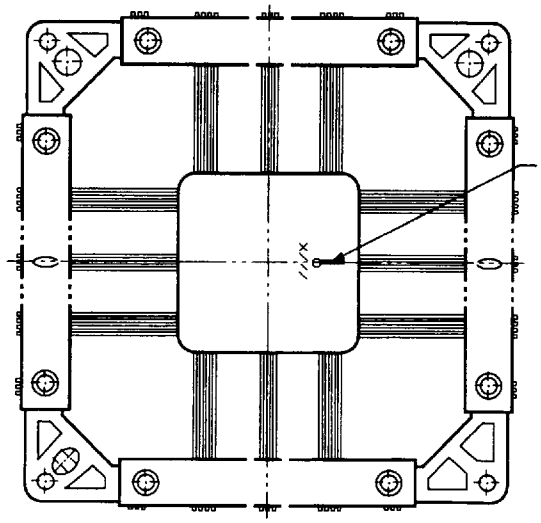



## Outline Diagrams (continued)

Dimensions are in inches and (millimeters).

### 100-Pin CQFP Package

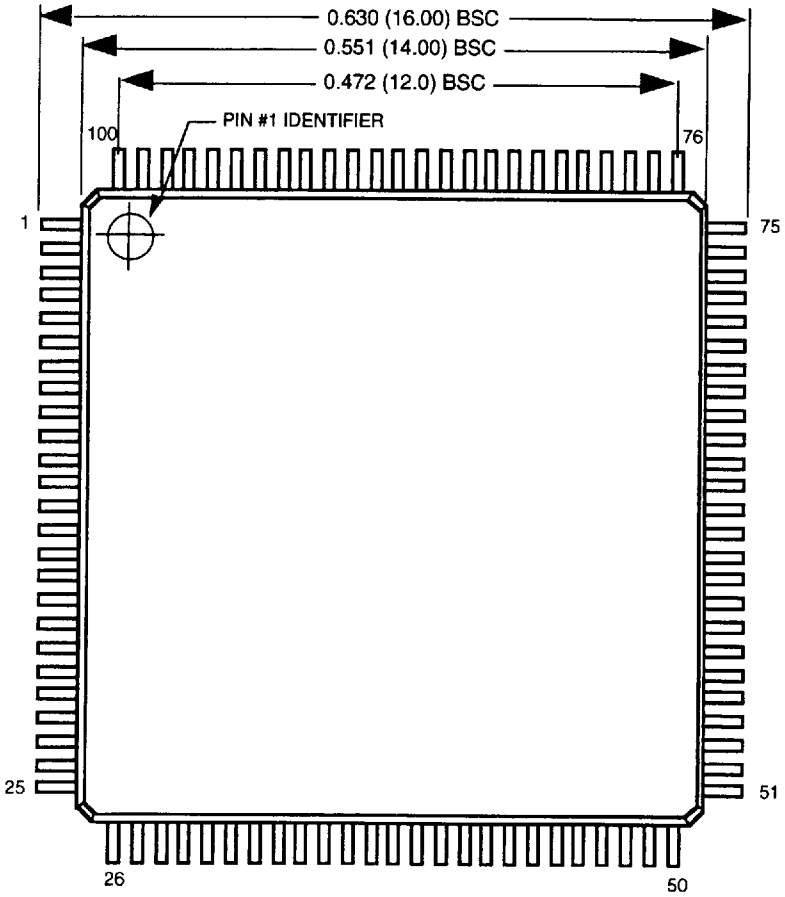


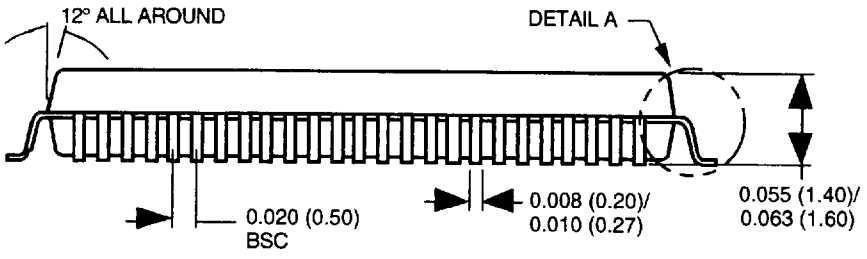



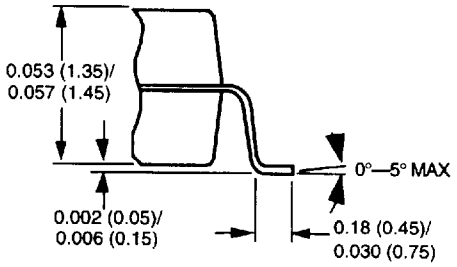
## Outline Diagrams (continued)

Dimensions are in inches and (millimeters).

### 100-Pin TQFP Package



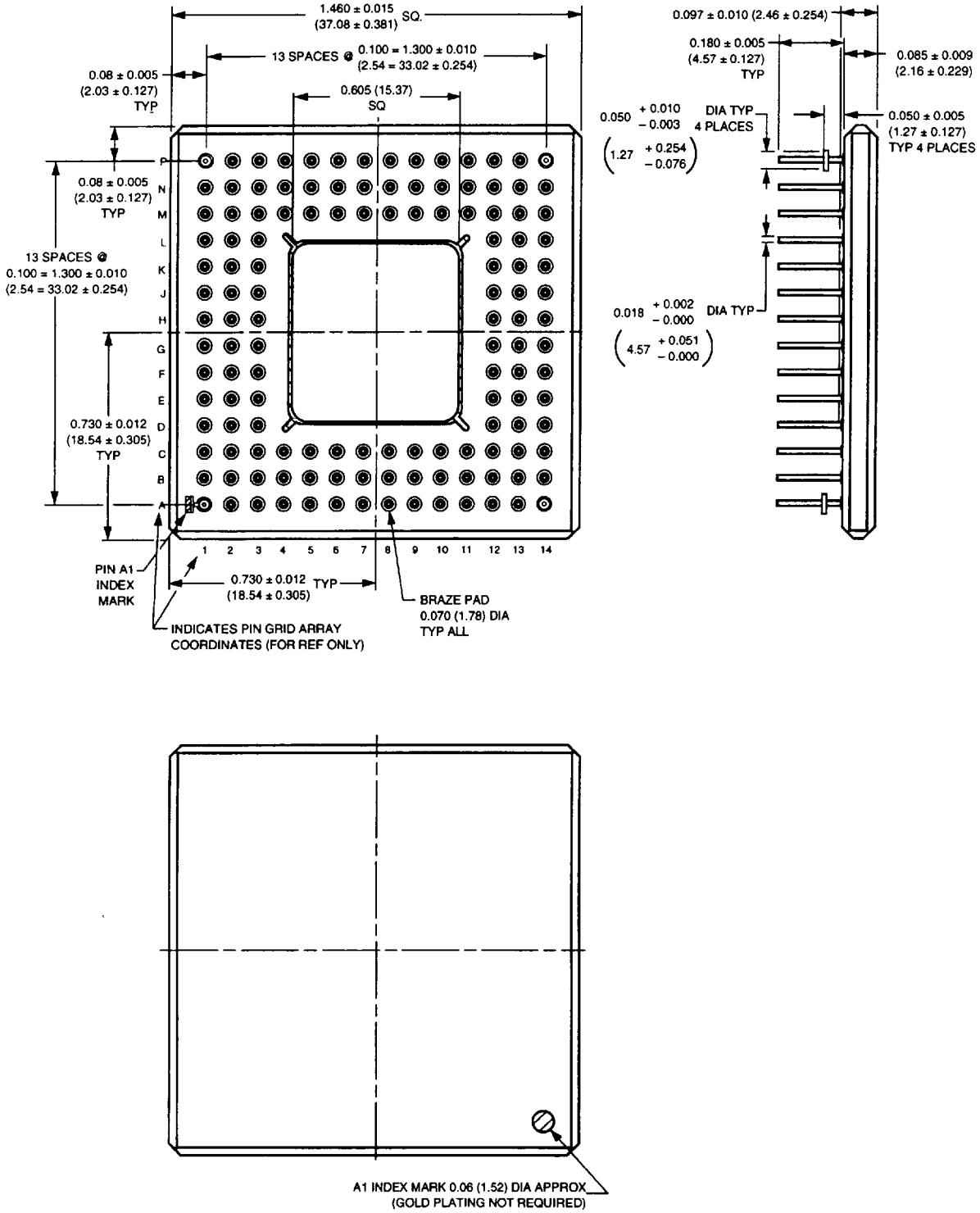




DETAIL A

## Outline Diagrams (continued)

Dimensions are in inches and (millimeters).

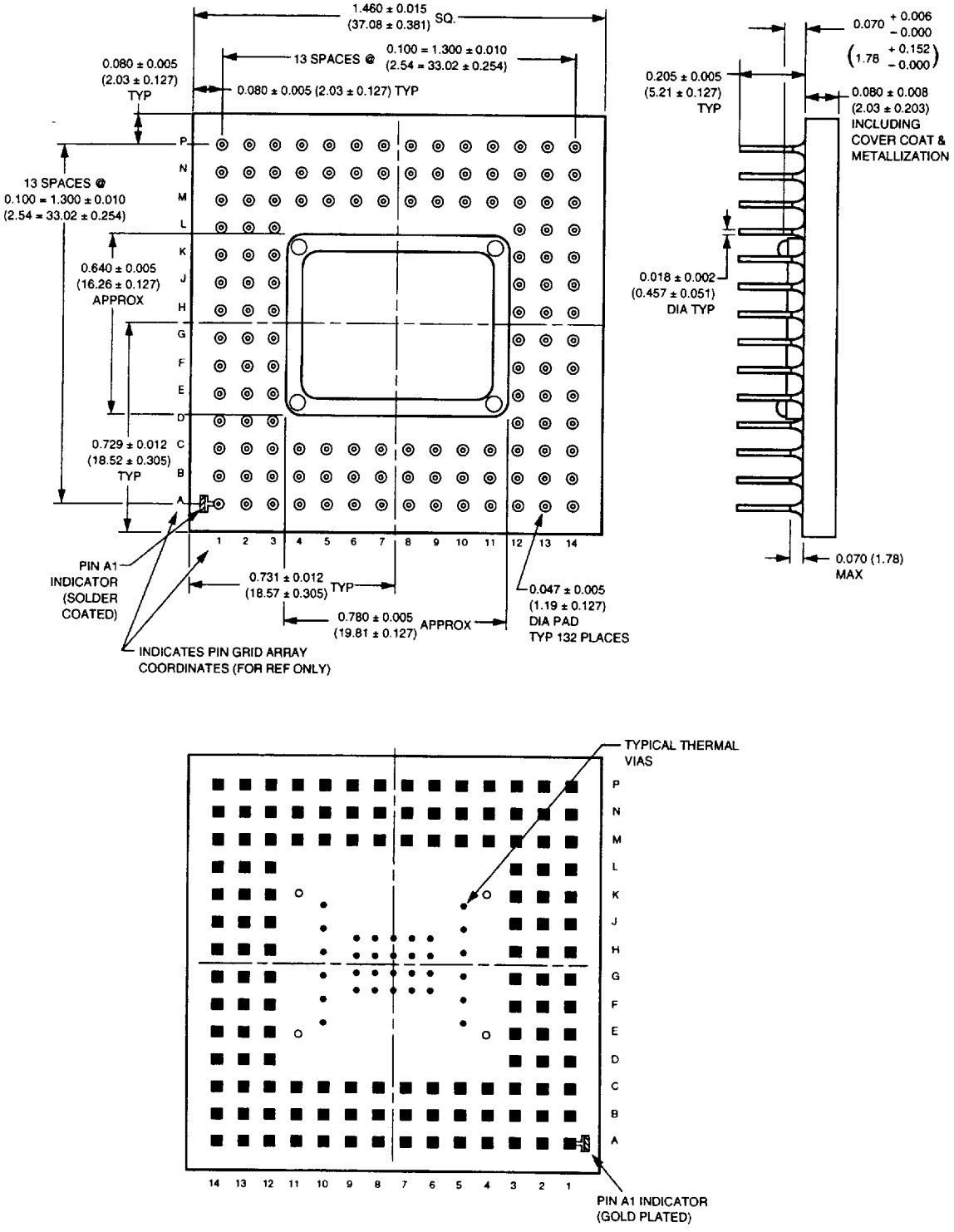
### 132-Pin Ceramic PGA Package



## Outline Diagrams (continued)

Dimensions are in inches and (millimeters).

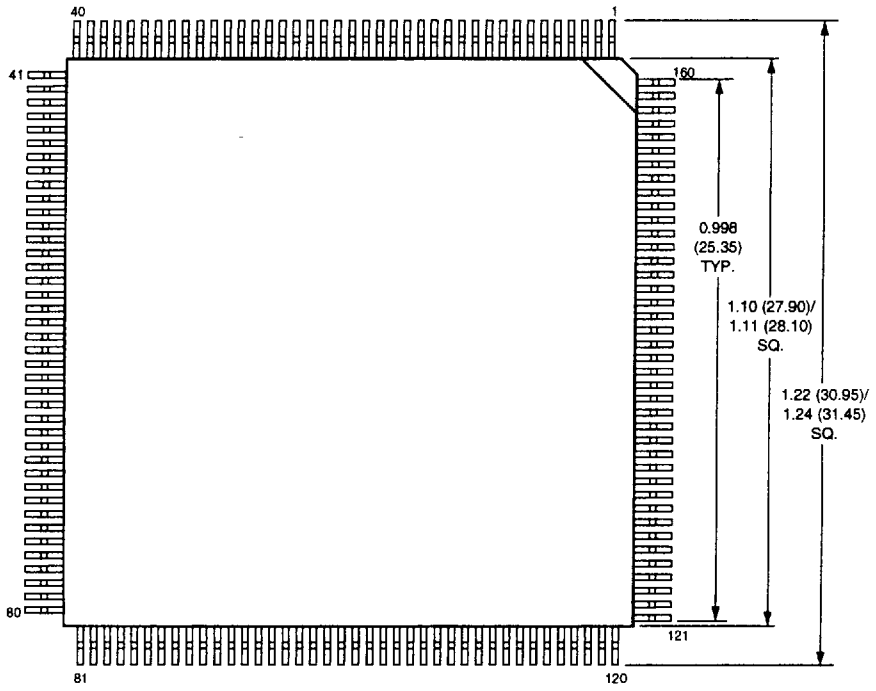
### 132-Pin PGA Package

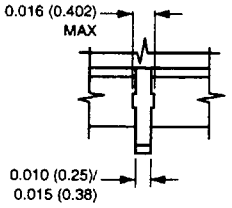


## Outline Diagrams (continued)

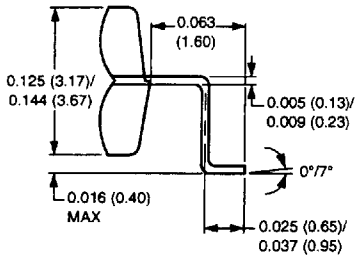
Dimensions are in inches and (millimeters).

### 160-Pin EIAJ QFP Package

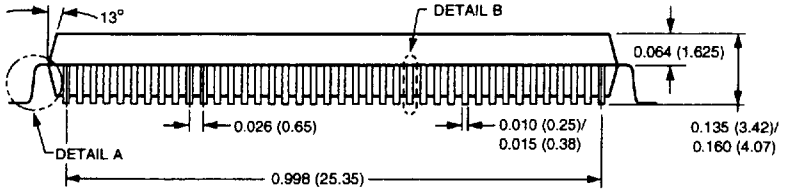



DETAIL B



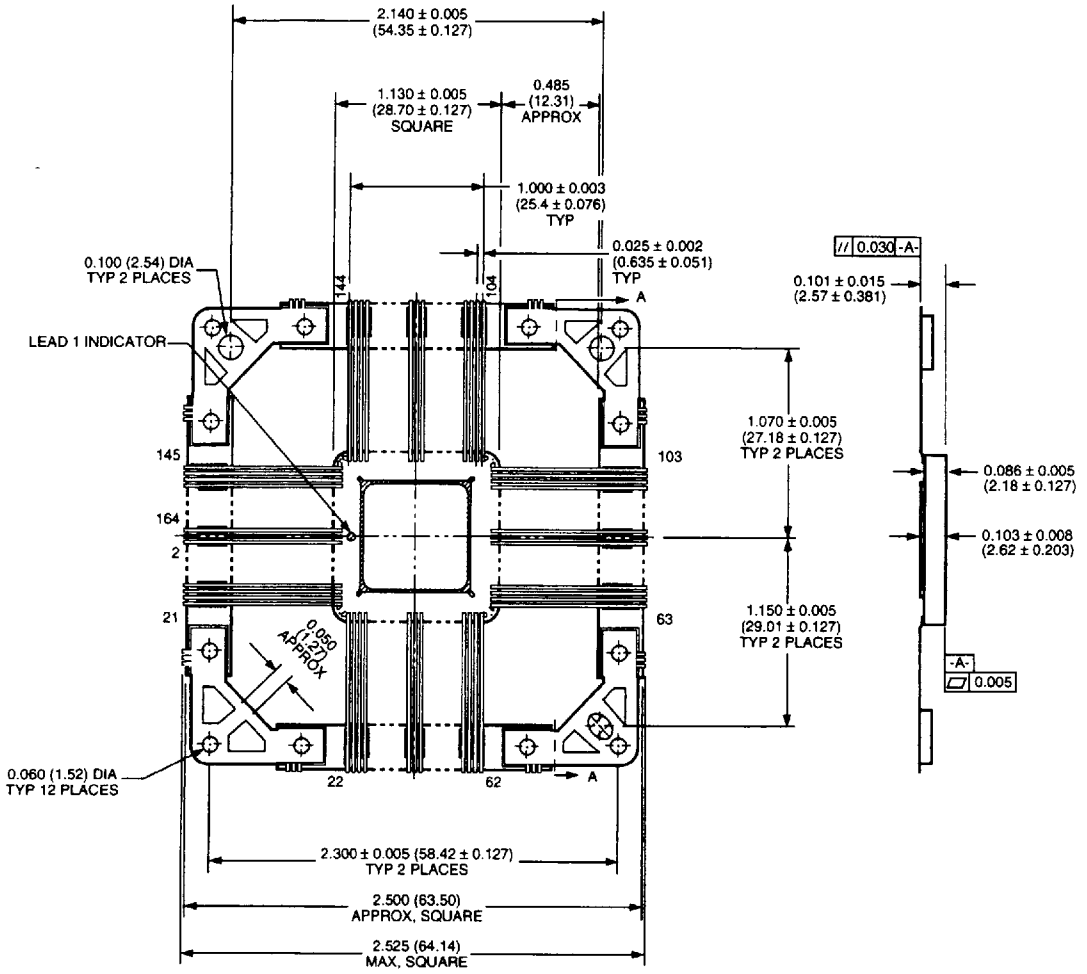

DETAIL A

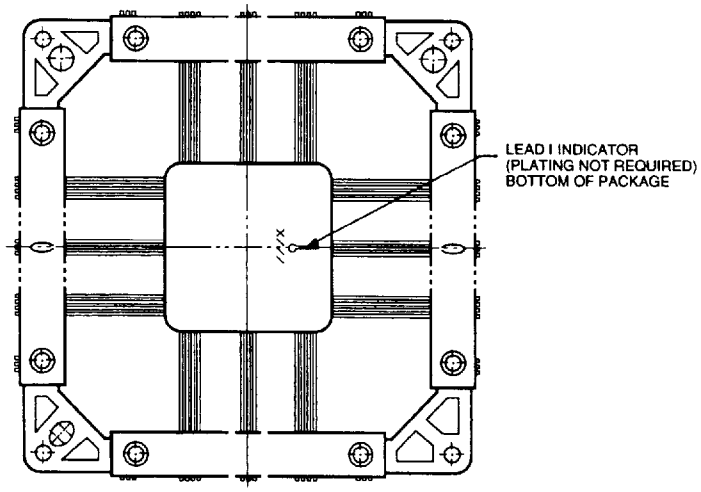


## Outline Diagrams (continued)

Dimensions are in inches and (millimeters).

### 164-Pin Ceramic QFP Package



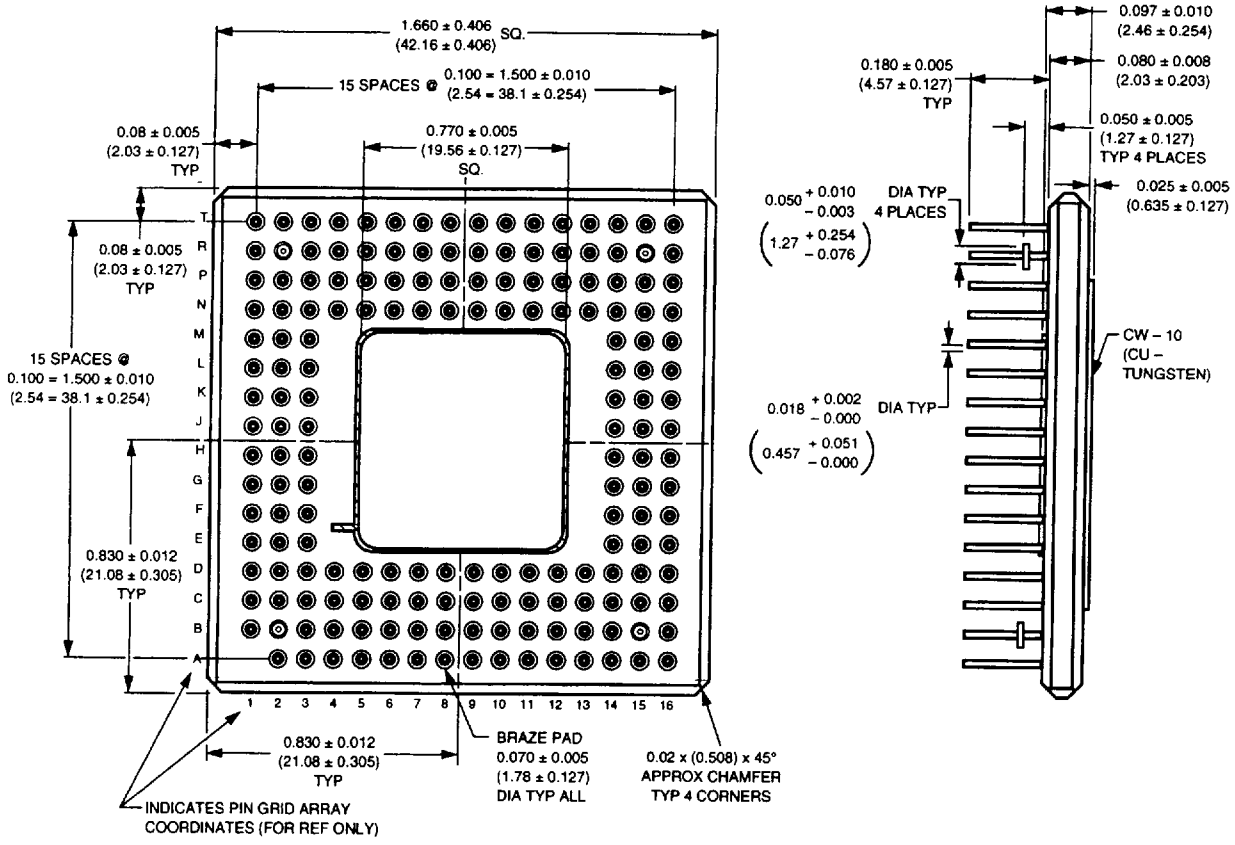



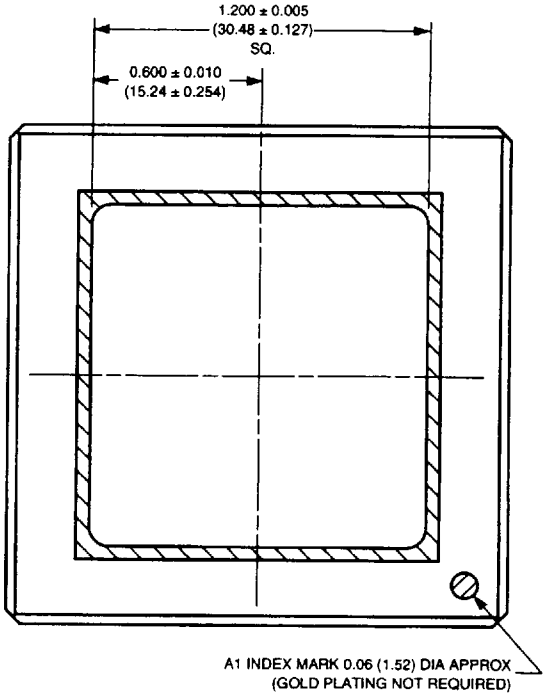

BOTTOM VIEW

## Outline Diagrams (continued)

Dimensions are in inches and (millimeters).

### 175-Pin Ceramic PGA Package

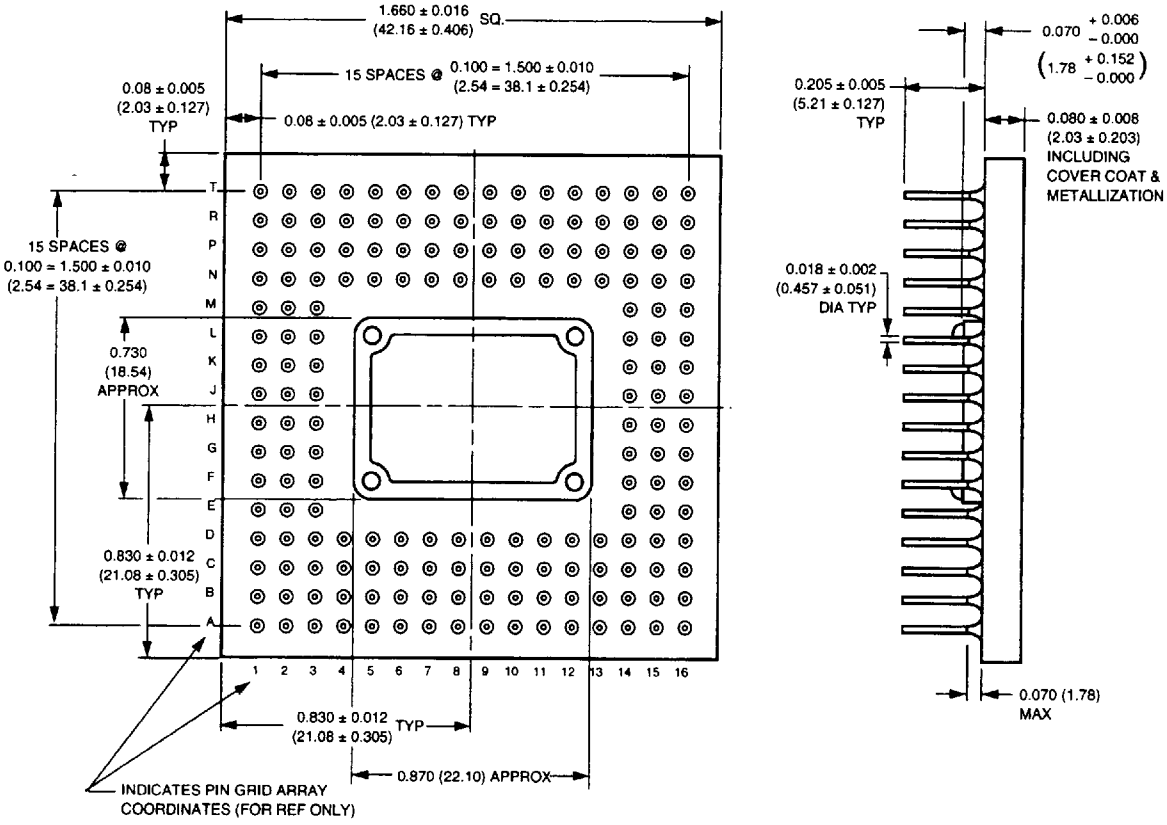


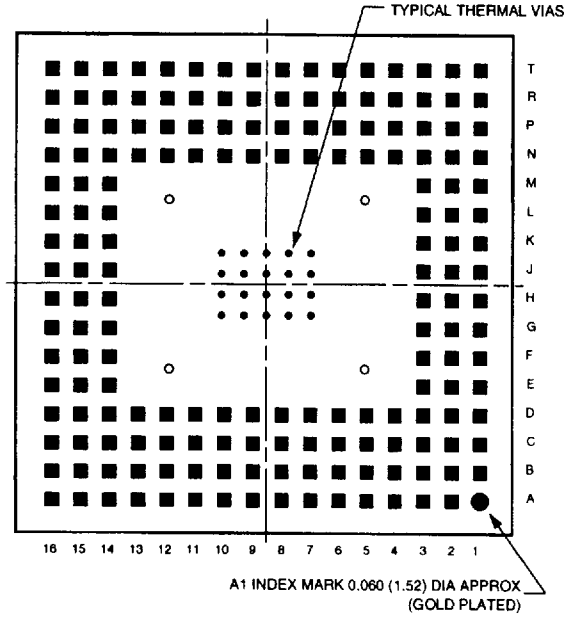



## Outline Diagrams (continued)

Dimensions are in inches and (millimeters).

### 175-Pin PGA Package

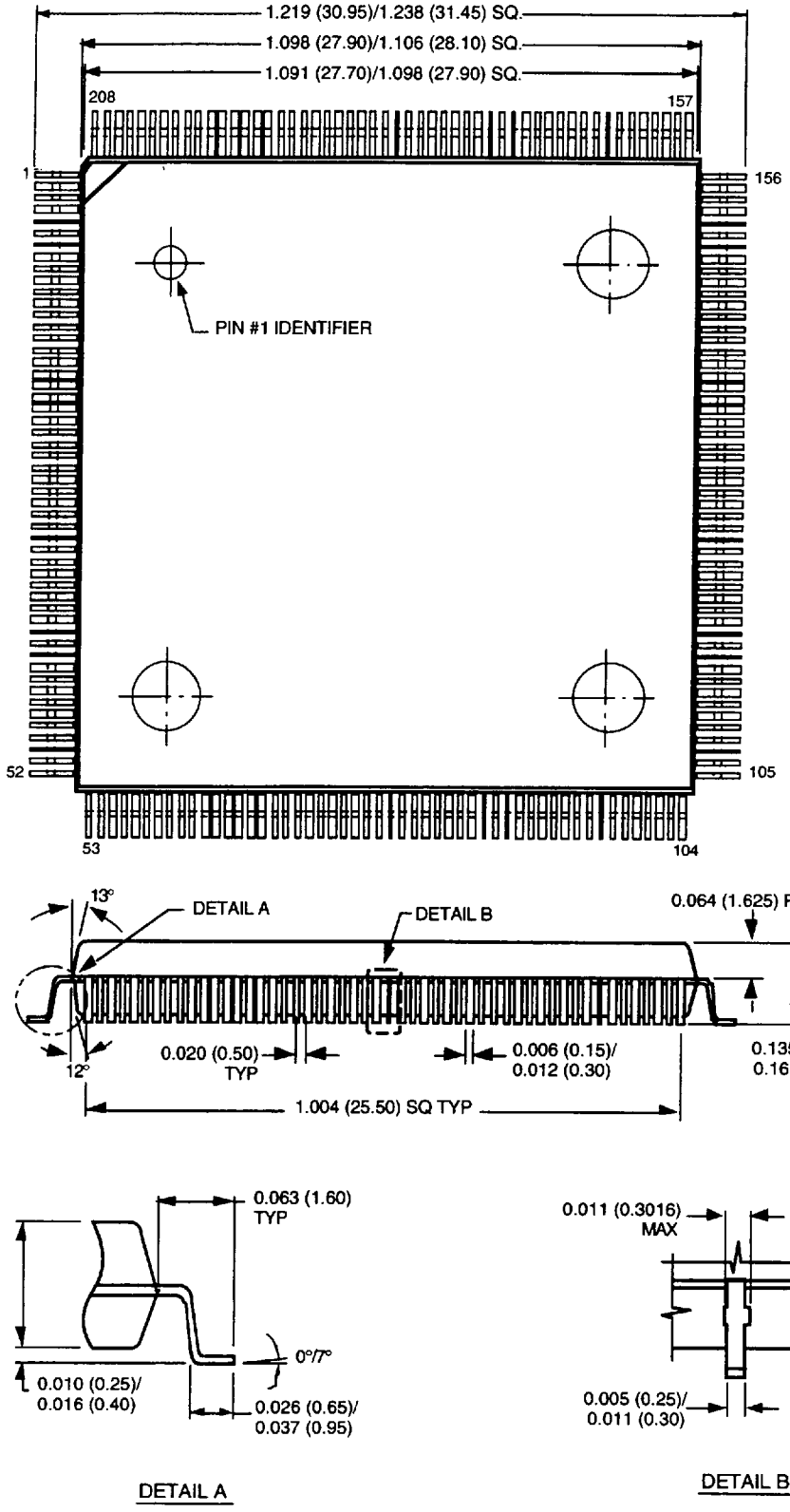


## Outline Diagrams (continued)

Dimensions are in inches and (millimeters).

### 208-Pin SQFP Package




DETAIL A

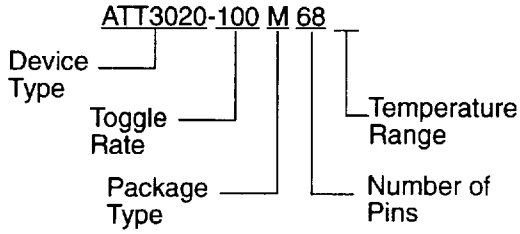
DETAIL B

## Ordering Information

The ATT3000 Series includes standard and high performance FPGAs. The part nomenclature uses two different suffixes for speed designation. The lower speed, ATT3000 Series devices use a flip-flop toggle rate (–50, –70, –100, –125, –150), which corresponds to *XC3000* Series nomenclature. The ATT3000 Series High-Performance FPGAs use a suffix which is an approximation of the lookup table delay (–5, –4, and –3), which corresponds to *XC3100* nomenclature.

For burn-in diagrams and/or package assembly information, order Technical Note 1-5 by calling 1-800-EASY-FPG(A) or 1-800-327-9374.

Example: ATT3020, 100 MHz, 68-Lead PLCC, Commercial Temperature




Note: For availability of device types or packaging options, please contact your AT&T Sales Representative or an authorized distributor.

**Table 27. FPGA Temperature Options**

| Symbol | Description | Temperature |
|---|---|---|
| (Blank) | Commercial | 0 °C to 70 °C |
| I | Industrial | –40 °C to +85 °C |
| M | Military | –55 °C to +125 °C |

**Table 28. FPGA Package Options**

| Symbol | Description |
|---|---|
| H | Plastic Pin Grid Array |
| J | EIAJ Plastic Quad Flat Package |
| M | Plastic Leaded Chip Carrier |
| N | JEDEC Ceramic Quad Flat Package |
| S | Shrink Quad Flat Package |
| R | Ceramic Pin Grid Array |
| T | Thin Quad Flat Package |

## Ordering Information (continued)

### Table 29. Ordering Information—Commercial, Industrial, and Military

| Device | Speed | 44-Pin | 68-Pin | 84-Pin | | 100-Pin | | | 132-Pin | | 160-Pin | 164-Pin | 175-Pin | | 208-Pin |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | PLCC | PLCC | PLCC | Ceramic PGA | EIAJ QFP | TQFP | Ceramic QFP | Plastic PGA | Ceramic PGA | EIAJ QFP | Ceramic QFP | Plastic PGA | Ceramic PGA | Plastic SQFP |
| | | M44 | M68 | M84 | R84 | J100 | T100 | N100 | H132 | R132 | J160 | N164 | H175 | R175 | Q208 |
| ATT3020 | 50 | — | — | — | M | — | — | M | — | — | — | — | — | — | — |
| | 70 | — | CI | CI | CIM | CI | — | CM | — | — | — | — | — | — | — |
| | 100 | — | CI | CI | CIM | CI | — | CM | — | — | — | — | — | — | — |
| | 125 | — | C | C | CM | C | — | CM | — | — | — | — | — | — | — |
| | 150 | — | C | C | C | C | — | C | — | — | — | — | — | — | — |
| | –5 | — | C | C | C | C | — | C | — | — | — | — | — | — | — |
| | –4 | — | C | C | C | C | — | C | — | — | — | — | — | — | — |
| | –3 | — | C | C | C | C | — | C | — | — | — | — | — | — | — |
| ATT3030 | 70 | CI | CI | CI | CI | CI | — | — | — | — | — | — | — | — | — |
| | 100 | CI | CI | CI | CI | CI | — | — | — | — | — | — | — | — | — |
| | 125 | C | C | C | C | C | — | — | — | — | — | — | — | — | — |
| | 150 | C | C | C | C | C | C | — | — | — | — | — | — | — | — |
| | –5 | C | C | C | C | C | C | — | — | — | — | — | — | — | — |
| | –4 | C | C | C | C | C | C | — | — | — | — | — | — | — | — |
| | –3 | C | C | C | C | C | C | — | — | — | — | — | — | — | — |
| ATT3042 | 50 | — | — | — | M | — | — | M | — | M | — | — | — | — | — |
| | 70 | — | — | CI | CIM | CI | — | CM | CI | CIM | — | — | — | — | — |
| | 100 | — | — | CI | CIM | CI | — | CM | CI | CIM | — | — | — | — | — |
| | 125 | — | — | C | CM | C | — | CM | C | CM | — | — | — | — | — |
| | 150 | — | — | C | C | C | C | C | C | C | — | — | — | — | — |
| | –5 | — | — | C | C | C | C | C | C | C | — | — | — | — | — |
| | –4 | — | — | C | C | C | C | C | C | C | — | — | — | — | — |
| | –3 | — | — | C | C | C | C | C | C | C | — | — | — | — | — |
| ATT3064 | 70 | — | — | CI | — | — | — | — | CI | CI | CI | — | — | — | — |
| | 100 | — | — | CI | — | — | — | — | CI | CI | CI | — | — | — | — |
| | 125 | — | — | C | — | — | — | — | C | C | C | — | — | — | — |
| | 150 | — | — | C | — | — | — | — | C | C | C | — | — | — | — |
| | –5 | — | — | C | — | — | — | — | C | C | C | — | — | — | — |
| | –4 | — | — | C | — | — | — | — | C | C | C | — | — | — | — |
| | –3 | — | — | C | — | — | — | — | C | C | C | — | — | — | — |
| ATT3090 | 50 | — | — | — | — | — | — | — | — | — | — | M | — | M | — |
| | 70 | — | — | CI | — | — | — | — | — | — | CI | CIM | CI | CIM | — |
| | 100 | — | — | CI | — | — | — | — | — | — | CI | CIM | CI | CIM | — |
| | 125 | — | — | C | — | — | — | — | — | — | C | CM | C | CM | — |
| | 150 | — | — | C | — | — | — | — | — | — | C | C | C | C | C |
| | –5 | — | — | C | — | — | — | — | — | — | C | C | C | C | C |
| | –4 | — | — | C | — | — | — | — | — | — | C | C | C | C | C |
| | –3 | — | — | C | — | — | — | — | — | — | C | C | C | C | C |

Key: C = Commercial temperature option
I = Industrial temperature option
M = Military temperature option