

1K

Commercial  
Industrial

X2001  
X2001I

128 x 8 Bit

## Nonvolatile Static RAM

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### FEATURES

- Nonvolatile Data Integrity
- Automatic Store Timing
- Store and Array Recall Combined on One Line (NE)
- Enhanced Store Protection
- Infinite E2PROM Array Recall, and RAM Read and Write Cycles
- Single 5V Supply
- High Reliability
  - Store Cycles: 100,000
  - Data Retention: 100 Years
- Fast Access Time: 200 ns Max.
- Automatic Recall on Power-Up
- JEDEC Approved Byte-Wide Pinout

### DESCRIPTION

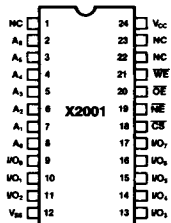
The Xicor X2001 is a byte-wide NOVRAM featuring a high-speed static RAM overlaid bit-for-bit with a nonvolatile electrically erasable PROM (E2PROM). The X2001

is fabricated with the same reliable N-channel floating gate MOS technology used in all Xicor 5V programmable nonvolatile memories. The X2001 features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs, ROMs, EPROMs and E2PROMs.

The NOVRAM design allows data to be easily transferred from RAM to E2PROM (store) and E2PROM to RAM (recall). With  $\overline{NE}$  LOW, these functions are performed in the same manner as RAM read and write operations. The store operation is completed in 10 ms or less and the recall operation is completed in 5  $\mu$ s or less.

Xicor NOVRAMs are designed for unlimited write operations to RAM, either from the host or recalls from E2PROM, and a minimum 100,000 store operations to the E2PROM. Inherent data retention is specified to be greater than 100 years. Refer to RR-520, RR-504 and RR-515 for details on Xicor nonvolatile memory endurance and data retention characteristics.

### PIN CONFIGURATION

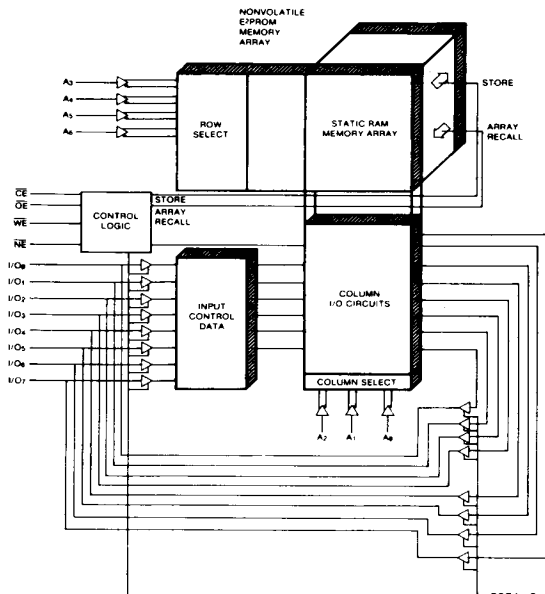


0051-1

### PIN NAMES

A <sub>0</sub> –A <sub>6</sub>	Address Inputs
I/O <sub>0</sub> –I/O <sub>7</sub>	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
$\overline{NE}$	Nonvolatile Enable
V <sub>CC</sub>	+5V
V <sub>SS</sub>	Ground
NC	No Connect

### FUNCTIONAL DIAGRAM



0051-2

# X2001, X2001I

## ABSOLUTE MAXIMUM RATINGS\*

Temperature Under Bias	
X2001	−10°C to +85°C
X2001I	−65°C to +135°C
Storage Temperature	−65°C to +150°C
Voltage on any Pin with Respect to Ground	−1.0V to +7V
D.C. Output Current	5 mA
Lead Temperature (Soldering, 10 Seconds)	300°C

## \*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## D.C. OPERATING CHARACTERISTICS

X2001  $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ,  $V_{CC} = +5\text{V} \pm 5\%$ , unless otherwise specified.

X2001I  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{CC} = +5\text{V} \pm 10\%$ , unless otherwise specified.

Symbol	Parameter	X2001 Limits		X2001I Limits		Units	Test Conditions
		Min.	Max.	Min.	Max.		
$I_{CC}$	$V_{CC}$ Current (Active)		80		100	mA	$\overline{CE} = V_{IL}$ , All Other Inputs = $V_{CC}$ $I_{I/O} = 0\text{ mA}$
$I_{SB}$	$V_{CC}$ Current (Standby)		50		65	mA	All Inputs = $V_{CC}$ $I_{I/O} = 0\text{ mA}$
$I_{LI}$	Input Leakage Current		10		10	$\mu\text{A}$	$V_{IN} = \text{GND to } V_{CC}$
$I_{LO}$	Output Leakage Current		10		10	$\mu\text{A}$	$V_{OUT} = \text{GND to } V_{CC}$
$V_{IL}^{(2)}$	Input Low Voltage	−1.0	0.8	−1.0	0.8	V	
$V_{IH}^{(2)}$	Input High Voltage	2.0	$V_{CC} + 0.5$	2.0	$V_{CC} + 1.0$	V	
$V_{OL}$	Output Low Voltage		0.4		0.4	V	$I_{OL} = 2.1\text{ mA}$
$V_{OH}$	Output High Voltage	2.4		2.4		V	$I_{OH} = -400\text{ }\mu\text{A}$

**CAPACITANCE**  $T_A = 25^\circ\text{C}$ ,  $f = 1.0\text{ MHz}$ ,  $V_{CC} = 5\text{V}$

Symbol	Test	Max.	Units	Conditions
$C_{I/O}^{(1)}$	Input/Output Capacitance	10	pF	$V_{I/O} = 0\text{V}$
$C_{IN}^{(1)}$	Input Capacitance	6	pF	$V_{IN} = 0\text{V}$

## A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	1.5V
Output Load	1 TTL Gate and $C_L = 100\text{ pF}$

## MODE SELECTION

$\overline{CE}$	WE	NE	$\overline{OE}$	Mode	I/O	Power
H	X	X	X	Not Selected	Output High Z	Standby
L	H	H	L	Read RAM	Output Data	Active
L	L	H	X	Write "1" RAM	Input Data High	Active
L	L	H	X	Write "0" RAM	Input Data Low	Active
L	H	L	L	Array Recall	Output High Z	Active
L	L	L	H	Nonvolatile Storing	Output High Z	Active
L	H	H	H	Output Disabled	Output High Z	Active
L	L	L	L	Not Allowed	Output High Z	Active
L	H	L	H	No Operation	Output High Z	Active

**Notes:** (1) This parameter is periodically sampled and not 100% tested.

(2)  $V_{IL}$  min. and  $V_{IH}$  max. are for reference only and are not tested.

# X2001, X2001I

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## ENDURANCE AND DATA RETENTION

Parameter	Min.	Units	Conditions
Endurance	10,000	Data Changes Per Bit	Xicor Reliability Reports RR-520 and RR-504
Store Cycles	100,000	Store Cycles	Xicor Reliability Reports RR-520 and RR-504
Data Retention	100	Years	Xicor Reliability Report RR-515

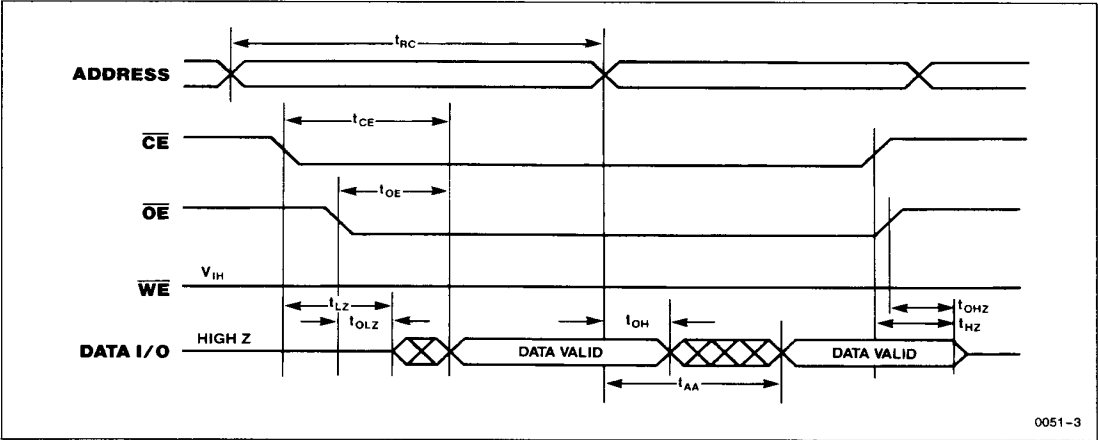
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X2001  $T_A = 0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$ ,  $V_{CC} = +5\text{V} \pm 5\%$ , unless otherwise specified.  
X2001I  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = +5\text{V} \pm 10\%$ , unless otherwise specified.

## Read Cycle Limits

Symbol	Parameter	X2001-20 X2001I-20		X2001-25 X2001I-25		X2001 X2001I		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{RC}$	Read Cycle Time	200		250		300		ns
$t_{CE}$	Chip Enable Access Time		200		250		300	ns
$t_{AA}$	Address Access Time		200		250		300	ns
$t_{OE}$	Output Enable Access Time		70		100		150	ns
$t_{LZ}^{(3)}$	Chip Enable to Output in Low Z	10		10		10		ns
$t_{HZ}^{(3)}$	Chip Disable to Output in High Z	10	100	10	100	10	100	ns
$t_{OLZ}^{(3)}$	Output Enable to Output in Low Z	10		10		10		ns
$t_{OHZ}^{(3)}$	Output Disable to Output in High Z	10	100	10	100	10	100	ns
$t_{OH}$	Output Hold from Address Change	0		0		0		ns

## Read Cycle



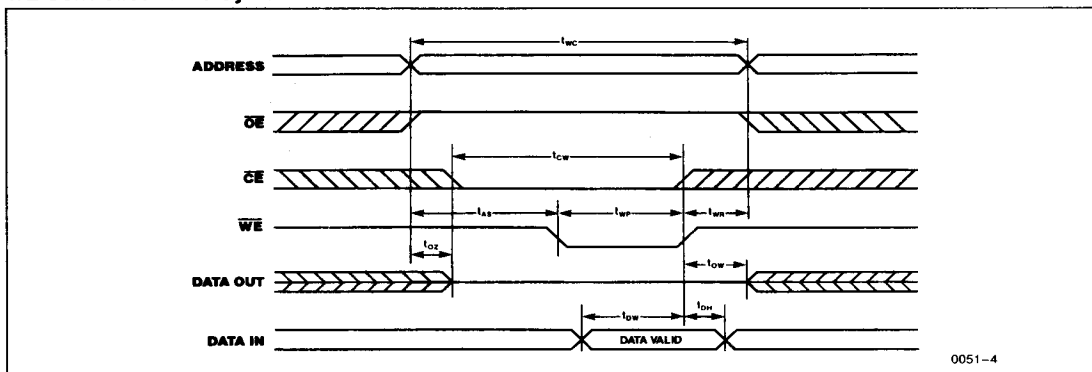
**Note:** (3)  $t_{LZ}$  min.,  $t_{HZ}$  min.,  $t_{OLZ}$  min. and  $t_{OHZ}$  min. are periodically sampled and not 100% tested.  $t_{HZ}$  max. and  $t_{OHZ}$  max. are measured from the point when  $\overline{CE}$  or  $\overline{OE}$  return high (whichever occurs first) to the time when the outputs are no longer driven.

## X2001, X2001I

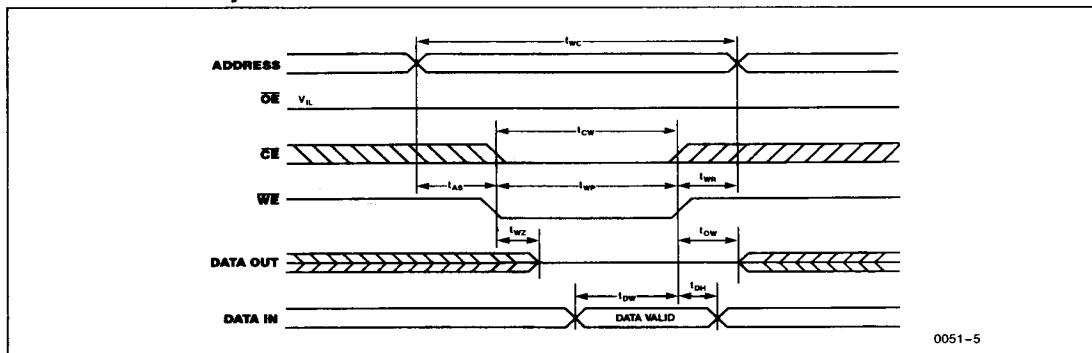
### Write Cycle Limits

Symbol	Parameter	X2001-20 X2001I-20		X2001-25 X2001I-25		X2001 X2001I		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{WC}$	Write Cycle Time	200		250		300		ns
$t_{CW}$	Chip Enable to End of Write Input	200		250		300		ns
$t_{AS}$	Address Setup Time	0		0		0		ns
$t_{WP}$	Write Pulse Width	120		150		200		ns
$t_{WR}$	Write Recovery Time	0		0		0		ns
$t_{DW}$	Data Valid to End of Write	120		150		200		ns
$t_{DH}$	Data Hold Time	0		0		0		ns
$t_{WZ}$	Write Enable to Output in High Z	10	100	10	100	10	100	ns
$t_{OW}$	Output Active from End of Write	10		10		10		ns
$t_{OZ}$	Output Enable to Output in High Z	10	100	10	100	10	100	ns

### $\overline{WE}$ Controlled Write Cycle



### $\overline{CE}$ Controlled Write Cycle



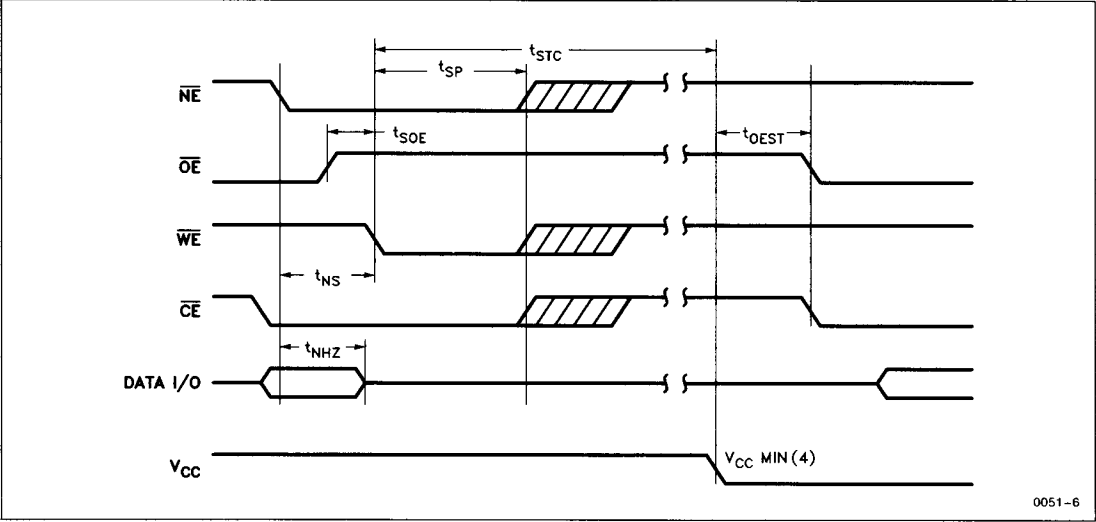
# X2001, X2001I

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## Store Limits

Symbol	Parameter	X2001-20 X2001I-20		X2001-25 X2001I-25		X2001 X2001I		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>STC</sub>	Store Time		10		10		10	ms
t <sub>SP</sub>	Store Pulse Width	120		150		200		ns
t <sub>NHZ</sub>	Nonvolatile Enable to Output in High Z		100		100		100	ns
t <sub>OEST</sub>	Output Enable from End of Store	10		10		10		ns
t <sub>SOE</sub>	$\overline{\text{OE}}$ Disable to Store Function	20		20		20		ns
t <sub>NS</sub>	$\overline{\text{NE}}$ Setup Time from $\overline{\text{WE}}$	0		0		0		ns

## Store Timing



**Note:** (4) X2001  $V_{\text{CC}}$  Min. = 4.75V  
X2001I  $V_{\text{CC}}$  Min. = 4.5V

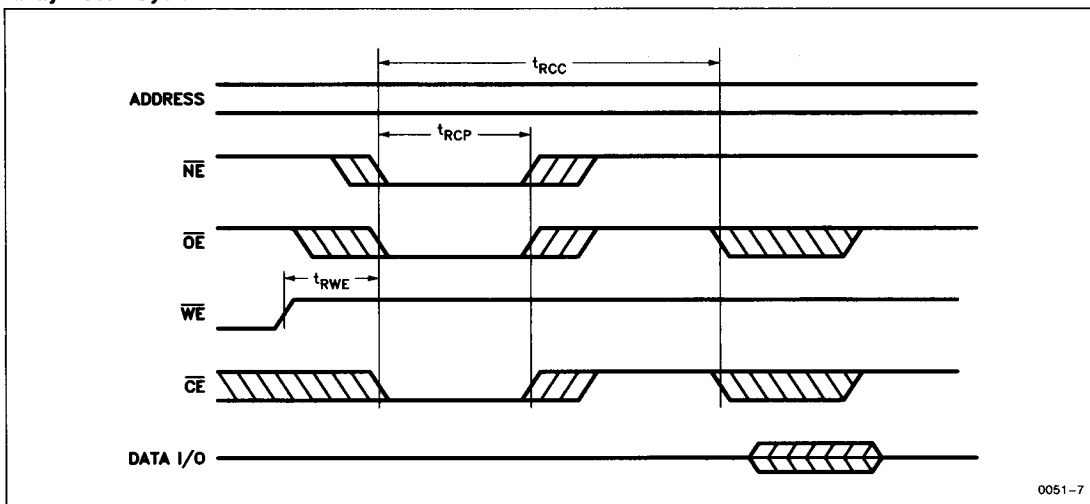
The Store Pulse Width ( $t_{\text{SP}}$ ) is a minimum time that  $\overline{\text{NE}}$ ,  $\overline{\text{WE}}$  and  $\overline{\text{CE}}$  must be LOW simultaneously. To insure data integrity,  $\overline{\text{NE}}$  and  $\overline{\text{CE}}$  must return HIGH after initiation of and throughout the duration ( $t_{\text{STC}}$ , 10 ms) of the Store operation. During  $t_{\text{STC}}$ ,  $\overline{\text{OE}}$  and  $\overline{\text{WE}}$  may go LOW providing the host system access to other devices in the system.

## X2001, X2001I

### Array Recall Cycle Limits

Symbol	Parameter	X2001-20 X2001I-20		X2001-25 X2001I-25		X2001 X2001I		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{RCC}$	Array Recall Time		5.0		5.0		5.0	$\mu s$
$t_{RCP}$	Recall Pulse Width to Initiate Recall	120		150		200		ns
$t_{RWE}$	$\overline{WE}$ Setup Time to $\overline{NE}$	0		0		0		ns

### Array Recall Cycle



The Recall Pulse Width ( $t_{RCP}$ ) is a minimum time that  $\overline{NE}$ ,  $\overline{OE}$  and  $\overline{CE}$  must be LOW simultaneously. To insure data integrity,  $\overline{NE}$  and  $\overline{CE}$  must return HIGH after initiation of and through the duration ( $t_{RCC}$ , 5  $\mu s$ ) of the Recall operation. During  $t_{RCC}$ ,  $\overline{OE}$  and  $\overline{WE}$  may go LOW providing the host access to other devices in the system.

# X2001, X2001I

## PIN DESCRIPTIONS

### Addresses ( $A_0$ – $A_6$ )

The address inputs select an 8-bit word during a read or write operation.

### Chip Enable ( $\overline{CE}$ )

The Chip Enable input must be LOW to enable all read/write operations. When  $\overline{CE}$  is HIGH, power consumption is reduced.

### Output Enable ( $\overline{OE}$ )

The Output Enable input controls the data output buffers and is used to initiate read and recall operations. Output Enable LOW disables a store operation regardless of the state of  $\overline{CE}$ ,  $\overline{WE}$  or  $\overline{NE}$ .

### Data In/Data Out ( $I/O_0$ – $I/O_7$ )

Data is written to or read from the X2001 through the I/O pins. The I/O pins are placed in the high impedance state when either  $\overline{CE}$  or  $\overline{OE}$  is HIGH or when  $\overline{NE}$  is LOW.

### Write Enable ( $\overline{WE}$ )

The Write Enable input controls the writing of data to both the static RAM and stores to the E<sup>2</sup>PROM.

### Nonvolatile Enable ( $\overline{NE}$ )

The Nonvolatile Enable input controls all accesses to the E<sup>2</sup>PROM array (store and recall functions).

## DEVICE OPERATION

The  $\overline{CE}$ ,  $\overline{OE}$ ,  $\overline{WE}$  and  $\overline{NE}$  inputs control the X2001 operation. The X2001 byte-wide NOVRAM uses a 2-line control architecture to eliminate bus contention in a system environment. The I/O bus will be in a high impedance state when either  $\overline{OE}$  or  $\overline{CE}$  is HIGH, or when  $\overline{NE}$  is LOW.

## RAM OPERATIONS

RAM read and write operations are performed as they would be with any static RAM. A read operation

requires  $\overline{CE}$  and  $\overline{OE}$  to be LOW with  $\overline{WE}$  and  $\overline{NE}$  HIGH. A write operation requires  $\overline{CE}$  and  $\overline{WE}$  to be LOW with  $\overline{NE}$  HIGH. There is no limit to the number of read or write operations performed to the RAM portion of the X2001.

## NONVOLATILE OPERATIONS

With  $\overline{NE}$  LOW, recall and store operations are performed in the same manner as RAM read and write operations. A recall operation causes the entire contents of the E<sup>2</sup>PROM to be written into the RAM array. The time required for the operation to complete is 5  $\mu$ s or less. A store operation causes the entire contents of the RAM array to be stored in the nonvolatile E<sup>2</sup>PROM. The time for the operation to complete is 10 ms or less, typically 5 ms.

## POWER-UP RECALL

Upon power-up ( $V_{CC}$ ), the X2001 performs an automatic array recall. When  $V_{CC}$  minimum is reached, the recall is initiated, regardless of the state of  $\overline{CE}$ ,  $\overline{OE}$ ,  $\overline{WE}$  and  $\overline{NE}$ .

## WRITE PROTECTION






The X2001 has three write protect features that are employed to protect the contents of both the nonvolatile memory and the RAM.

- Noise Protection—A  $\overline{WE}$  pulse of less than 20 ns will *not* initiate a write cycle.
- Combined Signal Noise Protection—A combined  $\overline{WE}$  and  $\overline{NE}$  ( $\overline{WE} \bullet \overline{NE}$ ) pulse of less than 20 ns will *not* initiate a store cycle.
- Write Inhibit—Holding either  $\overline{OE}$  LOW,  $\overline{WE}$  HIGH,  $\overline{CE}$  HIGH or  $\overline{NE}$  HIGH during power-up or power-down, will prevent an inadvertent store operation.

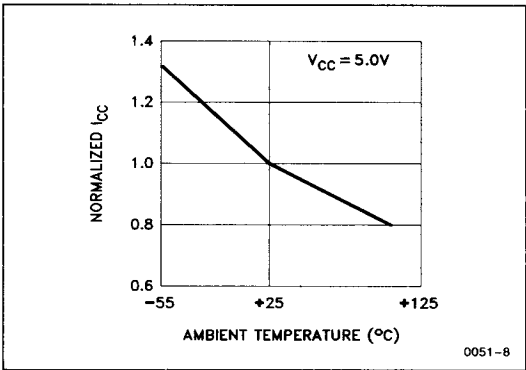
# X2001, X2001I

Part Number	Store Cycles	Data Changes Per Bit
X2001	100,000	10,000
X2001I	100,000	10,000

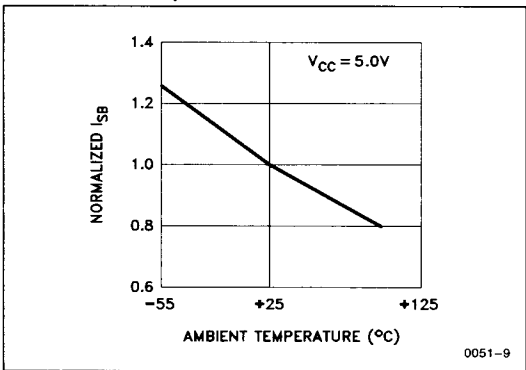
## SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care : Changes Allowed	Changing : State Not Known
	N/A	Center Line is High Impedance

**Normalized Active Supply Current vs. Ambient Temperature**



**Normalized Standby Supply Current vs. Ambient Temperature**



**Normalized Access Time vs. Ambient Temperature**

