

S6C0666

6 BIT 384 CHANNEL RSDS TFT-LCD SOURCE DRIVER

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Ver. 0.0

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INTRODUCTION

The S6C0666 is a Source Driver suitable for Reduced Swing Differential Signaling (RSDS) digital interface. It converts 18-bit digital data into the analog voltage for 384 channels, charging each sub-pixel to the correct gray level corresponding to the digital value.

The RSDS path to the panel timing controller contributes toward lowering radiated EMI, reducing system power consumption and eliminates one of the two pixel busses used in typical XGA, SXGA TFT LCD panels. This single 9-bit differential bus conveys the 18-bit color data for XGA, SXGA panels.

FEATURES

- TFT active matrix LCD source driver LSI
- 64 G/S is possible through 10 (5 by 2) external power supply and D/A converter
- Both dot inversion display and N-line inversion display are possible
- Compatible with gamma-correction
- Logic supply voltage: 2.7 to 3.6 V
- LCD driver supply voltage: 7.0 to 10.5 V
- Output dynamic range: 6.8 to 10.3 Vp-p
- Maximum operating frequency: $f_{max} = 65$ MHz (internal data transmission rate at 2.7 V operation)
- Output: 384 outputs
- Reduced Swing Differential Signaling (RSDS) digital interface for low power consumption and low EMI.
- Minimum RSDS input swing level (CLKN, CLKP, DATAN, DATAP): 100mV
- Data bus interface control pin (DATPOL)
- TCP or COF available

BLOCK DIAGRAM

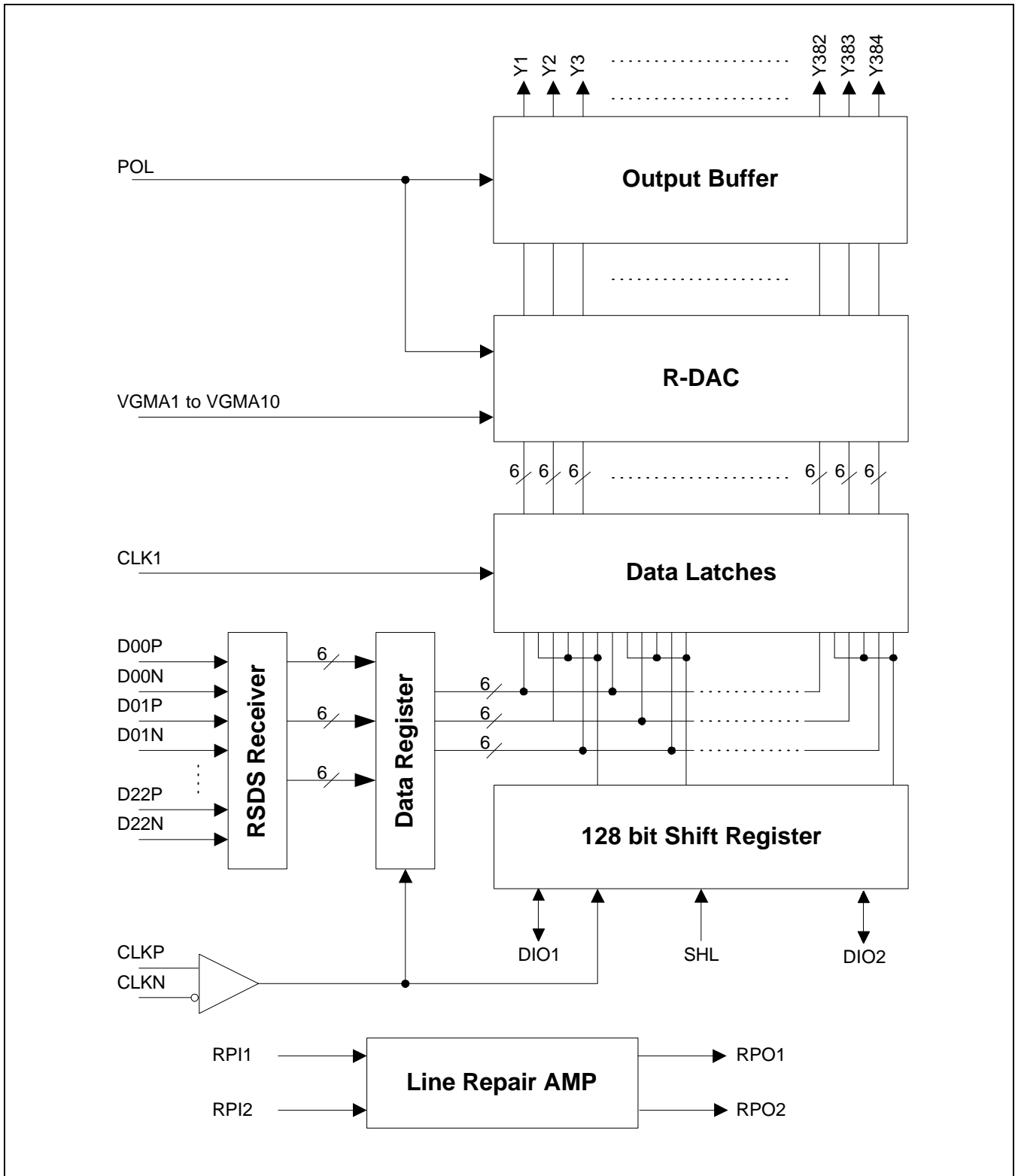


Figure 1. S6C0666 Block Diagram

PIN ASSINGMENTS

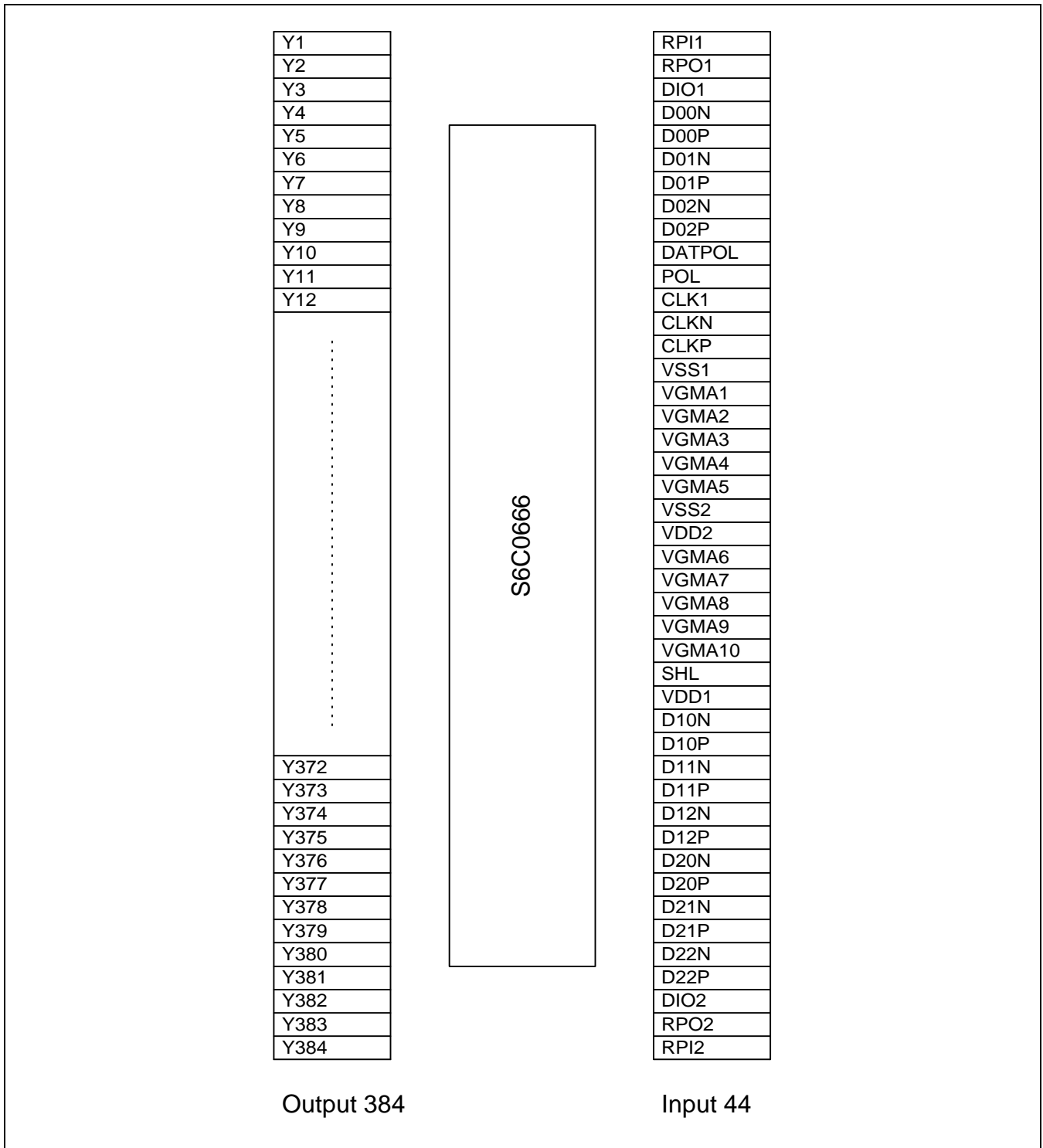


Figure 2. S6C0666 Pin Assignments

PIN DESCRIPTIONS

Symbol	Pin Name	Description
VDD1	Logic power supply	2.7 to 3.6 V
VDD2	Driver power supply	7.0 to 10.5 V
VSS1	Logic ground	Ground (0 V)
VSS2	Driver ground	Ground (0 V)
Y1 to Y384	Driver outputs	The D/A converted 64 gray-scale analog voltage is output.
D0P<0:2> D0N<0:2> D1P<0:2> D1N<0:2> D2P<0:2> D2N<0:2>	RSDS data input	Total data lines consist of 18 data bus. (6-bit digital, 3 colors (R, G, B) and 2 differential input pairs) The 3 - bit differential input pairs generate the internal 6 - bit data through the comparison between DxxP and DxxN.
SHL	Shift direction control input	This pin controls the direction of shift register in cascade connection. When SHL = H: DIO1 input, Y1 → Y384, DIO2 output When SHL = L: DIO2 input, Y384 → Y1, DIO1 output
DIO1	Start pulse input / output	SHL = H: Used as the start pulse input pin. SHL = L: Used as the start pulse output pin.
DIO2	Start pulse input / output	SHL = H: Used as the start pulse output pin. SHL = L: Used as the start pulse input pin.
DATPOL	Data inversion input	DATPOL = L: No inversion DATPOL = H: Data polarity inversion (H↔L)
POL	Polarity input	POL = H: The reference voltage for odd number outputs are VGMA1 to VGMA5 and those for even number outputs are VGMA6 to VGMA10. POL = L: The reference voltage for odd number outputs are VGMA6 to VGMA10 and those for even number outputs are VGMA1 to VGMA5.
CLKP CLKN	RSDS shift clock input	The RSDS clock input pairs generate the internal shift clock, CLK2, through the comparison between CLKP and CLKN.
CLK1	Latch input	S6C0666 clears 128 shift registers at the rising edge of CLK1 and outputs the analog data to the each channel at the falling edge.
VGMA1 to VGMA10	Gamma corrected power supplies	Input the gamma corrected power supplies from external source. VDD2 > VGMA1 > VGMA2 > > VGMA9 > VGMA10 > VSS2 Keep power supplies unchanged during the gray-scale voltage output.
RPI1, RPO1 RPI2, RPO2	Line-repair AMP input / output	The Structure of the line-repair amp is the same as that of the analog output. RPI1 (RPI2) → impedance changed → RPO1 (RPO2)
TEST	Test input	TEST = L: Normal operation mode TEST = H: Test mode (OP AMP CUT-OFF, Rpd = 15 kΩ)

OPERATION DESCRIPTION

RSDS RECEIVER AND DEMUX

The S6C0666 adapts the RSDS interface for EMI solution. The internal RSDS receiver block operates the comparison between the transmitted differential input pair data. The input data lines from the timing controller to the RSDS receiver consist of 6-bit digital, 3 colors, 1 port, 2 differential pairs (DxxP / DxxN).

The input common mode voltage range at the RSDS receiver is 1.2 V. The differential data and clock signals from the panel timing controller arrive at the S6C0666 as multiplexed, even and odd data fields. (i.e., the data is 2:1 multiplexed). The nominal peak to peak swing of this data is 200 mV across a termination resistor.

RSDS DATA BUS INTERFACE CONTROL

DATPOL controls the internal data inversion. When DATPOL = "H", the internal data is inverted. The inverted data is the same that the RSDS receiver operates the comparison between the cross-transmitted differential input pair data. Using the data inversion input pin, DATPOL, the RSDS data bus interface can be changed.

DISPLAY DATA TRANSFER

When DIO1 (or DIO2) pulse is loaded into the internal latch on the falling edge of CLKP, DIO1 (or DIO2) pulse enables the operation of data transfer, so display data is valid on the 2nd falling edge of CLKP. Once all the data of 384 channels is loaded into internal latch, it goes into stand-by state automatically, and any new data is not accepted even though CLKP is provided until next DIO1 (or DIO2) input. When next DIO1 (or DIO2) is provided, new display data is valid on the 2nd falling edge of CLKP after the rising edge of DIO1 (or DIO2).

EXTENSION OF OUTPUT

Output pin can be adjusted to an extended screen by cascade connection. When SHL = "L", Connect DIO1 pin of the previous stage to the DIO2 pin of the next stage and all the input pins except DIO1 and DIO2 are connected together in each device. When SHL = "H", Connect DIO2 pin of the previous stage to the DIO1 pin of the next stage and all the input pins except DIO2 and DIO1 are connected together in each device.

RELATIONSHIP BETWEEN INPUT DATA VALUE AND OUTPUT VOLTAGE

The LCD drive output voltages are determined by the input data and 10 (5 by 2) gamma corrected power supplies (VGMA1 to VGMA10). Besides, to be able to deal with dot line inversion when mounted on a single-side, gradation voltages with different polarity can be output to the odd number output pins and the even number output pins. Among 5 by 2 gamma corrected voltages, input gray scale voltages of the same polarity with respect to the common voltage, for the respective 5 gamma corrected voltages of VGMA1 to VGMA5 and VGMA6 to VGMA10.

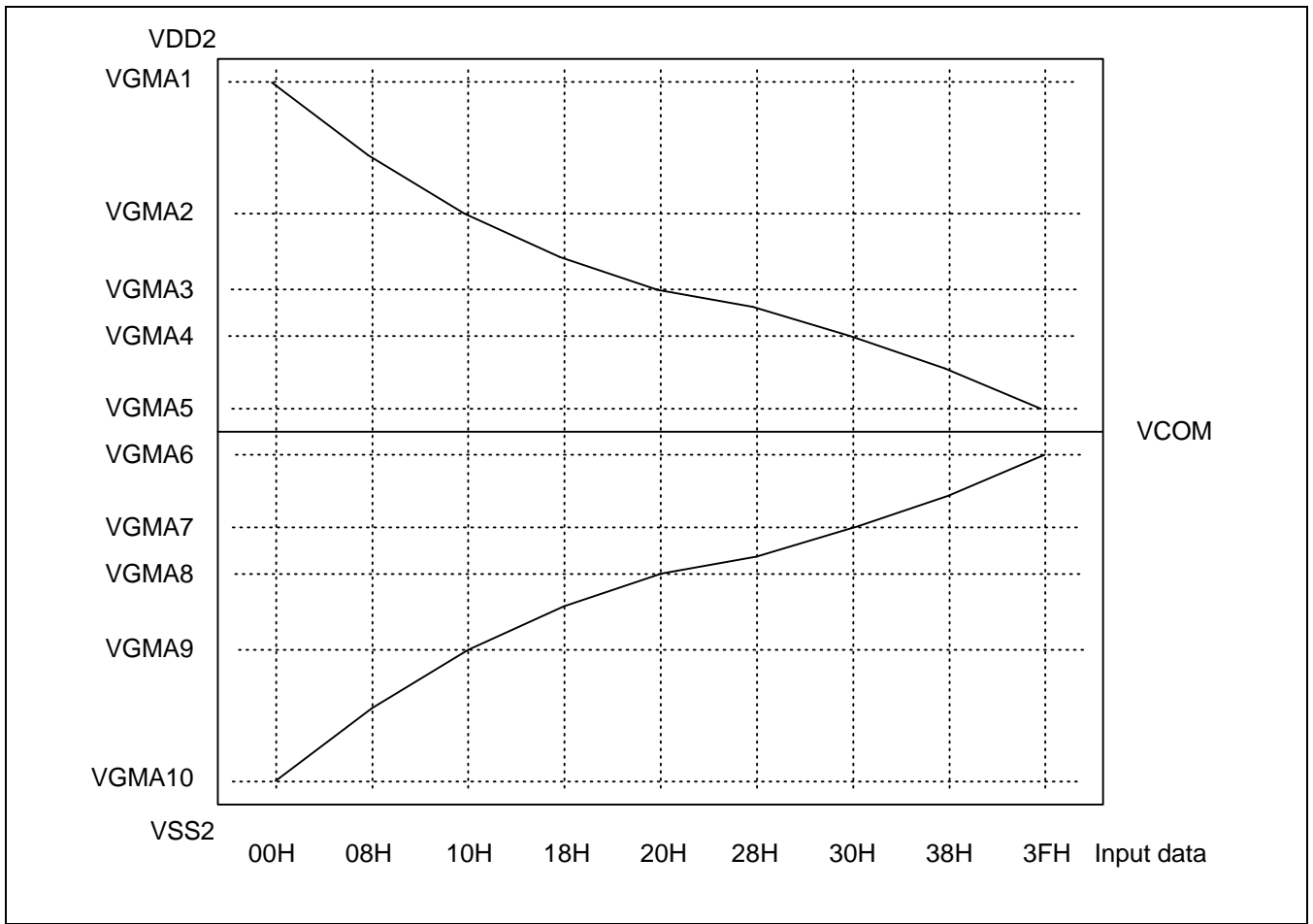


Figure 3. Gamma Correction Curve

Table 1. Resistor Strings (R0 to R62, unit: Ω)

Name	Value	Name	Value	Name	Value	Name	Value
R0	500	R16	330	R32	175	R48	210
R1	500	R17	330	R33	175	R49	220
R2	500	R18	330	R34	170	R50	230
R3	500	R19	320	R35	170	R51	240
R4	500	R20	300	R36	165	R52	250
R5	500	R21	280	R37	165	R53	260
R6	500	R22	270	R38	165	R54	270
R7	500	R23	260	R39	165	R55	290
R8	500	R24	250	R40	170	R56	300
R9	500	R25	240	R41	170	R57	310
R10	500	R26	230	R42	170	R58	320
R11	500	R27	220	R43	175	R59	340
R12	450	R28	210	R44	175	R60	340
R13	450	R29	200	R45	175	R61	340
R14	400	R30	190	R46	180	R62	340
R15	370	R31	180	R47	200		

Table 2. Relationship between Input Data and Output Voltage Value

Input Data	DX5	DX4	DX3	DX2	DX1	DX0	G/S	Output Voltage
00H	0	0	0	0	0	0	VH0	VGMA1
01H	0	0	0	0	0	1	VH1	$VGMA1+(VGMA2 - VGMA1) \times 500/7670$
02H	0	0	0	0	1	0	VH2	$VGMA1+(VGMA2-VGMA1) \times 1000/7670$
03H	0	0	0	0	1	1	VH3	$VGMA1+(VGMA2-VGMA1) \times 1500/7670$
04H	0	0	0	1	0	0	VH4	$VGMA1+(VGMA2-VGMA1) \times 2000/7670$
05H	0	0	0	1	0	1	VH5	$VGMA1+(VGMA2-VGMA1) \times 2500/7670$
06H	0	0	0	1	1	0	VH6	$VGMA1+(VGMA2-VGMA1) \times 3000/7670$
07H	0	0	0	1	1	1	VH7	$VGMA1+(VGMA2-VGMA1) \times 3500/7670$
08H	0	0	1	0	0	0	VH8	$VGMA1+(VGMA2-VGMA1) \times 4000/7670$
09H	0	0	1	0	0	1	VH9	$VGMA1+(VGMA2-VGMA1) \times 4500/7670$
0AH	0	0	1	0	1	0	VH10	$VGMA1+(VGMA2-VGMA1) \times 5000/7670$
0BH	0	0	1	0	1	1	VH11	$VGMA1+(VGMA2-VGMA1) \times 5500/7670$
0CH	0	0	1	1	0	0	VH12	$VGMA1+(VGMA2-VGMA1) \times 6000/7670$
0DH	0	0	1	1	0	1	VH13	$VGMA1+(VGMA2-VGMA1) \times 6450/7670$
0EH	0	0	1	1	1	0	VH14	$VGMA1+(VGMA2-VGMA1) \times 6900/7670$
0FH	0	0	1	1	1	1	VH15	$VGMA1+(VGMA2-VGMA1) \times 7300/7670$
10H	0	1	0	0	0	0	VH16	VGMA2
11H	0	1	0	0	0	1	VH17	$VGMA2+(VGMA3-VGMA2) \times 330/4140$
12H	0	1	0	0	1	0	VH18	$VGMA2+(VGMA3-VGMA2) \times 660/4140$
13H	0	1	0	0	1	1	VH19	$VGMA2+(VGMA3-VGMA2) \times 990/4140$
14H	0	1	0	1	0	0	VH20	$VGMA2+(VGMA3-VGMA2) \times 1310/4140$
15H	0	1	0	1	0	1	VH21	$VGMA2+(VGMA3-VGMA2) \times 1610/4140$
16H	0	1	0	1	1	0	VH22	$VGMA2+(VGMA3-VGMA2) \times 1890/4140$
17H	0	1	0	1	1	1	VH23	$VGMA2+(VGMA3-VGMA2) \times 2160/4140$
18H	0	1	1	0	0	0	VH24	$VGMA2+(VGMA3-VGMA2) \times 2420/4140$
19H	0	1	1	0	0	1	VH25	$VGMA2+(VGMA3-VGMA2) \times 2670/4140$
1AH	0	1	1	0	1	0	VH26	$VGMA2+(VGMA3-VGMA2) \times 2910/4140$
1BH	0	1	1	0	1	1	VH27	$VGMA2+(VGMA3-VGMA2) \times 3140/4140$
1CH	0	1	1	1	0	0	VH28	$VGMA2+(VGMA3-VGMA2) \times 3360/4140$
1DH	0	1	1	1	0	1	VH29	$VGMA2+(VGMA3-VGMA2) \times 3570/4140$
1EH	0	1	1	1	1	0	VH30	$VGMA2+(VGMA3-VGMA2) \times 3770/4140$
1FH	0	1	1	1	1	1	VH31	$VGMA2+(VGMA3-VGMA2) \times 3960/4140$

NOTE: VDD2 > VGMA1 > VGMA2 > VGMA3 > VGMA4 > VGMA5

Table 2. Relationship between Input Data and Output Voltage Value (Continued)

Input Data	DX5	DX4	DX3	DX2	DX1	DX0	G/S	Output Voltage
20H	1	0	0	0	0	0	VH32	VGMA3
21H	1	0	0	0	0	1	VH33	$VGMA3+(VGMA4-VGMA3) \times 175/2765$
22H	1	0	0	0	1	0	VH34	$VGMA3+(VGMA4-VGMA3) \times 350/2765$
23H	1	0	0	0	1	1	VH35	$VGMA3+(VGMA4-VGMA3) \times 520/2765$
24H	1	0	0	1	0	0	VH36	$VGMA3+(VGMA4-VGMA3) \times 690/2765$
25H	1	0	0	1	0	1	VH37	$VGMA3+(VGMA4-VGMA3) \times 855/2765$
26H	1	0	0	1	1	0	VH38	$VGMA3+(VGMA4-VGMA3) \times 1020/2765$
27H	1	0	0	1	1	1	VH39	$VGMA3+(VGMA4-VGMA3) \times 1185/2765$
28H	1	0	1	0	0	0	VH40	$VGMA3+(VGMA4-VGMA3) \times 1350/2765$
29H	1	0	1	0	0	1	VH41	$VGMA3+(VGMA4-VGMA3) \times 1520/2765$
2AH	1	0	1	0	1	0	VH42	$VGMA3+(VGMA4-VGMA3) \times 1690/2765$
2BH	1	0	1	0	1	1	VH43	$VGMA3+(VGMA4-VGMA3) \times 1860/2765$
2CH	1	0	1	1	0	0	VH44	$VGMA3+(VGMA4-VGMA3) \times 2035/2765$
2DH	1	0	1	1	0	1	VH45	$VGMA3+(VGMA4-VGMA3) \times 2210/2765$
2EH	1	0	1	1	1	0	VH46	$VGMA3+(VGMA4-VGMA3) \times 2385/2765$
2FH	1	0	1	1	1	1	VH47	$VGMA3+(VGMA4-VGMA3) \times 2565/2765$
30H	1	1	0	0	0	0	VH48	VGMA4
31H	1	1	0	0	0	1	VH49	$VGMA4+(VGMA5-VGMA4) \times 210/4260$
32H	1	1	0	0	1	0	VH50	$VGMA4+(VGMA5-VGMA4) \times 430/4260$
33H	1	1	0	0	1	1	VH51	$VGMA4+(VGMA5-VGMA4) \times 660/4260$
34H	1	1	0	1	0	0	VH52	$VGMA4+(VGMA5-VGMA4) \times 900/4260$
35H	1	1	0	1	0	1	VH53	$VGMA4+(VGMA5-VGMA4) \times 1150/4260$
36H	1	1	0	1	1	0	VH54	$VGMA4+(VGMA5-VGMA4) \times 1410/4260$
37H	1	1	0	1	1	1	VH55	$VGMA4+(VGMA5-VGMA4) \times 1680/4260$
38H	1	1	1	0	0	0	VH56	$VGMA4+(VGMA5-VGMA4) \times 1970/4260$
39H	1	1	1	0	0	1	VH57	$VGMA4+(VGMA5-VGMA4) \times 2270/4260$
3AH	1	1	1	0	1	0	VH58	$VGMA4+(VGMA5-VGMA4) \times 2580/4260$
3BH	1	1	1	0	1	1	VH59	$VGMA4+(VGMA5-VGMA4) \times 2900/4260$
3CH	1	1	1	1	0	0	VH60	$VGMA4+(VGMA5-VGMA4) \times 3240/4260$
3DH	1	1	1	1	0	1	VH61	$VGMA4+(VGMA5-VGMA4) \times 3580/4260$
3EH	1	1	1	1	1	0	VH62	$VGMA4+(VGMA5-VGMA4) \times 3920/4260$
3FH	1	1	1	1	1	1	VH63	VGMA5

Table 2. Relationship between Input Data and Output Voltage Value (Continued)

Input Data	DX5	DX4	DX3	DX2	DX1	DX0	G/S	Output Voltage
00H	0	0	0	0	0	0	VL0	VGMA10
01H	0	0	0	0	0	1	VL1	$VGMA10+(VGMA9-VGMA10) \times 500/7670$
02H	0	0	0	0	1	0	VL2	$VGMA10+(VGMA9-VGMA10) \times 1000/7670$
03H	0	0	0	0	1	1	VL3	$VGMA10+(VGMA9-VGMA10) \times 1500/7670$
04H	0	0	0	1	0	0	VL4	$VGMA10+(VGMA9-VGMA10) \times 2000/7670$
05H	0	0	0	1	0	1	VL5	$VGMA10+(VGMA9-VGMA10) \times 2500/7670$
06H	0	0	0	1	1	0	VL6	$VGMA10+(VGMA9-VGMA10) \times 3000/7670$
07H	0	0	0	1	1	1	VL7	$VGMA10+(VGMA9-VGMA10) \times 3500/7670$
08H	0	0	1	0	0	0	VL8	$VGMA10+(VGMA9-VGMA10) \times 4000/7670$
09H	0	0	1	0	0	1	VL9	$VGMA10+(VGMA9-VGMA10) \times 4500/7670$
0AH	0	0	1	0	1	0	VL10	$VGMA10+(VGMA9-VGMA10) \times 5000/7670$
0BH	0	0	1	0	1	1	VL11	$VGMA10+(VGMA9-VGMA10) \times 5500/7670$
0CH	0	0	1	1	0	0	VL12	$VGMA10+(VGMA9-VGMA10) \times 6000/7670$
0DH	0	0	1	1	0	1	VL13	$VGMA10+(VGMA9-VGMA10) \times 6450/7670$
0EH	0	0	1	1	1	0	VL14	$VGMA10+(VGMA9-VGMA10) \times 6900/7670$
0FH	0	0	1	1	1	1	VL15	$VGMA10+(VGMA9-VGMA10) \times 7300/7670$
10H	0	1	0	0	0	0	VL16	VGMA9
11H	0	1	0	0	0	1	VL17	$VGMA9+(VGMA8-VGMA9) \times 330/4140$
12H	0	1	0	0	1	0	VL18	$VGMA9+(VGMA8-VGMA9) \times 660/4140$
13H	0	1	0	0	1	1	VL19	$VGMA9+(VGMA8-VGMA9) \times 990/4140$
14H	0	1	0	1	0	0	VL20	$VGMA9+(VGMA8-VGMA9) \times 1310/4140$
15H	0	1	0	1	0	1	VL21	$VGMA9+(VGMA8-VGMA9) \times 1610/4140$
16H	0	1	0	1	1	0	VL22	$VGMA9+(VGMA8-VGMA9) \times 1890/4140$
17H	0	1	0	1	1	1	VL23	$VGMA9+(VGMA8-VGMA9) \times 2160/4140$
18H	0	1	1	0	0	0	VL24	$VGMA9+(VGMA8-VGMA9) \times 2420/4140$
19H	0	1	1	0	0	1	VL25	$VGMA9+(VGMA8-VGMA9) \times 2670/4140$
1AH	0	1	1	0	1	0	VL26	$VGMA9+(VGMA8-VGMA9) \times 2910/4140$
1BH	0	1	1	0	1	1	VL27	$VGMA9+(VGMA8-VGMA9) \times 3140/4140$
1CH	0	1	1	1	0	0	VL28	$VGMA9+(VGMA8-VGMA9) \times 3360/4140$
1DH	0	1	1	1	0	1	VL29	$VGMA9+(VGMA8-VGMA9) \times 3570/4140$
1EH	0	1	1	1	1	0	VL30	$VGMA9+(VGMA8-VGMA9) \times 3770/4140$
1FH	0	1	1	1	1	1	VL31	$VGMA9+(VGMA8-VGMA9) \times 3960/4140$

NOTE: VGMA6 > VGMA7 > VGMA8 > VGMA9 > VGMA10 > VSS2

Table 2. Relationship between Input Data and Output Voltage Value (Continued)

Input Data	DX5	DX4	DX3	DX2	DX1	DX0	G/S	Output Voltage
20H	1	0	0	0	0	0	VL32	VGMA8
21H	1	0	0	0	0	1	VL33	$VGMA8+(VGMA7-VGMA8) \times 175/2765$
22H	1	0	0	0	1	0	VL34	$VGMA8+(VGMA7-VGMA8) \times 350/2765$
23H	1	0	0	0	1	1	VL35	$VGMA8+(VGMA7-VGMA8) \times 520/2765$
24H	1	0	0	1	0	0	VL36	$VGMA8+(VGMA7-VGMA8) \times 690/2765$
25H	1	0	0	1	0	1	VL37	$VGMA8+(VGMA7-VGMA8) \times 855/2765$
26H	1	0	0	1	1	0	VL38	$VGMA8+(VGMA7-VGMA8) \times 1020/2765$
27H	1	0	0	1	1	1	VL39	$VGMA8+(VGMA7-VGMA8) \times 1185/2765$
28H	1	0	1	0	0	0	VL40	$VGMA8+(VGMA7-VGMA8) \times 1350/2765$
29H	1	0	1	0	0	1	VL41	$VGMA8+(VGMA7-VGMA8) \times 1520/2765$
2AH	1	0	1	0	1	0	VL42	$VGMA8+(VGMA7-VGMA8) \times 1690/2765$
2BH	1	0	1	0	1	1	VL43	$VGMA8+(VGMA7-VGMA8) \times 1860/2765$
2CH	1	0	1	1	0	0	VL44	$VGMA8+(VGMA7-VGMA8) \times 2035/2765$
2DH	1	0	1	1	0	1	VL45	$VGMA8+(VGMA7-VGMA8) \times 2210/2765$
2EH	1	0	1	1	1	0	VL46	$VGMA8+(VGMA7-VGMA8) \times 2385/2765$
2FH	1	0	1	1	1	1	VL47	$VGMA8+(VGMA7-VGMA8) \times 2565/2765$
30H	1	1	0	0	0	0	VL48	VGMA7
31H	1	1	0	0	0	1	VL49	$VGMA7+(VGMA6-VGMA7) \times 210/4260$
32H	1	1	0	0	1	0	VL50	$VGMA7+(VGMA6-VGMA7) \times 430/4260$
33H	1	1	0	0	1	1	VL51	$VGMA7+(VGMA6-VGMA7) \times 660/4260$
34H	1	1	0	1	0	0	VL52	$VGMA7+(VGMA6-VGMA7) \times 900/4260$
35H	1	1	0	1	0	1	VL53	$VGMA7+(VGMA6-VGMA7) \times 1150/4260$
36H	1	1	0	1	1	0	VL54	$VGMA7+(VGMA6-VGMA7) \times 1410/4260$
37H	1	1	0	1	1	1	VL55	$VGMA7+(VGMA6-VGMA7) \times 1680/4260$
38H	1	1	1	0	0	0	VL56	$VGMA7+(VGMA6-VGMA7) \times 1970/4260$
39H	1	1	1	0	0	1	VL57	$VGMA7+(VGMA6-VGMA7) \times 2270/4260$
3AH	1	1	1	0	1	0	VL58	$VGMA7+(VGMA6-VGMA7) \times 2580/4260$
3BH	1	1	1	0	1	1	VL59	$VGMA7+(VGMA6-VGMA7) \times 2900/4260$
3CH	1	1	1	1	0	0	VL60	$VGMA7+(VGMA6-VGMA7) \times 3240/4260$
3DH	1	1	1	1	0	1	VL61	$VGMA7+(VGMA6-VGMA7) \times 3580/4260$
3EH	1	1	1	1	1	0	VL62	$VGMA7+(VGMA6-VGMA7) \times 3920/4260$
3FH	1	1	1	1	1	1	VL63	VGMA6

ABSOLUTE MAXIMUM RATINGS

Table 3. Absolute Maximum Ratings (VSS1 = VSS2 = 0 V)

Parameter	Symbol	Ratings	Unit
Logic supply voltage	VDD1	-0.3 to 5.0	V
Driver supply voltage	VDD2	-0.3 to 12.0	V
Input voltage	VGMA1 to 10	-0.3 to VDD2 + 0.3	V
	RPI1, RPI2	-0.3 to VDD2 + 0.3	
	Others	-0.3 to VDD1 + 0.3	
Output voltage	DIO1, DIO2	-0.3 to VDD1 + 0.3	V
	Y1 to Y384	-0.3 to VDD2 + 0.3	
	RPO1, RPO2	-0.3 to VDD2 + 0.3	
Operating power dissipation	Pd	150	mW
Operation temperature	Top	-20 to 75	°C
Storage temperature	Tstg	-55 to 125	°C

CAUTIONS:

If LSIs are stressed beyond those listed above “absolute maximum ratings”, they may be permanently destroyed. These are stress ratings only, and functional operation of the device at these or any other condition beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Turn on power order: VDD1 → control signal input → VDD2 → VGMA1 to VGMA10

Turn off power order: VGMA1 to VGMA10 → VDD2 → control signal input → VDD1

RECOMMENDED OPERATION CONDITIONS

Table 4. Recommended Operation Conditions (Ta = - 20 to 70 °C, VSS1 = VSS2 = 0 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Logic supply voltage	VDD1	2.7	3.0	3.6	V
Driver supply voltage	VDD2	7.0	-	10.5	V
Gamma corrected voltage	VGMA1 to VGMA5	0.5VDD2	-	VDD2 - 0.1	V
	VGMA6 to VGMA10	+ 0.1	-	0.5VDD2	V
Driver part output voltage	Vyo	+ 0.1	-	VDD2 - 0.1	V
Maximum clock frequency	fmax	VDD1 = 2.7V	-	65	MHz
		VDD1 = 3.0V	-	75	
Output load capacitance	CL	-	-	150	pF / PIN

DC CHARACTERISTICS

Table 5 . DC Characteristics
(Ta = -20 to 75 °C, VDD1 = 2.7 to 3.6 V, VDD2 = 7.0 to 10.5 V, VSS1 = VSS2 = 0)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
High level input voltage	VIH	SHL, CLK1, POL, DIO1 (DIO2)	0.7VDD1	-	VDD1	V
Low level input voltage	VIL		0	-	0.3VDD1	
Input leakage current	IL1		-1	-	1	μA
Repair input leak current	IL2	RPI1(RPI2)	-1	-	1	
High level output voltage	VOH	DIO1(DIO2), IO = - 1.0 mA	VDD1 - 0.5	-	-	V
Low level output voltage	VOL	DIO1(DIO2), IO = + 1.0 mA	-	-	0.5	
Resistance between gamma voltage	R0 to R62	Refer to Table 1. Resistor Strings	Rn × 0.7		Rn × 1.3	Ω
Driver output current	IVOH1	VDD2 = 8.0 V, Vx(1) = 4.0 V, Vyo(2) = 7.0 V	-	-0.8	-0.4	mA
	IVOL1	VDD2 = 8.0 V, Vx(1) = 4.0 V, Vyo(2) = 1.0 V	0.4	0.8	-	
Line-repair Driver output current	IVOH2	VDD2 = 8.0 V, Vx(1) = 4.0 V, Vyo(2) = 7.0 V	-	-2.0	-1.0	
	IVOL2	VDD2 = 8.0 V, Vx(1) = 4.0 V, Vyo(2) = 1.0 V	1.0	2.0	-	
Output voltage deviation	DVO	Input data: 00H to 3FH	-	± 10	± 20	mV
Output swing voltage difference deviation	dVrms(3)	Input data: 00H to 3FH	-	± 5	± 15	
Output voltage range	VYO	Input data: 00H to 3FH	VSS2 + 0.1	-	VDD2 - 0.1	V
Logic part dynamic current	IDD1	VDD1 = 3.0 V (4)	-	6.0	8.0	mA
Driver part dynamic current	IDD2	VDD1 = 3.0 V, VDD2 = 9.0 V, VGMA1 = 8.5 V, VGMA5 = 5.0 V, VGMA6 = 4.0 V, VGMA10 = 0.5 V (4) (5)	-	6.0	9.0	

NOTES:

- Vx is the voltage applied to analog output pins Y1 to Y384.
- Vyo is the output voltage of analog output pins Y1 to Y384.
- dVrms = max. deviation of (VHx-VLx)
VHx; the x gray level positive polarity driver output voltage
VLx; the x gray level negative polarity driver output voltage
- CLK1 period = 20 μs at fCLKP = 33 MHz, data pattern = 1010....., (checkerboard pattern), Ta = 25 °C
- Yout load condition (refer to Figure 4. Yout Load Condition) applied.

RSDS CHARACTERISTICS

Table 6 . RSDS Characteristics
($T_a = -20$ to 75 °C, $V_{DD1} = 2.7$ to 3.6 V, $V_{DD2} = 7.0$ to 10.5 V, $V_{SS1} = V_{SS2} = 0$)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
RSDS high input voltage	V_{IHRSDS}	$V_{CMRSDS} = +1.2$ V ⁽¹⁾	100	200		mV
RSDS low input voltage	V_{ILRSDS}	$V_{CMRSDS} = +1.2$ V ⁽¹⁾		-200	-100	
RSDS common mode input voltage range	V_{CMRSDS}	$V_{DIFFRSDS} = +200$ mV ⁽²⁾	$V_{SS1} + 0.1$	-	$V_{DD1} - 1.5$	V
RSDS input leakage current	IDL	DxxP, DxxN, CLKP, CLKN	-10	-	10	μ A

NOTES:

- $V_{CMRSDS} = (V_{CLKP} + V_{CLKN}) / 2$ or $V_{CMRSDS} = (V_{DxxP} + V_{DxxN}) / 2$
- $V_{DIFFRSDS} = V_{CLKP} - V_{CLKN}$ or $V_{DIFFRSDS} = V_{DxxP} - V_{DxxN}$

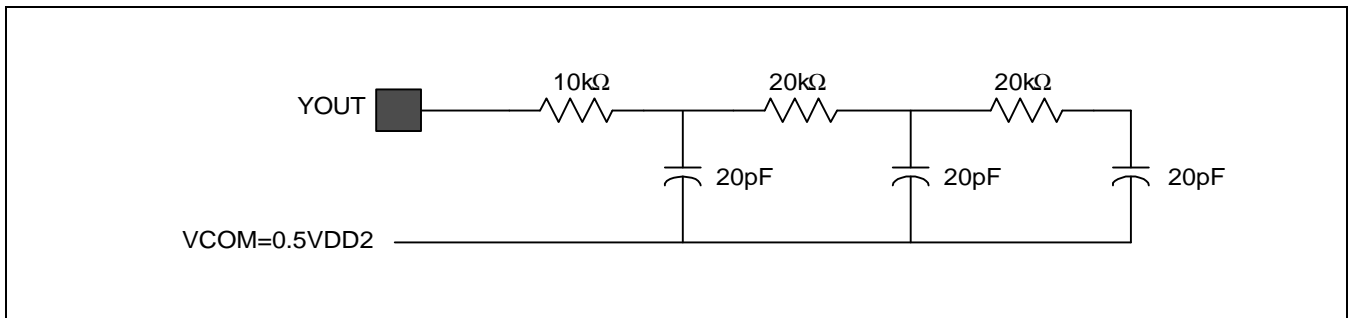


Figure 4. Yout Load Condition

AC CHARACTERISTICS

Table 6. AC Characteristics (Ta = - 20 to 75 °C, VDD2 = 7.0 to 10.5 V, VSS1 = VSS2 = 0 V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock pulse width	PWCLK	-	15	-	-	ns
Clock pulse low period	PWCLK(L)	-	6	-	-	
Clock pulse high period	PWCLK(H)	-	6	-	-	
Data setup time	tSETUP1	-	2	-	-	
Data hold time	tHOLD1	-	0	-	-	
Start pulse setup time	tSETUP2	-	4	-	-	
Start pulse hold time	tHOLD2	-	2	-	-	
Start pulse delay time	tPLH1	CL = 15pF	-	-	12	
DIO signal pulse width	PWDIO		1CLKP	-	2CLKP	CLKP period
CLK1 setup time	tSETUP3	-	2CLKP	-	-	μs
CLK1 high pulse width	PWCLK1	-	5CLKP	-	2	
Driver output delay time1	tPHL1	(1) (3)	-	-	6	
Driver output delay time2	tPHL2	(2) (3)	-	-	10	
Repair output delay time1	tPHL3	CL = 150pF	-	-	6	
Repair output delay time2	tPHL4	CL = 150pF	-	-	10	
Last data timing	tLDT	-	1CLKP	-	-	CLKP period
CLK1-CLK2 time	tCLK1-CLK2	CLK1 ↑ → CLKP ↓	4	-	-	ns
POL-CLK1 time	tPOL-CLK1	POL ↑ or ↓ → CLK1 ↑	14	-	-	
CLK1-POL time	tCLK1-POL	CLK1 ↓ → POL ↑ or ↓	10	-	-	

NOTES:

1. The value is specified when the drive voltage value reaches the target output voltage level of 90%
2. The value is specified when the drive voltage value reaches the target output voltage level of 6-bit accuracy.
3. Yout load condition (refer to Figure 4. Yout Load Condition)

WAVEFORMS

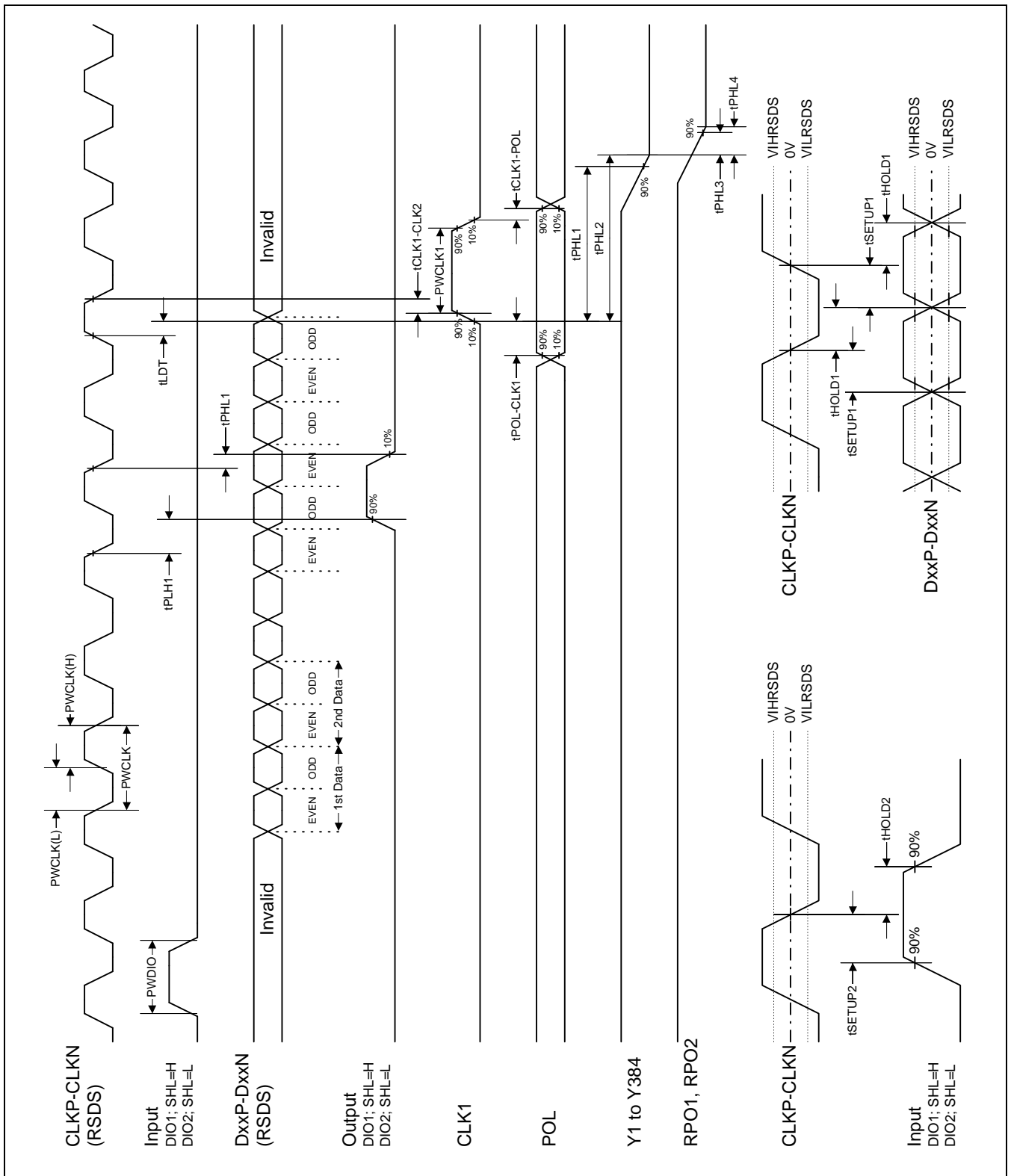


Figure 5. Waveforms

RSDS DATA TIMING DIAGRAM

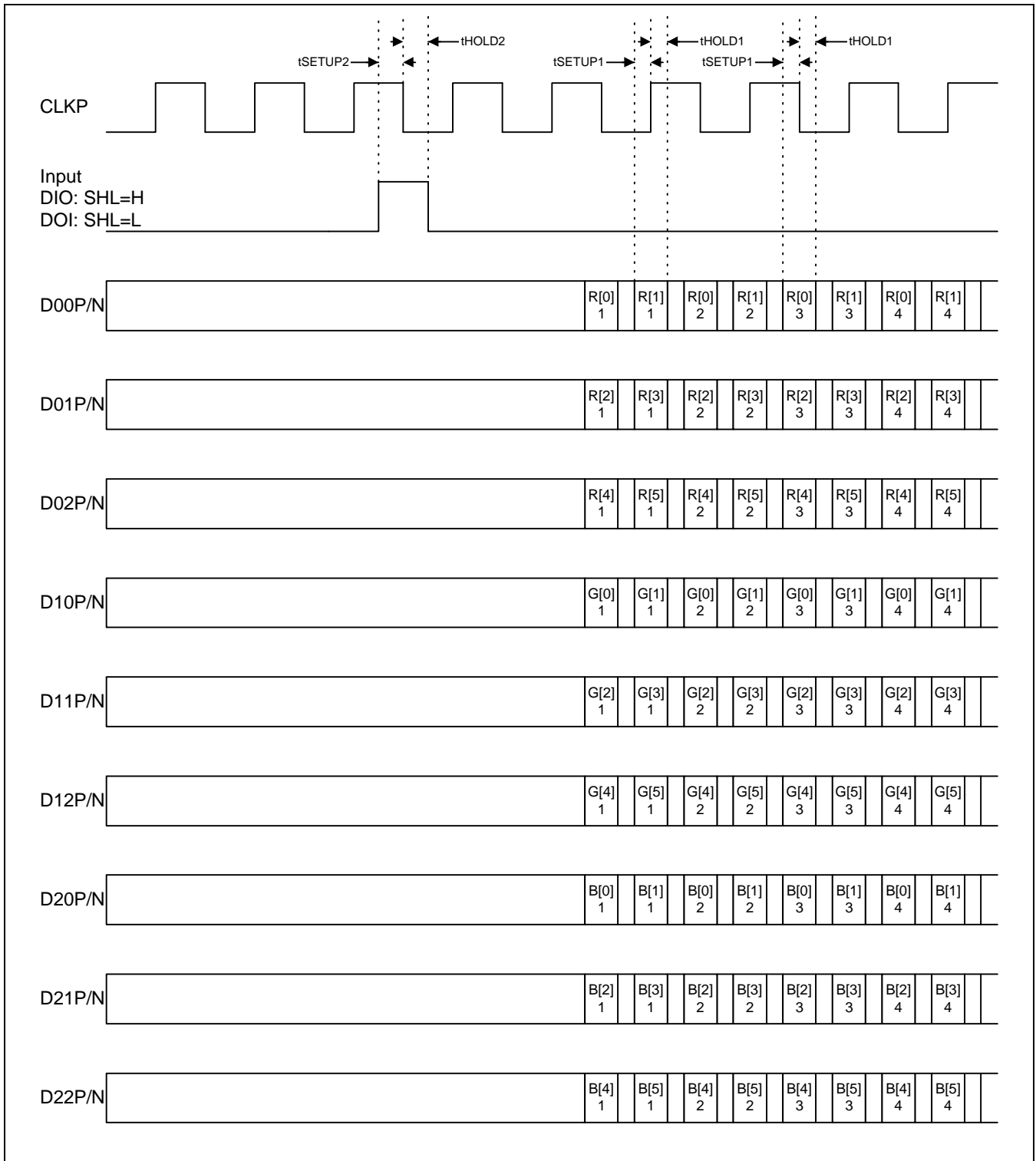


Figure 6. RSDS Data Timing Diagram