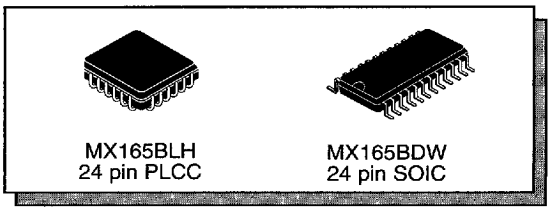
CTCSS ENCODER/DECODER
WITH TX/RX AUDIO FILTERS

FEATURES
- 39 CTCSS Tones + Notone
- TX/RX Audio Filters
- TX Tone Phase Reversals
- Serial or Parallel Programming
- Low Voltage Supply: 3.0 to 5.5 V

BENEFITS
- Scanning of any Channel
- Improved Sinad
- Squelch Tail Elimination
- Easy µP Interface

APPLICATIONS
- Mobile Radio Channel Sharing
- Wireless Intercom
- TIA/EIA-603 - 37 Tone Plus 97.4Hz & 69.3Hz
- Serves 3-Cell Applications



Description

Voice on shared radio channels is multiplexed with a subaudible CTCSS tone as a means of directing messages among user groups sharing the same RF frequency. Continuous Tone Controlled Squelch System (CTCSS) modulates the transmitter with a discrete tone, taken from a field of 39 in the range of 67 to 250 Hz, according to TIA/EIA-603 Standard plus 69.3Hz and 97.4Hz. Groups of radio receivers, segregated by common interest and assigned tone, demodulate the voice/tone mixture for voice messages to be heard.

The MX165B CTCSS Encoder/Decoder enhances voice/tone multiplexing with an on-chip filter that attenuates TX speech 36dB at 250Hz, while passing signals >300Hz with only ±1dB of ripple.

Early CTCSS designs did not filter TX speech, depending instead on the host transmitter's pre-emphasis network. At only 6dB/octave, their attenuation of speech components at the higher CTCSS tones was only a few dB, which resulted in "talk-off" (low frequency voice components unsquelching the receiver audio).

The MX165B features TX/RX selection and a LOAD/LATCH pin. A Notone program code has been included to permit scanning channels without CTCSS. A choice of serial or parallel tone programming is offered. Operation of the PTL signal during TX reverses the phase of the transmitted CTCSS tone by 180°. This is used in some radios to eliminate squelch tails.

The MX165B requires a single 3.75- or 5-volt supply and a 1 MHz clock or crystal.

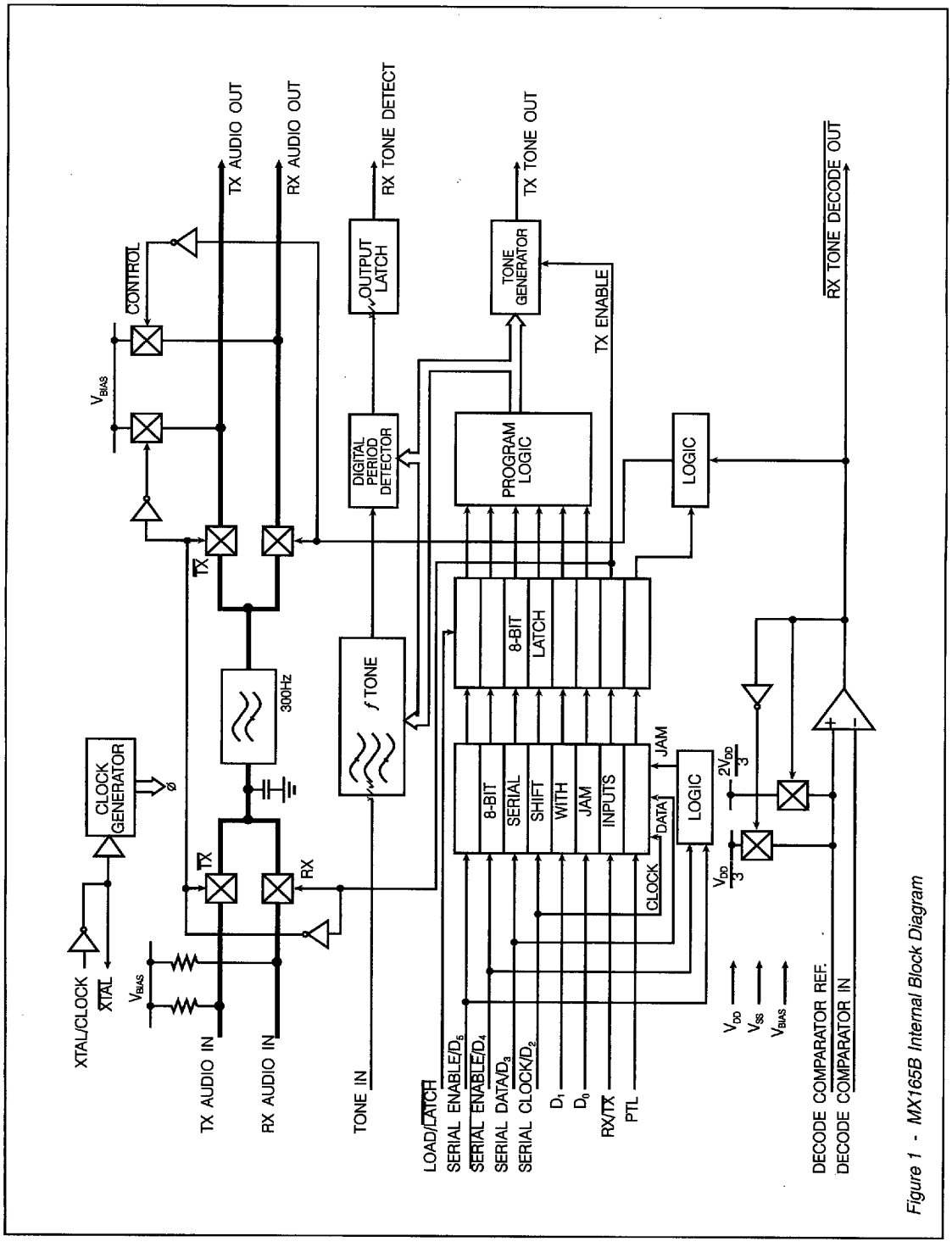


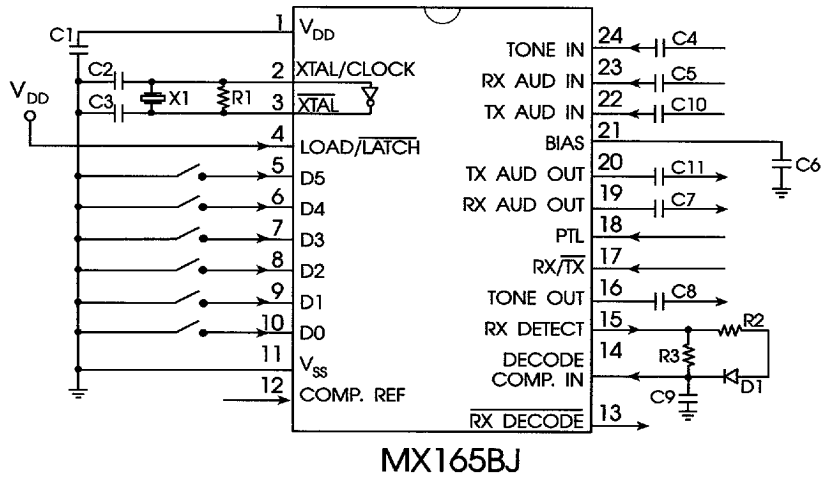
Figure 1 - MX165B Internal Block Diagram

PIN FUNCTION TABLE

Pin	Function
MX165A MX365A	
1	**V_{DD}:** Positive Supply.
2	**Xtal/Clock:** Input to the on-chip inverter used with a 1 MHz Xtal or external clock source.
3	**$\overline{\text{Xtal}}$:** Output of the on-chip inverter (clock output).
4	**Load/$\overline{\text{Latch}}$:** Controls 8 on-chip latches and is used to latch RX/TX, PTL, and D0-D5. This pin is internally pulled to V_{DD}. A logic "1" applied to this input puts the 8 latches in "transparent" mode. A logic "0" applied to this input puts the 8 latches in the "latched" mode. In parallel mode data is loaded and latched by a logic 1-0 transition (see Fig. 3). In serial mode data is loaded and latched by a 0-1-0 strobe pulse on this pin (see Fig. 4).
5	**D5/Serial Enable 1:** Data input D5 (in parallel mode). A logic "1" applied to this input together with a logic "0" applied to D4/Serial Enable 2 will put the device in serial mode (see Fig. 4). This pin is internally pulled to V_{DD}.
6	**D4/$\overline{\text{Serial Enable 2}}$:** Data input D4 (in parallel mode). A logic "0" applied to this input together with a logic "1" on pin 5 will place the device in serial mode (see Fig. 5). This pin is internally pulled to V_{DD}.
7	**D3/Serial Data Input:** Data input D3 (in parallel mode). In serial mode this pin becomes the serial data input for D5-D0, RX/TX and PTL (see Fig. 4). D5 is clocked first and PTL last. This pin is internally pulled to V_{DD}.
8	**D2/Serial Clock:** Data input D2 (in parallel mode). In serial mode this pin becomes the serial clock input. Data is clocked on the positive going edge (see Fig. 4). This pin is internally pulled to V_{DD}.
9	**D1:** Data input D1 (in parallel mode). This pin is internally pulled to V_{DD}.
10	**D0:** Data input D0 (in parallel mode). This pin is internally pulled to V_{DD}.
11	**V_{SS}:** Negative supply.
12	**Decode Comparator Ref.:** This pin is internally biased to $V_{DD}/3$ or $2V_{DD}/3$ via 1M resistors depending on the logical state of the RX Tone Decode Out pin. RX Tone Decode Out = 1 will bias this input $2V_{DD}/3$; a logic "0" will bias this input $V_{DD}/3$. This input provides the decode comparator reference voltage, and switching of bias voltages provides hysteresis to reduce "chatter" under marginal conditions.
13	**$\overline{\text{RX Tone Decode Out}}$:** This is the gated output of the decode comparator. This output is used to gate the RX Audio path. A logic "0" on this pin indicates a successful decode and that the Decode Comparator Input pin is more positive than the Decode Comparator Ref. input (see Table 1).
14	**Decode Comparator Input:** This is the inverting input of the decode comparator. This pin is normally connected to the integrated output of the RX Tone Detect line.
15	**RX Tone Detect:** In RX mode this output will go to logic "1" during a successful decode. It must be externally integrated to control response and deresponse times (see Table 1).
16	**TX Tone Out:** The CTCSS sinewave output appears on this pin under control of the RX/$\overline{\text{TX}}$ pin. This pin, when not transmitting a tone, may be biased to V_{DD}-0.7V or O/C (see Table 1). This pin is an emitter follower output with high impedance load, requiring capacitive coupling or a low impedance (<1kΩ) load to ground.

PIN FUNCTION TABLE

Pin	Function
17	**RX/$\overline{TX}$:** This input (in parallel mode) selects RX or TX modes (see Fig. 2). In serial mode this function is serially loaded. This pin is internally pulled to V_{DD} via a 1MΩ resistor.
18	**PTL:** In parallel RX mode this pin operates as a "Push To Listen" function by enabling the RX audio path, thus overriding the tone squelch function. In parallel TX mode this pin reverses the phase of the transmitted CTCSS tone (used for squelch tail elimination). In serial mode this function is serially loaded (see Fig. 2).
19	**RX Audio Out:** This is the high pass filtered receive audio output pin. This pin outputs audio when RX Tone Decode = 0, or PTL = 1, or when Notone is programmed (see Table 2). In TX mode this pin is biased to $V_{DD}/2$.
20	**TX Audio Out:** This is the high pass filtered transmit audio output pin. In TX mode this pin outputs audio present at the TX Audio Input pin. In RX mode this pin is biased to $V_{DD}/2$.
21	**Bias:** This pin is the output of an internally generated $V_{DD}/2$ bias level and would normally be externally decoupled to V_{SS} via capacitor C7.
22	**TX Audio In:** This is the TX Audio input pin. In TX mode it may be prefiltered, using the TX audio path, thus helping to aviod talkoff due to intermodulation of speech frequencies with the transmitted CTCSS tone. This pin is internally biased to $V_{DD}/2$.
23	**RX Audio In:** This is the input to the audio high pass filter in RX mode. It is internally biased to $V_{DD}/2$.
24	**Tone Input:** This is the input to the CTCSS tone detector. It is internally biased to $V_{DD}/2$.
	NOTE: Pins labeled "N/C" (no connect) may have internal connections. Do Not Use.



Component Values

R1	1MΩ
R2	560kΩ
R3	820kΩ
X1	1MHz
C1	0.1µF
C2	68pF
C3	33pF
C4	0.1µF
C5	0.1µF
C6	0.47µF
C7	0.1µF
C8	0.1µF
C9	0.1µF
C10	0.1µF
C11	0.1µF
D1	small signal

Tolerances: Resistors: ±10%
Capacitors: ±20%
Xtal: ±0.1%

Figure 2 - External Component Diagram

I/O CONDITIONS

	INPUT PIN CONDITION			OUTPUT PIN CONDITION		RESULT/FUNCTION					
D0-D5	RX/$\overline{TX}$	PTL	Decode Comp. Input	RX Tone Detect	$\overline{Tone}$ Decode	Tone Transmitter Enabled	TX Tone Phase Reversed	TX Audio Path Enabled	Tone Decoder Enabled	RX Audio Path Enabled	Notes
Tone	0	0	X	0	1	Yes	No	Yes	No	No (bias)	1a
Tone	0	1	X	0	1	Yes	Yes	Yes	No	No (bias)	1b
No tone	0	X	X	0	1	No (bias)	X	Yes	No	No (bias)	2
Tone	1	0	0	0	1	No (o/c)	X	No	Yes	No (bias)	3a
Tone	1	1	0	0	1	No (o/c)	X	No	Yes	Yes	3b
Tone	1	X	1	1	0	No (o/c)	X	No	Yes	Yes	4
No tone	1	X	X	X	0	No (o/c)	X	No	Yes	Yes	5

Table 1 - Combinations of Input/Output Conditions

o/c = open circuit
X = don't care

Notes:

1a. Normal tone transmit condition.
1b. Tone transmit with phase reversed.
2 Notone programmed in TX mode, tone transmit O/P set to $V_{DD}/2$ - 0.7V. TX audio path enabled.
3a. Normal decode standby.
3b. Normal decode standby with PTL used to enable audio.
4. Normal decode of correct CTCSS tone condition, PTL has no effect.
5. Notone programmed in RX mode, tone transmit O/P (o/c). RX audio path enabled.

FILTER RESPONSE

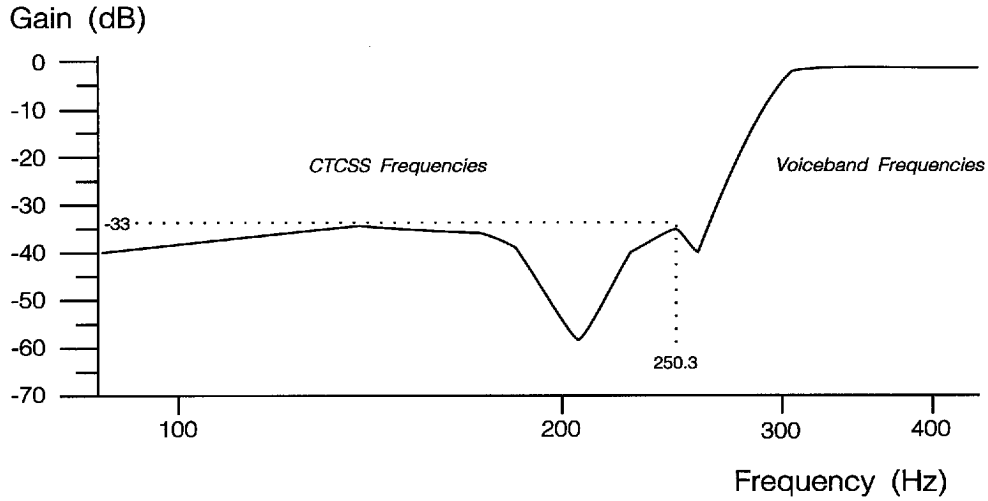
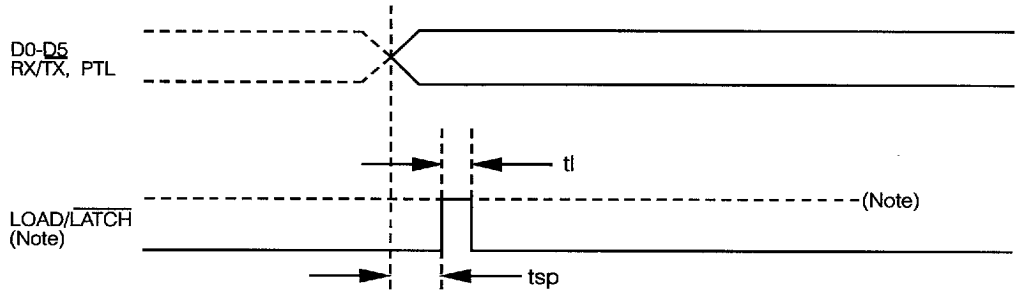


Figure 3 - Voiceband Filter Response

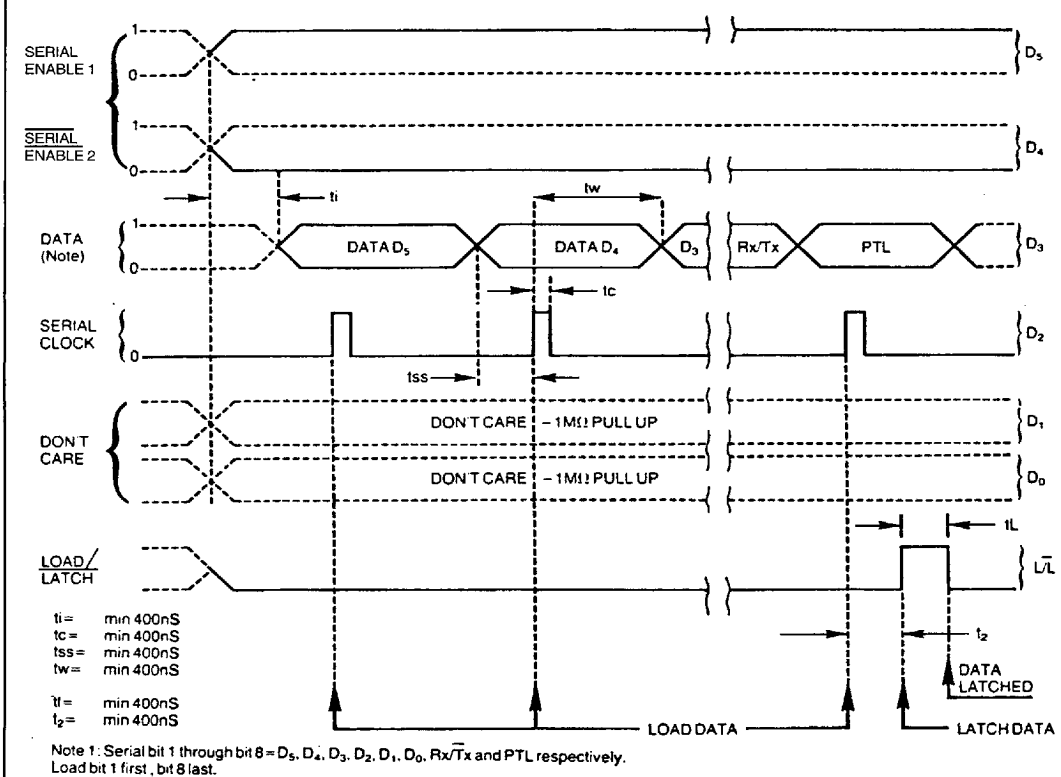
SERIAL AND PARALLEL MODE TIMING



Note: For wired, non microprocessor applications Load/Latch should be connected to V_{DD}.

tl min. = 400ns
tsp min. = 400ns

Figure 4 - Parallel Mode (not to scale)



Note 1: Serial bit 1 through bit 8 = D_5, D_4, D_3, D_2, D_1, D_0, $Rx/\overline{Tx}$ and PTL respectively.
Load bit 1 first, bit 8 last.

Figure 5 - Serial Mode (not to scale)

CTCSS PROGRAMMING TABLE

Tone			Programming Inputs						
Nominal Frequency (Hz)	MX165B Freq. (Hz)	△fo (%)	D5	D4	D3	D2	D1	D0	Hex
67.0	67.05	+0.07	1	1	1	1	1	1	3F
69.3	69.32	+.03	1	1	1	0	0	1	39
71.9	71.9	0	0	1	1	1	1	1	1F
74.4	74.35	-0.07	1	1	1	1	1	0	3E
77.0	76.96	-0.05	0	0	1	1	1	1	0F
79.7	79.77	+0.09	1	1	1	1	0	1	3D
82.5	82.59	+0.1	0	1	1	1	1	0	1E
85.4	85.38	-0.2	1	1	1	1	0	0	3C
88.5	88.61	+0.13	0	0	1	1	1	0	0E
91.5	91.58	+0.09	1	1	1	0	1	1	3B
94.8	94.76	-0.04	0	1	1	1	0	1	1D
97.4	97.29	-0.11	1	1	1	0	1	0	3A
100.0	99.96	-0.04	0	0	1	1	0	1	0D
103.5	103.43	-0.07	0	1	1	1	0	0	1C
107.2	107.15	-0.05	0	0	1	1	0	0	0C
110.9	110.77	-0.12	0	1	1	0	1	1	1B
114.8	114.64	-0.14	0	0	1	0	1	1	0B
118.8	118.8	0	0	1	1	0	1	0	1A
123.0	122.8	-0.17	0	0	1	0	1	0	0A
127.3	127.08	-0.17	0	1	1	0	0	1	19
131.8	131.67	-0.10	0	0	1	0	0	1	09
136.5	136.61	+0.08	0	1	1	0	0	0	18
141.3	141.32	+0.02	0	0	1	0	0	0	08
146.2	146.37	+0.12	0	1	0	1	1	1	17
151.4	151.09	-0.2	0	0	0	1	1	1	07
156.7	156.88	+0.11	0	1	0	1	1	0	16
162.2	162.31	+0.07	0	0	0	1	1	0	06
167.9	168.14	+0.14	0	1	0	1	0	1	15
173.8	173.48	-0.19	0	0	0	1	0	1	05
179.9	180.15	+0.14	0	1	0	1	0	0	14
186.2	186.29	+0.05	0	0	0	1	0	0	04
192.8	192.86	+0.03	0	1	0	0	1	1	13
203.5	203.65	+0.07	0	0	0	0	1	1	03
210.7	210.17	-0.25	0	1	0	0	1	0	12
218.1	218.58	+0.22	0	0	0	0	1	0	02
225.7	226.12	+0.18	0	1	0	0	0	1	11
233.6	234.19	+0.25	0	0	0	0	0	1	01
241.8	241.08	-0.30	0	1	0	0	0	0	10
250.3	250.28	-0.01	0	0	0	0	0	0	00
Notone		N/A	1	1	0	0	0	0	30
Serial Input Mode		N/A	1	0	Data	Clock	X	X	2X
Test	4082	N/A	1	1	0	0	1	1	33 or any invalid address

Table 2 - CTCSS Tones

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not suggested.

Supply Voltage	-0.3 to 7.0 V
Input Voltage at any pin (ref V_{SS} = 0V)	-0.3 V to V_{DD} + 0.3 V
Sink/Source Current	
(supply pins)	±30mA
(other pins)	±20mA
Maximum Device Dissipation	100mW
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C

OPERATING LIMITS

All devices were measured under the following conditions unless otherwise noted.

V_{DD} = 3.75V
T_{AMB}=25°C
Xtal/Clock f_0 = 1.0 MHz
0dB ref. = 100mVrms @ 1kHz

Composite signal: 1kHz test tone at 300 mVrms, 75 mVrms noise (band limited 6kHz gaussian white noise), 30 mVrms CTCSS tone.

2

Characteristics	See Note	Min.	Typ.	Max.	Unit
STATIC VALUES					
Supply Voltage		3.0	3.75	5.5	V
Supply Current					
TX		-	-	3.5	mA
RX		-	-	3.5	mA
Tone Input Impedance		-	1	-	MΩ
Tone Output Impedance		-	4	-	kΩ
Audio Input Impedance		-	1	-	MΩ
Audio Output Impedance		-	1	-	kΩ
Digital Input Impedance	1	-	1	-	MΩ
Input logic"1"	1	70%V_{DD}	-	-	V
Input logic "0"	1	-	-	30%V_{DD}	V
Logic "1" output 1' source = 0.1mA	2	80%V_{DD}	-	-	V
Logic "0" output 1' sink - 0.1mA	2	-	-	20%V_{DD}	V
DYNAMIC VALUES					
Decoder					
Decode Input Signal Level	3	30	-	-	mVrms
Decode Response Time	3,6,10	-	-	250	ms
Deresponse Time	3,6,10	-	180	250	ms
Decode Selectivity (see Fig. 6)	3,12	±0.5	-	-	%f_0

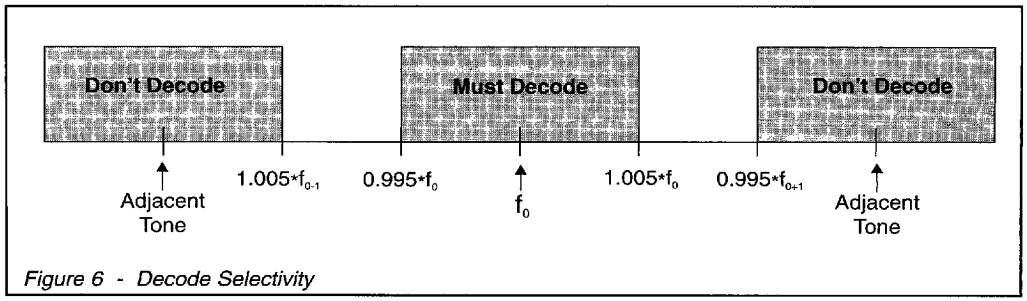


Figure 6 - Decode Selectivity

Characteristics	See Note	Min.	Typ.	Max.	Unit
Encoder					
Tone Output Level		400	627	800	mVrms
Tone Frequency Accuracy (f error)		-0.3	-	+0.3	$\%f_0$
Risetime to 90% nominal O/P:					
f_0>100Hz	4,10	-	55	-	ms
f_0<100Hz	4,10	-	70	-	ms
Tone Output Load Current		-	-	5	mA
Total Harmonic Distortion		-	2	5	%
Output Level Variation Between Tones	11	-1.0	-	+1.0	dB
TX Output Impedance		-	2.0	-	kΩ
Audio Filter					
Total Harmonic Distortion	5,10	-	2	5	%
Output Noise Level	8	-	2	-	mVrms
(input a.c. short circuit, audio switch enabled)					
Sinad	9	36	40	-	dB
Spurious Emissions	13	-	-48	-	dB
Cutoff Frequency	7	-	300	-	Hz
Passband		300	-	3000	Hz
Bandpass Ripple		-	-	2	dB
Stopband Attenuation <250Hz	5,7	33	36	-	dB
Passband Gain 1kHz		-2.0	-	0.5	dB
Audio Switch					
Isolation	5	-	60	-	dB
Serial/Parallel Inputs (See Figures 3 &4)					
Parallel Set-up Time t_{SP}		400	-	-	ns
Load/Latch Pulse Width t_l		400	-	-	ns
Serial Clock Pulse Width t_c		400	-	-	ns
Serial Set-up Time t_{SS}		400	-	-	ns
Serial Clock Frequency		-	1	-	MHz

NOTES:

1. Refers to RX/TX, PTL, Decode Comparator Input, D0-D5.
2. All logic outputs.
3. Composite Signal Test Condition.
4. Any programming tone and RL = 10,000, CL = 15pF. This includes response to a phase reversal instruction.
5. 1kHz references = 0dB.
6. f_0>100Hz (for 100 Hz>f_0>67Hz: t = 100/f_0Hz x 250ms)
7. See Figure 3.
8. Measured in a 30kHz bandwidth.
9. Measured with an input level of 100 mV @ 1kHz, in a 30 kHz bandwidth.
10. Per TIA/EIA-603.
11. Ref. to 100 Hz.
12. Complies with TIA/EIA-603, must not decode adjacent fo ±0.5%.
13. Test system resolution is ≈ -35dB.