National Semiconductor

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INS1771-1 Floppy Disk Formatter/Controller

General Description

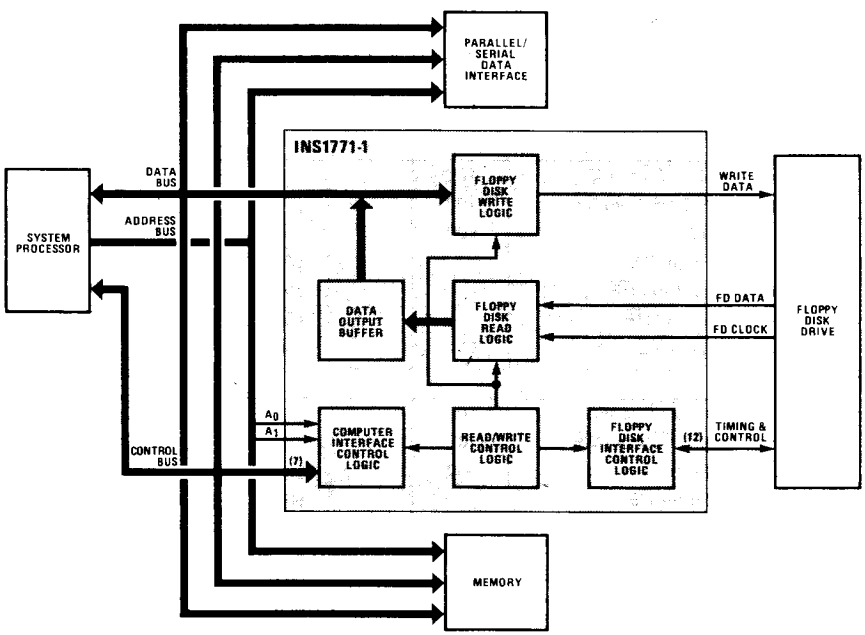
The INS1771-1 is a programmable floppy disk formatter/controller chip contained in a standard 40-pin dual-in-line package. The chip, which is fabricated using N-channel silicon gate technology, interfaces a floppy disk drive directly to a computer interface bus. The INS1771-1 provides soft sector formatting, which may be either IBM 3740 compatible or a user-selected sector format.

The INS1771-1 is designed to operate on a multiplexed, TRI-STATE® 8-bit bidirectional bus with other bus-oriented devices. The chip is programmed by the system software via the bus and all data, status information, and control words are transferred over the bus lines.

Features

- Soft Sector Format Compatibility
- Automatic Track Seek with Verification
- Provisions for Miniature Floppy Disk Interface
- Read Mode Capabilities
  - Single/Multiple Record Read with Automatic Sector Search or Entire Track Read
  - Selectable 128-Byte or Variable Record Length
- Write Mode Capabilities
  - Single/Multiple Record Write with Automatic Sector Search
  - Entire Track Write for Diskette Initialization
- Programmable Controls
  - Selectable Track-to-Track Stepping Time
  - Selectable Head Settling and Head Engage Times
  - Selectable Three Phase or Step and Direction and Head Positioning Motor Controls
- Double Buffering of Data
- TTL Compatible
- DMA or Programmed Data Transfers
- Reduces System Component Count
- On-Chip CRC Generation and Checking
- Direct Plug-in Replacement for Western Digital FD1771-1

INS1771-1 General System Configuration



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Absolute Maximum Ratings

V_{DD} with Respect to V_B . . . . . +20 V to −0.3 V
Max Voltage to Any Input with Respect to V_{BB} . . . +20 V to −0.3 V
Operating Temperature. . . . . 0°C to +70°C
Storage Temperature . . . . . −55°C to +125°C

Note: Maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under dc electrical characteristics.

DC Electrical Characteristics

T_A = 0°C to +70°C, V_{DD} = +12.0 V ± 0.6 V, V_{BB} = −5.0 V ± 0.25 V, V_{SS} = 0 V, V_{CC} = +5 V ± 0.25 V, I_{DD} = 10 mA nominal, I_{CC} = 30 mA nominal, I_{BB} = 0.4 nA nominal.

Symbol	Characteristic	Min	Typ	Max	Unit	Conditions
I_{LI}	Input Leakage			10	μA	$V_{IN} = V_{DD}$
I_{LO}	Output Leakage			10	μA	$V_{OUT} = V_{DD}$
V_{IH}	Input High Voltage	2.6			V	
V_{IL}	Input Low Voltage (All Inputs)			0.8	V	
V_{OH}	Output High Voltage	2.8			V	I_O = −100 μA
V_{OL}*	Output Low Voltage			0.45	V	I_O = 1.6 mA

Note: $V_{OL} \leq 0.4$ V when interfacing with low-power Schottky parts ($I_O < 1$ mA).

*V_{OL} = 0.5 V on WG.

AC Electrical Characteristics

T_A = 0°C to +70°C, V_{DD} = +12 V ± 0.6 V, V_{BB} = −5 V ± 0.25 V, V_{SS} = 0 V, V_{CC} = +5 V ± 0.25 V.

Symbol	Characteristic	Min	Typ	Max	Unit	Conditions
Read Operations						
t_{ET}	Setup ADDR & $\overline{CS}$ to $\overline{RE}$	100			ns	
t_{HLD}	Hold ADDR & $\overline{CS}$ from $\overline{RE}$	10			ns	
t_{RE}	$\overline{RE}$ Pulse Width	500			ns	C_L = 25 pF
t_{DRR}	DRQ Reset from $\overline{RE}$			500	ns	
t_{IRR}	INTRQ Reset from $\overline{RE}$			3000	ns	
t_{DACC}	Data Access from $\overline{RE}$			450	ns	C_L = 25 pF
t_{DOH}	Data Hold from $\overline{RE}$	50		150	ns	C_L = 25 pF
Write Operations						
t_{SET}	Setup ADDR & $\overline{CS}$ to $\overline{WE}$	100			ns	
t_{HLD}	Hold ADDR & $\overline{CS}$ from $\overline{WE}$	10			ns	
t_{WE}	$\overline{WE}$ Pulse Width	350			ns	
t_{DRR}	DRQ Reset from $\overline{WE}$			500	ns	
t_{IRR}	INTRQ Reset from $\overline{WE}$			3000	ns	(see note)
t_{DS}	Data Setup to $\overline{WE}$	250			ns	
t_{DH}	Data Hold from $\overline{WE}$	150			ns	

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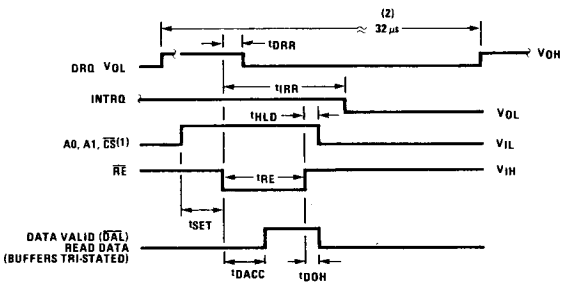
AC Electrical Characteristics (cont.)

T_A = 0°C to +70°C, V_{DD} = +12 V ± 0.6 V, V_{BB} = −5 V ± 0.25 V, V_{SS} = 0 V, V_{CC} = +5 V ± 0.25 V.

Symbol	Characteristic	Min	Typ	Max	Unit	Conditions
External Data Separation ($\overline{XTDS}$ = 0)						
t_{PWX}	Pulse Width Rd Data & Rd Clock	150		350	ns	
t_{CX}	Clock Cycle Ext	2500			ns	
t_{DEX}	Data to Clock	500			ns	
t_{DDX}	Data to Data Cycle	2500			ns	
Internal Data Separation ($\overline{XTDS}$ = 1)						
t_{PWI}	Pulse Width Data & Clock	150		1000	ns	
t_{CI}	Clock Cycle Internal	3500		5000	ns	
Write Data Timing						
t_{WGD}	Write Gate to Data		1200		ns	300 ns ± CLK tolerance
t_{PWW}	Pulse Width Write Data	500		600	ns	
t_{CDW}	Clock to Data		2000		ns	±0.5% ± CLK tolerance
t_{CW}	Clock Cycle Write		4000		ns	±0.5% ± CLK tolerance
t_{WGH}	Write Gate Hold to Data	0		100	ns	
Miscellaneous Timing						
t_{CD1}	Clock Duty	175			ns	2 MHz ± 1% (see note)
t_{CD2}	Clock Duty	210			ns	
t_{STP}	Step Pulse Output	3800		4200	ns	
t_{DIR}	Dir Setup to Step	24			µs	
t_{MR}	Master Reset Pulse Width	10			µs	These times doubled when CLK = 1 MHz
t_{IP}	Index Pulse Width	10			µs	
t_{WF}	Write Fault Pulse Width	10			µs	

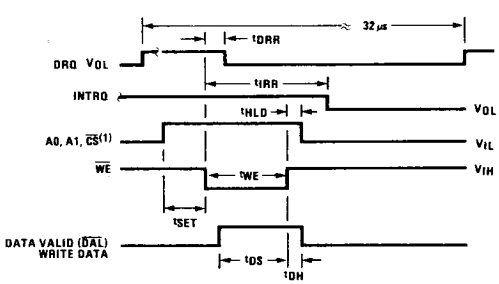
Note: Timings are given for 2 MHz Clock. For those timings noted, values will double when chip is operated at 1 MHz.

Timing Waveforms



NOTES:
1. $\overline{CS}$ MAY BE PERMANENTLY TIED LOW IF DESIRED.
2. FOR READ TRACK COMMAND, THIS TIME MAY BE 12 TO 32 µs WHEN $\overline{T}$ = 0. (THIS TIME DOUBLES WHEN CLK = 1 MHz.)

Read Enable Timing



NOTES:
1. $\overline{CS}$ MAY BE PERMANENTLY TIED LOW IF DESIRED.
2. WHEN WRITING DATA INTO SECTOR, TRACK, OR DATA REGISTER, USER CANNOT READ THIS REGISTER UNTIL AT LEAST 8 µs AFTER THE RISING EDGE OF WE. WHEN WRITING INTO THE COMMAND REGISTER, STATUS IS NOT VALID UNTIL SOME 12 µs LATER. THESE TIMES ARE DOUBLED WHEN CLK = 1 MHz.

Write Enable Timing

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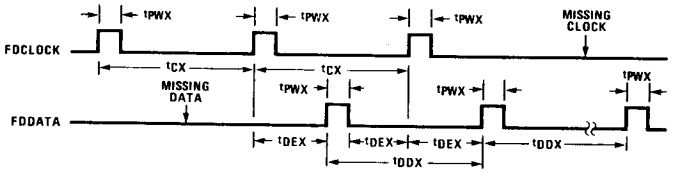
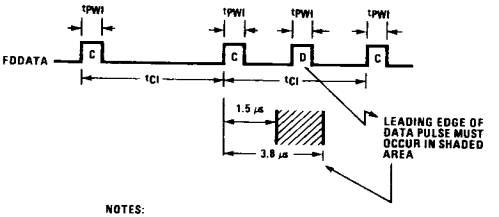
Timing Waveforms (cont.)



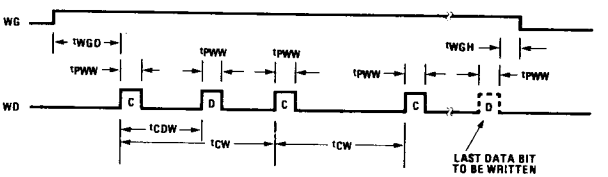
NOTES:
1. ABOVE TIMES ARE DOUBLED WHEN CLK = 1 MHz.
2. CONTACT NSC FOR EXTERNAL CLOCK/DATA SEPARATOR CIRCUITS.

Read Timing ($\overline{XTDS}$ = 0)

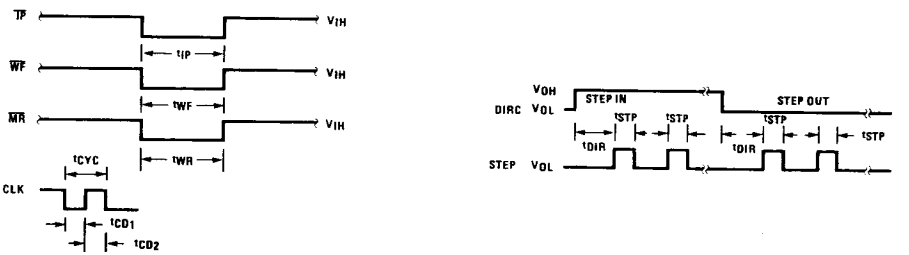


NOTES:
1. INTERNAL DATA SEPARATION MAY WORK FOR SOME APPLICATIONS. HOWEVER, FOR APPLICATIONS REQUIRING HIGH DATA RECOVERY RELIABILITY, NSC RECOMMENDS THAT EXTERNAL DATA SEPARATION BE USED.
2. FDCLOCK MUST BE TIED HIGH.

Read Timing ($\overline{XTDS}$ = 1)



Write Data Timing



Miscellaneous Timing

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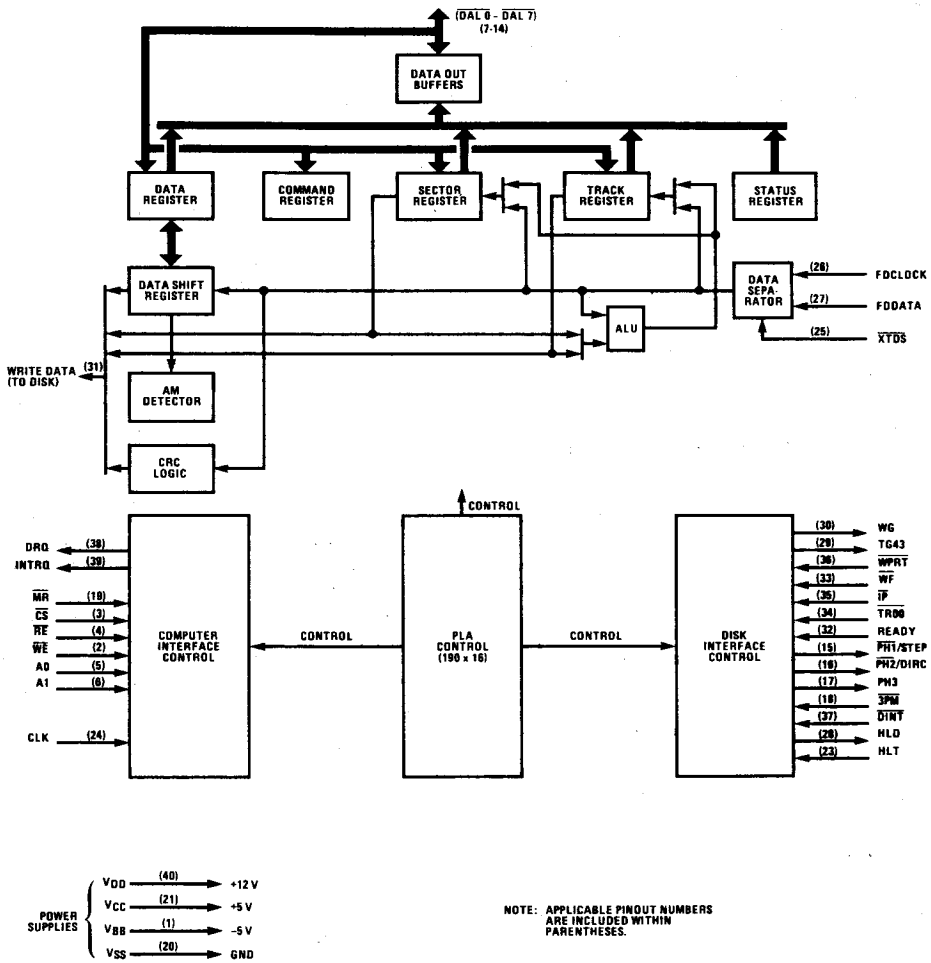
INS1771-1 Block Diagram



NOTE: APPLICABLE PINOUT NUMBERS ARE INCLUDED WITHIN PARENTHESES.

INS1771-1 Functional Pin Definitions

The following describes the function of all INS1771-1 input/output pins. Some of these descriptions reference internal circuits.

NOTE

In the following descriptions, a low represents a logic 0 (0 Volt nominal) and a high represents a logic 1 (+5 Volts nominal).

INPUT SIGNALS

Chip Select ($\overline{CS}$): When low, the chip is selected. This enables communication between the INS1771-1 and the CPU.

Read Enable ($\overline{RE}$): When low coincident with an active (low) $\overline{CS}$ input, allows the CPU to read data or status information from a selected register of the chip.

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Functional Pin Definitions (cont.)

Write Enable ($\overline{WE}$): When low coincident with an active (low) $\overline{CS}$ input, allows the CPU to write data or control words into a selected register of the chip.

Register Select (A_0, A_1) Lines: These two inputs are used in conjunction with either an active (low) $\overline{RE}$ or $\overline{WE}$ input to select an INS1771-1 register to read from or write into as indicated below.

A_1	A_0	$\overline{RE}$	$\overline{WE}$	Selected Register
0	0	0	1	Status Register
0	0	1	0	Command Register
0	1	0	1	Track Register
0	1	1	0	
1	0	0	1	Sector Register
1	0	1	0	
1	1	0	1	Data Register
1	1	1	0	

Master Reset ($\overline{MR}$): When low, clears the Command Register, resets bit 7 (Not Ready) of the Status Register low, and makes the $\overline{PH1}$/STEP output active low. When the $\overline{MR}$ returns high, a Restore command is executed (regardless of the state of the Ready input from the floppy disk drive).

Clock (CLK): This input pin requires a 2-megahertz (±1%) squarewave clock as a reference for all internal timing.

NOTE

For a miniature floppy disk, a 1-MHz (±1%) squarewave clock is required.

External Data Separator ($\overline{XTDS}$): When low, the composite read disk serial data (data bits and clock) from the floppy disk drive is separated externally by the user. When high or open, the composite read disk data is separated by the internal data separator of the chip.

Floppy Disk Data (FDDATA): This input pin provides either of the following serial data: both clock and data bits (composite read disk data) when the $\overline{XTDS}$ input is high; or externally separated data bits when the $\overline{XTDS}$ input is low.

Floppy Disk Clock (FDCLK): This input pin provides the externally separated clock when the $\overline{XTDS}$ input is low. The FDCLK input should be connected to +5 Volts (logic 1) when the $\overline{XTDS}$ input is high.

Write Protect ($\overline{WPRT}$): When low, immediately terminates a Write command and sets bit 6 (Record Type/Write Protect) of the Status Register high. In addition, an interrupt is generated when the $\overline{WPRT}$ input is low. The $\overline{WPRT}$ input is sampled whenever a Write command is received from the CPU.

Write Fault ($\overline{WF}$): When low coincident with an active (high) Write Gate (WG) output, causes the current Write command to be terminated and sets bit 5 (Record Type/Write Fault) of the Status Register high. The $\overline{WF}$ input should be made inactive (high) coincident with an inactive (low) WG output. If not used, tie high.

Index Pulse ($\overline{IP}$): Goes low for 10 microseconds (minimum) whenever an index mark is encountered (once per revolution) on the diskette.

Track 00 ($\overline{TR00}$): Goes low whenever the Read/Write head is positioned over track 00 of the diskette.

Ready: When high before the execution of a Read or Write command, indicates that the floppy disk drive is ready for a Read or Write operation. When low, the Read or Write operation is not performed and an interrupt is generated. However, a Seek operation is always performed. The complement of the Ready input appears as bit 7 (Not Ready) of the Status Register.

Three-Phase Motor Select ($\overline{3PM}$): When low, the three-phase motor control interface is selected for the floppy disk drive by the INS1771-1. When high or open, the step-direction motor control interface is selected by the INS1771-1.

Disk Initialization ($\overline{DINT}$): When low coincident with a Write Track command from the CPU, causes the Write Track operation to be terminated and bit 6 (Record Type/Write Protect) of the Status Register to be set high.

Test: This input pin is normally tied to +5 Volts. However, it may be used to disable the programmed stepping rate delays for testing the INS1771-1 or for disk drives that do not require the long delay times to change tracks. These delays are disabled by tying the Test input to ground.

Head Load Timing (HLT): When high, the Read/Write head is assumed to be engaged against the recording medium (diskette). The HLT input is sampled after each 10 millisecond internal delay after HLD is asserted.

V_{BB}: −5 Volt supply.

V_{CC}: +5 Volt supply.

V_{DD}: +12 Volt supply.

V_{SS}: Ground (0 Volt) reference.

OUTPUT SIGNALS

Data Request (DRQ): Open-drain output to the CPU that goes high when the INS1771-1 is ready to transfer a byte of data during a Read or Write operation. The DRQ output is reset low upon the completion of a byte Read or Write operation.

Interrupt Request (INTRQ): Open-drain output to the CPU that goes high at the completion or termination of any operation. The INTRQ output is reset low when a new command is loaded into the Command Register, or Status Register Read.

Write Data (WD): Composite write disk data (both clock and data bits of 500 nanoseconds in duration) output to the floppy disk drive. The WD output can drive two TTL loads.

Write Gate (WG): Active (high) whenever data is to be written on the diskette. As a precaution to erroneous writing, the first data byte must be loaded into the Data Register (in response to a DRQ output from the INS1771-1) before the WG output can be activated.

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Functional Pin Definitions (cont.)

Track Greater Than 43 (TG43): When high during a Read or Write operation, informs the floppy disk drive that the Read/Write head is positioned between tracks 44 and 76.

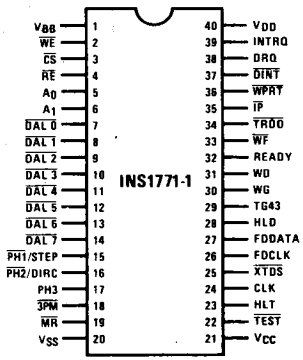
Three-Phase Motors/Step-Direction Motors Control Lines ($\overline{PH1}$/STEP, $\overline{PH2}$/DIRC, PH3): These three control lines provide either of the following outputs: successive three-phase pulses (active high PH3 signal and active low $\overline{PH1}$ and $\overline{PH2}$ signals) over the lines for three-phase stepping motors; or a level over the $\overline{PH2}$/DIRC line (high level for stepping in and low level for stepping out) and 4 microsecond high-level pulses over the $\overline{PH1}$/STEP line to determine the direction and stepping rate for step-direction motors. For direction control of three-phase motors, the stepping sequence is 1-2-3-1 when stepping in and 1-3-2 when stepping out. The particular motor interface selected is determined by the hardwiring of the $\overline{3PM}$ input. The $\overline{PH1}$/STEP output is made active low after a master reset.

Head Load (HLD): High-level output that controls the loading of the Read/Write head against the recording medium (diskette). A Read or Write operation does not occur until a high-level HLT input is sampled by the INS1771-1. The HLD becomes active at the beginning of a Read, Write (E flag is set high) or Verify operation, or a Seek or Step Operation with the H flag set high; it remains active until the third index pulse following the last operation that used the head.

INPUT/OUTPUT SIGNALS

Data Access Lines (DAL) Bus: This TRI-STATE bus comprises eight inverted input/output lines ($\overline{DAL0}$ - $\overline{DAL7}$). The bus provides bidirectional communications between the CPU and the INS1771-1. Data, control words and status information are transferred via the DAL Bus.

Pin Configuration



INS1771-1 Commands

The INS1771-1 accepts and executes the eleven commands listed and summarized in table 1. Flags associated with these commands are summarized in table 2. With the exception of the Force Interrupt command, a command word should be loaded into the internal Command Register only when bit 0 (Busy) of the Status Register is inactive (low). Whenever a command is being executed, the Busy status bit is set high. When a command is completed or an error condition exists, an interrupt is generated and the Busy status bit is reset low. The Status Register indicates whether a completed command encountered an error or was fault free.

As indicated in table 1, the eleven commands accepted and executed by the INS1771-1 are divided into four types. The following paragraphs describe the eleven commands under these four divisions.

TYPE I COMMANDS

Type I Commands are basically head positioning commands and include the Restore, Seek, Step, Step-In, and Step-Out commands. Each of the Type I Commands contains a rate (r_1r_0) field (bits 0 and 1) that determines the stepping motor rate as defined in the table below:

The Type I Commands contain a head load (h) flag (bit 3) that determines whether or not the head is to be loaded at the beginning of the command. If h = 1, the head is loaded at the beginning of the command (HLD output made active high). If h = 0, the HLD output is made inactive low. Once the head is loaded (HLD is active), the head will remain engaged until the INS1771-1 receives a command that specifically disengages the head. If the INS1771-1 does not receive any commands after two revolutions of the disk, the head will be disengaged (HLD made inactive). The Head Load Timing (HLT) input is only sampled after a 10 millisecond delay, when actual reading or writing on the diskette is to occur. Note that a verification, described below, requires reading off the diskette.

The Type I Commands also contain a verification (V) flag (bit 2) that determines whether or not verification is to take place on the last track. If V = 0, no verification is performed. If V = 1, a verification is performed.

During verification, the head is loaded (HLD is active) and after an internal 10 millisecond delay, the HLT input is sampled. When the HLT input is active (high),

r_1	r_0	CLK = 2 MHz TEST = 1	CLK = 1 MHz TEST = 1	CLK = 2 MHz TEST = 0	CLK = 1 MHz TEST = 0
0	0	6 ms	12 ms	≈ 400 μs	≈ 800 μs
0	1	6 ms	12 ms		
1	0	10 ms	20 ms		
1	1	20 ms	40 ms		

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Table 1. Commands Summary

Type	Command	Bits							
		7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	u	h	V	r_1	r_0
I	Step In	0	1	0	u	h	V	r_1	r_0
I	Step Out	0	1	1	u	h	V	r_1	r_0
II	Read Command	1	0	0	m	b	E	0	0
II	Write Command	1	0	1	m	b	E	a_1	a_0
III	Read Address	1	1	0	0	0	E	0	0
III	Read Track	1	1	1	0	0	E	0	$\bar{s}$
III	Write Track	1	1	1	1	0	E	0	0
IV	Force Interrupt	1	1	0	1	I_3	I_2	I_1	I_0

Table 2. Command Flags Summary

h = Head Load flag (bit 3 of Type I)

h = 1, Load head at beginning
h = 0, Do not load head at beginning

V = Verify flag (bit 2 of Type I)

V = 1, Verify on last track
V = 0, No verify

r_1r_0 = Stepping Motor Rate (bits 1 - 0 of Type I)

r_1r_0 = 00, 6 ms between steps
r_1r_0 = 01, 6 ms between steps
r_1r_0 = 10, 10 ms between steps
r_1r_0 = 11, 20 ms between steps

u = Update flag (bit 4 of Type I)

u = 1, Update Track Register
u = 0, No update

m = Multiple Record flag (bit 4 of Type II)

m = 0, Single Record
m = 1, Multiple Records

b = Block Length flag (bit 3 of Type II)

b = 1, IBM format (128 to 1024 bytes)
b = 0, Non-IBM format (16 to 4096 bytes)

E = Enable HLD & 10 ms delay (bit 2 of Type II)

E = 1, Enable HLD, HLT & 10 ms delay
E = 0, Head is assumed engaged & no 10 ms delay

a_1a_0 = Data Address Mark (bits 1 - 0 of Type II)

a_1a_0 = 00, FB (Data Mark)
a_1a_0 = 01, FA (Data Mark)
a_1a_0 = 10, F9 (Data Mark)
a_1a_0 = 11, F8 (Data Mark)

$\bar{s}$ = Synchronize flag (bit 0 of Type III)

$\bar{s}$ = 0, Synchronize to AM
$\bar{s}$ = 1, Do not synchronize to AM

I_n = Interrupt Condition flags (bits 3 - 0 of Type IV)

I_0 = 1, Not Ready to Ready Transition
I_1 = 1, Ready to Not Ready Transition
I_2 = 1, Index Pulse
I_3 = Immediately

INS1771-1 Commands (cont.)

the first encountered ID field is read off the diskette. The track address of the ID field is then compared to the Track Register. If there is a match and a valid ID CRC, the verification is complete, an interrupt is generated, and the Busy status bit is reset. If there is not a match and a valid ID CRC, an interrupt is generated, the Seek Error status bit (bit 4) is set high, and the Busy status bit is reset low. If there is not a valid CRC, the CRC Error status bit (bit 3) is set high, and the next encountered ID field is read off the diskette for verification. If an ID field with a valid CRC cannot be found after four revolutions of the diskette, the INS1771-1 terminates the operation and sends an interrupt (INTRQ) signal to the CPU.

The Step, Step-In and Step-Out commands contain an update (u) flag (bit 4). When u = 1, the Track Register is updated by one for each step. When u = 0, the Track Register is not updated.

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Restore (Seek Track 0): Upon receipt of this command, the Track 00 ($\overline{TR00}$) input is sampled. If $\overline{TR00}$ is active low (indicating the Read/Write head is positioned over track 0), the Track Register is loaded with zeros and an interrupt is generated. If $\overline{TR00}$ is not active low, stepping pulses at a rate specified by the r_1r_0 field (bits 0 and 1) are issued until the $\overline{TR00}$ input is active low. At this time, the Track Register is loaded with zeros and an interrupt is generated. If the $\overline{TR00}$ input does not go active low after 255 stepping pulses, the INS1771-1 gives up and interrupts with the Seek Error status bit set. Note that the Restore command is executed when the $\overline{MR}$ input goes from an active (low) to an inactive (high) state. A verification operation takes place if the V flag (bit 2) is set. The setting of the h flag (bit 3) allows the head to be loaded at the start of the command.

Seek: This command assumes that the Track Register contains the track number of the current position of the Read/Write head and that the Data Register contains the desired track number. The INS1771-1 will update the Track Register and issue stepping pulses in the appropriate direction until the contents of the Track Register are equal to the contents of the Data Register. A verification operation takes place if the V flag (bit 2) is set. The setting of the h flag (bit 3) allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

Step: Upon receipt of this command, the INS1771-1 issues one stepping pulse to the floppy disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the r_1r_0 field (bits 0 and 1), a verification takes place if the V flag (bit 2) is set. If the u flag (bit 4) is set, the Track Register is updated. The setting of the h flag (bit 3) allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

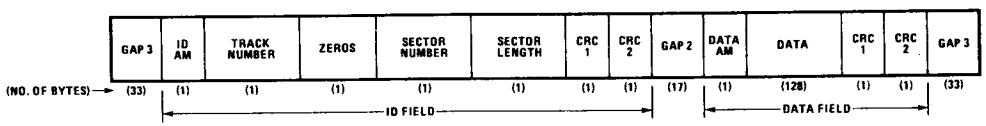
Step-In: Upon receipt of this command, the INS1771-1 issues one stepping pulse in the direction towards track 76. If the u flag (bit 4) is set, the Track Register is decremented by one. After a delay determined by the r_1r_0 field (bits 0 and 1), a verification takes place if the V flag (bit 2) is set. The setting of the h flag (bit 3) allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

Step-Out: Upon receipt of this command, the INS1771-1 issues one stepping pulse in the direction towards track 0. If the u flag (bit 4) is set, the Track Register is decremented by one. After a delay determined by the r_1r_0 field (bits 0 and 1), a verification takes place if the V flag (bit 2) is on. The setting of the h flag (bit 3) allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

TYPE II COMMANDS

The Type II Commands include the Read sector(s) and Write sector(s) commands. Prior to loading the Type II Commands into the Command Register, the computer must load the Sector Register with the desired sector number. Upon receipt of the Type II Commands, the Busy status bit is set. If the E flag (bit 2) = 1 (this is the normal case), HLD is made active and HLT is sampled after an internal 10 millisecond delay. If the E flag = 0, the head is assumed engaged and there is no internal 10 millisecond delay.

When an ID field (see figure 1) is located on the diskette, the INS1771-1 compares the Track Number of the ID field with the Track Register. If there is not a match, the next encountered ID field is read and a comparison is made. If there is a match, the sector number of the ID field is then compared with the Sector Register. If there is not a match, the next encountered ID field is read and a comparison is made. If there is a match, the CRC field is read. (The polynomial for the CRC is $G(x) = x^{16} + x^{12} + x^5 + 1$. The CRC includes all the information starting with the address mark and up to the CRC characters.) If there is a CRC error, the CRC Error status bit is set and the next ID field is read off the diskette and comparisons are made. If the CRC is correct, the data field is located and will be either written or read, depending upon command. The INS1771-1 must find an ID field with a valid track number, sector number, and CRC within four revolutions of the diskette; otherwise, the Record Not Found status bit (bit 4) is set and the command is terminated with an interrupt.



IDAM = ID ADDRESS MARK; DATA = (FE), CLK = (C7)
DATA AM = DATA ADDRESS MARK; DATA = (F8, F9, FA, OR FB), CLK = (C7)

Figure 1. IBM 3740 ID Field and Data Field Formats

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Each of the Type II Commands contains a b flag (bit 3), which in conjunction with the sector length field contents of the ID, determines the length (number of characters) of the data field. For IBM 3740 compatibility, the b flag (bit 3) should equal 1. The numbers of bytes in the data field (sector) is then 128×2^n where n = 0, 1, 2, or 3.

For b = 1:

Sector Length Field (hex)	Number of Bytes in Sector (decimal)
00	128
01	256
02	512
03	1024

When the b flag (bit 3) equals zero, the sector length field (n) multiplied by 16 determines the number of bytes in the sector or data field as shown below:

For b = 0:

Sector Length Field (hex)	Number of Bytes in Sector (decimal)
01	16
02	32
03	48
04	64
•	•
•	•
•	•
FF	4080
00	4096

Each of the Type II Commands also contains an m flag (bit 4) that determines whether multiple records (sectors) are to be read or written, depending upon the command. If m = 0, a single sector is read or written and an interrupt is generated at the completion of the command. If m = 1, multiple records are read or written with the Sector Register internally updated so that an address verification can occur on the next record. The INS1771-1 continues to read or write multiple records and update the Sector Register until the Sector Register exceeds the number of sectors on the track or until the Force Interrupt command is loaded into the Command Register. When either of these occurs, the command is terminated and an interrupt is generated.

Read Command: Upón receipt of this command, the Read/Write head is loaded and the Busy status bit is set. Then, when an ID field is encountered that has the correct track number, correct sector number, and correct CRC, the data field is inputted to the computer. The Data Address Mark of the data field must be found within 28 bytes of the correct ID field. If not, the Record Not Found status bit is set and the operation is terminated. When the first character or byte of the data field has been shifted through the Data Shift Register, it is transferred to the Data Register and a Data Request (DRQ) output is generated. When the next byte is loaded into the Data Shift Register, it is transferred to the Data Register and another DRQ output is generated, provided that the CPU has previously read the Data Register. If one or more characters are lost, the Lost Data status bit is set. This sequence continues until the data field has been inputted to the computer. If there is a CRC error in the data field, the CRC Error status bit is set, and the command is terminated (even if it is a multiple record command). At the end of the operation, the type of Data Address Mark encountered in the data field is recorded in the Status Register (bits 5 and 6) as shown below:

Status Bit 5	Status Bit 6	Data AM (hex)
0	0	FB
0	1	FA
1	0	F9
1	1	F8

Write Command: Upon receipt of this command, the Read/Write head is loaded (HLD active) and the Busy status bit is set. When an ID field is encountered that has the correct track number, correct sector number, and correct CRC, a DRQ output is generated. The INS1771-1 counts off 11 bytes from the CRC field and the Write Gate (WG) output is made active if the DRQ is serviced (i.e., the Data Register has been loaded by the computer). If DRQ has not been serviced, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, the WG is made active and six bytes of all Zero levels are then written on the diskette. At this time, the Data Address Mark is then written on the diskette, as determined by the a_1a_0 field (bits 0 and 1) of the command as shown below:

a_1	a_0	Data Mark (hex)	Clock Mark (hex)
0	0	FB	C7
0	1	FA	C7
1	0	F9	C7
1	1	F8	C7

The INS1771-1 then writes the data field by generating DRQ outputs to the computer. If the DRQ is not serviced in time, the Lost Data status bit is set and a byte of zeros is written on the diskette. The command is not terminated. After the last data byte has been written on the diskette, the two-byte CRC is computed internally and written on the diskette followed by one byte of all One levels. WG is then made inactive.

TYPE III COMMANDS

Read Address: Upon receipt of this command, the head is loaded and the Busy status bit is set. The next encountered ID field is then read in off the diskette, and the six data bytes of the ID field are assembled and transferred to the Data Register, and a DRQ output is generated for each byte. (The six bytes of the ID field are shown in figure 1.)

Although the CRC characters are inputted to the computer, the INS1771-1 checks for validity and the CRC Error status bit is set if there is a CRC error. The Sector Address of the ID field is written into the Sector Register. At the end of the operation, an interrupt is generated and the Busy status bit is reset.

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INS1771-1 Commands (cont.)

Read Track: Upon receipt of this command, the head is loaded and the Busy status bit is set. Reading starts with the leading edge of the first encountered index mark and continues until the next index pulse. As each byte is assembled, it is transferred to the Data Register and the Data Request (DRQ) output is generated for each byte. No CRC checking is performed. Gaps are included in the input data stream. If the $\bar{s}$ flag (bit 0) of the command is a low, the accumulation of bytes is synchronized to each Address Mark encountered. Upon completion of the command, the interrupt is activated.

The INS1771-1 handles single density frequency modulated (FM) data. Each data cell is defined by clock pulses. A pulse recorded between clock pulses indicates the presence of a logic 1 bit; the absence of this pulse is interpreted as a logic 0 bit. The Address Marks for Index, ID, and Data are identified by a particular pattern not repeated in the remainder of the ID field or Data field. This is accomplished by reading patterns that are recorded with missing clock bits (logic 0) as shown below:

For initialization:

Write 2 CRC Characters	Data	1 1 1 1 0 1 1 1 = F7
	Clock	1 1 1 1 1 1 1 1 = FF
Index Address Mark	Data	1 1 1 1 1 1 0 0 = FC
	Clock	1 1 0 1 0 1 1 1 = D7
ID Address Mark	Data	1 1 1 1 1 1 1 0 = FE
	Clock	1 1 0 0 0 1 1 1 = C7
Data Address Mark	Data	1 1 1 1 1 0 1 1 = F9 - FB
	Clock	1 1 0 0 0 1 1 1 = C7
Deleted Data Address Mark	Data	1 1 1 1 1 0 0 0 = F8
	Clock	1 1 0 0 0 1 1 1 = C7
Spare	Data	1 1 1 1 1 1 0 1 = FD
	Clock	(user designated)

These patterns are used as synchronization codes by the INS1771-1 when reading data and are recorded by the formatting command (Write Track) when the INS1771-1 is presented with data F7 through FE.

Write Track: Upon receipt of this command, the head is loaded and the Busy status bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which time the interrupt is activated. The Data Request output is activated immediately upon receiving the command and writing does not start until after the first byte has been loaded into the Data Register. If the Data Register has not been loaded by the second index pulse, the operation is terminated. This sets the Not Busy and Lost Data status bits, and activates the interrupt. If a byte is not present in the Data Register when needed, a byte of zeros is substituted. Address Marks and CRC characters are written on the diskette by detecting certain data byte patterns in the outgoing data stream as shown above. The CRC generator is initialized to all Ones when any data byte from F8 to FE is about to be transferred from the Data Register to the Data Shift Register.

The Write Track command does not execute if the $\overline{DINT}$ input is grounded. Instead, the Write Protect status bit is set and the interrupt is activated. One F7 pattern in the Data Register generates 2 CRC characters.

TYPE IV COMMANDS

Force Interrupt: This command can be loaded into the Command Register at any time. If there is a current command under execution (Busy status bit is set), the command is terminated and an interrupt is generated when the condition specified in the I_0 through I_3 field (bits 0 through 3) is detected. More than one condition may be specified. The interrupt conditions are indicated below:

I_0 = Not Ready-to-Ready Transition
I_1 = Ready-to-Ready Transition
I_2 = Every Index Pulse
I_3 = Interrupt Occurs Immediately

NOTE

If I_0 through I_3 = 0, no interrupt is generated; however, the current command is terminated and the Busy status bit is reset.

INS1771-1 Status Register

An 8-bit register is provided in the INS1771-1 to hold device status information. This Status information varies according to the type of command executed as shown in table 3. The contents of the Status Register, which can be read into the DAL Bus by a Read operation, are described below.

Bit 0: When high (set), indicates that a command is under execution. When low (reset), indicates that no command is under execution.

Bit 1: For Type I Commands, this bit is the complement of the Index Pulse ($\overline{IP}$) input. When set, it indicates that an index mark has been detected on the diskette.

For Types II and III Commands, this bit is a copy of the Data Request (DRQ) output. When set, it indicates that the Data Register is full during a Read operation or that the Data Register is empty during a Write operation. Bit 1 is reset to zero when updated.

Bit 2: For Type I Commands, this bit is the complement of the Track 00 ($\overline{TR00}$) input. When set, it indicates that the Read/Write head is positioned over track 0.

For Types II and III Commands, this bit is set to indicate that the computer did not respond to the DRQ output from the INS1771-1 in one byte time. Bit 2 is reset to zero when updated.

Bit 3: For Type I Commands, this bit is set when one or more CRC errors were encountered on an unsuccessful Track Verification operation. Bit 3 is reset to zero when updated.

For Type II and III Commands, bit 3 is set when an error is found in one or more ID fields, while bit 4 is set. Bit 3 is reset low when updated.

Bit 4: For Type I Commands, this bit is set to indicate that the desired track was not verified. Bit 4 is reset low when updated.

For Type II and III Commands, bit 4 is set to indicate that the desired track and sector were not found. Bit 4 is reset low when updated.

Bit 5: For Type I Commands, this bit is set to indicate that the Read/Write head is loaded and engaged. Bit 5

D.3

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INS1771-1 Commands (cont.)

is the logical AND of the Head Load (HLD) output and the Head Load Timing (HLT) input.

For Type II and III Commands, bit 5 indicates the following: the LSB of the record-type code from the data field address mark during execution of a Read Command; and a write fault during execution of a Write or Write Track Command. Bit 5 is reset low when updated.

Bit 6: For Type I Commands, this bit is the complement of the Write Protect ($\overline{WRPT}$) input. When set, it indicates that the write protect is activated.

For Type II and III Commands, bit 6 indicates the following: the MSB of the record-type code from the data field address mark during execution of a Read Command; and a write fault during execution of a Write or Write Track command. Bit 6 is reset low when updated.

Bit 7: When set, indicates that the floppy disk drive is not ready. When reset, indicates that the drive is ready. Bit 7 is the complement of the Ready input and is logically ORed with the Master Reset ($\overline{MR}$) input. The Types II and III Commands are not executed unless the floppy disk drive is ready.

Table 3. Status Register Summary

Bit	Commands					
	All Type I Commands	Read Address	Read	Read Track	Write	Write Track
S7	Not Ready	Not Ready	Not Ready	Not Ready	Not Ready	Not Ready
S6	Write Protect	0	Record Type	0	Write Protect	Write Protect
S5	Head Engaged	0	Record Type	0	Write Fault	Write Fault
S4	Seek Error	ID Not Found	Record Not Found	0	Record Not Found	0
S3	CRC Error	CRC Error	CRC Error	0	CRC Error	0
S2	Track 0	Lost Data	Lost Data	Lost Data	Lost Data	Lost Data
S1	Index	DRQ	DRQ	DRQ	DRQ	DRQ
S0	Busy	Busy	Busy	Busy	Busy	Busy

Programming Examples

Some examples of the software control of the INS1771-1 are shown in flowchart form. The first example (figure 2) shows the writing of information onto a particular track and sector. The second example (figure 3) shows accessing of information from successive sectors. The third example (figure 4) shows how information may be sought by using Track 00 as a table of contents.

INS1771-1 Operation

The following describes the operation of the INS1771-1. Use the block diagram on page 5, as necessary, to follow these descriptions.

INS1771-1 PROCESSOR INTERFACE

All commands, status and data are transferred over the TRI-STATE bidirectional DAL (Data Access Lines) Bus. The 8 lines of the DAL Bus ($\overline{DAL0}$ - $\overline{DAL7}$) present an open circuit to the comman processor peripheral bus until activated by the low-level $\overline{CS}$ (Chip Select) signal. An active $\overline{CS}$ combined with a low-level $\overline{RE}$ (Read Enable) sets the DAL Bus into the transmitter mode, while the $\overline{CS}$ combined with a low-level $\overline{WE}$ (Write Enable) sets the DAL Bus in the receiver mode.

When transfer of data with the INS1771-1 is required by the host processor, the device address is decoded and $\overline{CS}$ is made low. The least significant address bits A1 and A0, combined with the signals $\overline{RE}$ during a Read operation or $\overline{WE}$ during a Write operation, are interpreted as selecting the following registers:

A1	A0	Read ($\overline{RE}$)	Write ($\overline{WE}$)
0	0	Status Register	Command Register
0	1	Track Register	Track Register
1	0	Sector Register	Sector Register
1	1	Data Register	Data Register

During Direct Memory Access (DMA) types of data transfers between the Data Register of the INS1771-1 and the processor, the Data Request (DRQ) output is used in Data Transfer control. This signal also appears as status bit 1 during Read and Write operations.

On Disk Read operations, the Data Request (DRQ) output is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more

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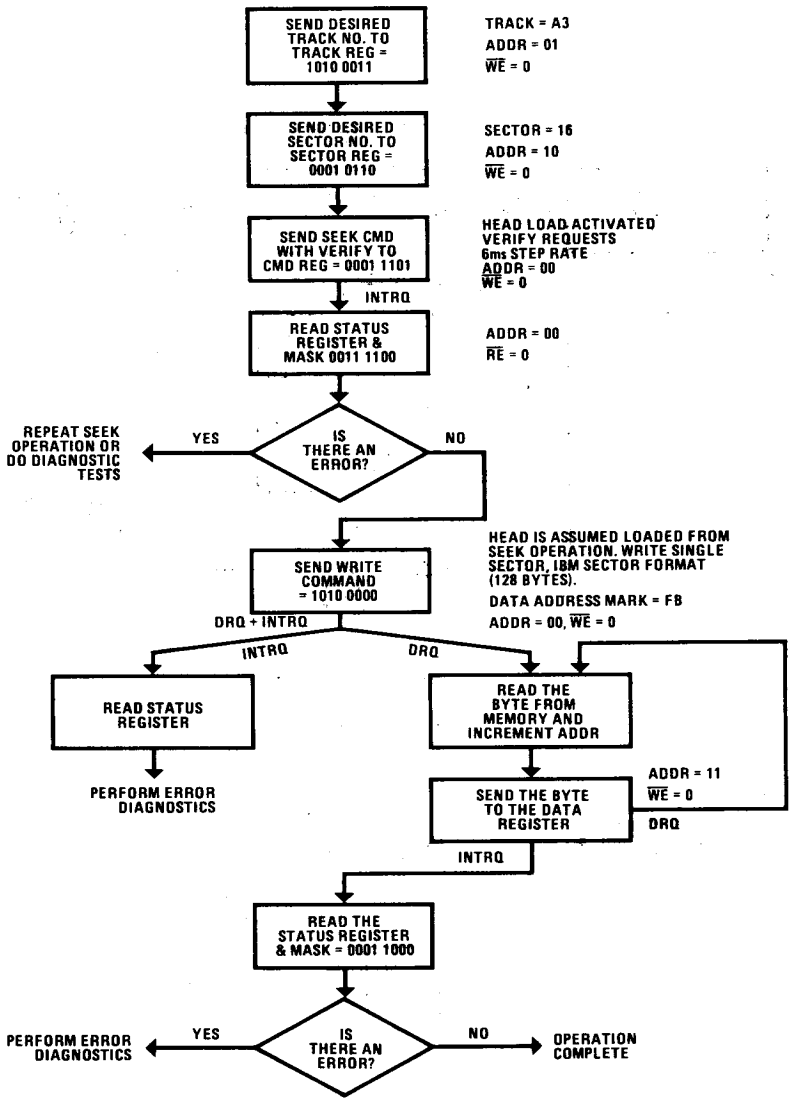

Figure 2. Writing Data

D.3

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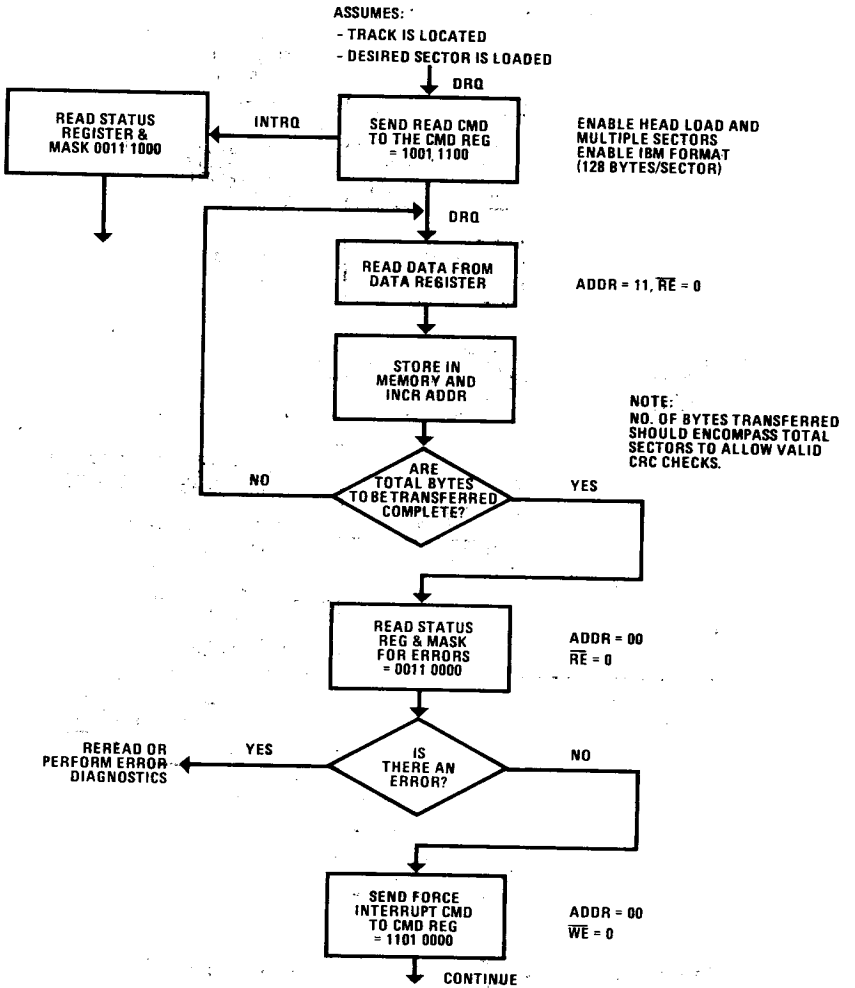

Figure 3. Reading Successive Sectors of Data

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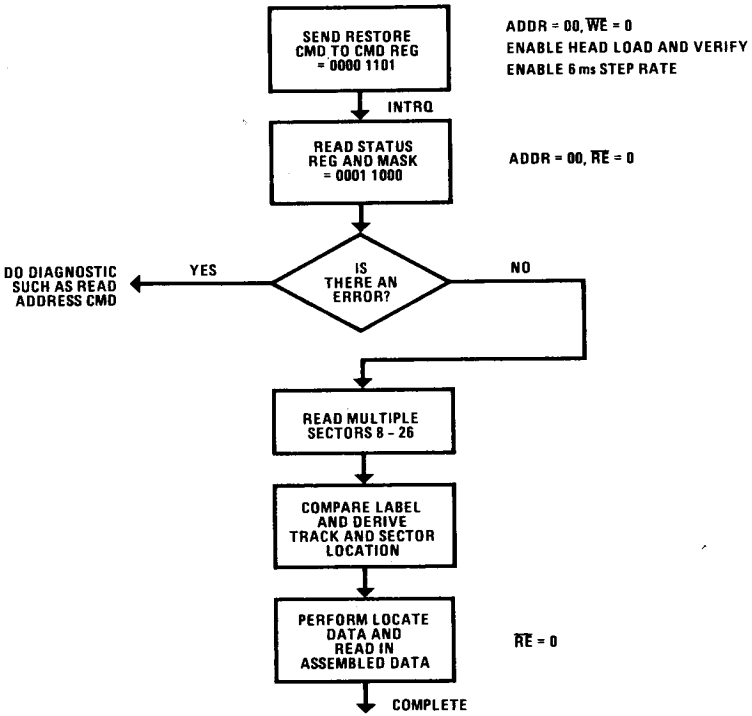

Figure 4. Using Track 00 as Table of Contents

characters are lost, by having new data transferred into the register prior to processor readout, the Lost Data bit is set in the Status Register. The Read operation continues until the end of sector is reached.

On Disk Write operations, the Data Request output is activated when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the floppy disk drive, a byte of zeroes is written on the diskette and the Lost Data bit is set in the Status Register.

The Lost Data bit and certain other bits in the Status Register will activate the Interrupt Request (INTRQ) output. The interrupt line is also activated with normal completion or abnormal termination of all controller operations. The INTRQ signal remains active until reset by reading the Status Register to the processor or by the loading of the Command Register. In addition, the INTRQ output is generated if a Force Interrupt command condition is met.

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INS1771-1 FLOPPY DISK DRIVE INTERFACE

The INS1771-1 floppy disk drive interface consists of head positioning controls, write gate controls, and data transfers. A 2.0 MHz ± 1% square wave clock is required at the CLK input for internal control timing. (A 1.0 MHz clock is required for a miniature floppy disk.)

Head Positioning

Four commands cause positioning of the Read/Write head (see INS1771-1 Commands section). The period of each positioning step is specified by the r field in bits 1 and 0 of the command word. After the last directional step, an additional 10 milliseconds of head settling time takes place. The four programmable stepping rates (r_1r_0) are tabulated under the Type I Commands description.

The r_1r_0 rates can be applied to a three-phase motor or a step-direction motor through the device interface. When the $\overline{3PM}$ input is connected to ground the device operates with a three-phase motor control interface, with one active signal per phase on the three output signals ($\overline{PH1}$, $\overline{PH2}$ and PH3). The stepping sequence is 1-2-3-1 when stepping in and 1-3-2-1 when stepping out. Phase 1 is active low after Master Reset.

The Step-Direction Motor Control interface is activated by leaving input $\overline{3PM}$ open or connecting it to +5 Volts. The phase 1 pin ($\overline{PH1}$) becomes a step pulse of 4 microseconds width. The phase 2 pin ($\overline{PH2}$) becomes a direction control, with a high voltage on this pin indicating a Step In, and a low voltage indicating a Step Out. The Direction output is valid a minimum of 24 microseconds prior to the activation of the step pulse.

When a Seek, Step or Restore command is executed, an optional verification of Read/Write head position can be performed by setting bit 2 in the command word to a logic 1. The verification operation begins at the end of the 10 millisecond settling time after the head is loaded against the medium. The track number from the first encountered ID Field is compared against the contents of the Track Register. If the track numbers compare and the ID Field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete. If track comparison is not made but the CRC checks, an interrupt is generated, the Seek Error status bit (bit 4) is set, and the Busy status bit is preset. If there is no track comparison nor a valid CRC, a step is made in the same direction as specified and the verify operation is repeated. The additional stepping can be repeated twice to account for two defective tracks. If no verification is received at this point, the Seek Error (bit 4) is set in the Status Register.

The Head Load (HDL) output controls the movement of the Read/Write head against the diskette for data recording or retrieval. It is activated at the beginning of a Read, Write (E flag on) or Verify operation, or a Seek or Step operation with the head load bit (h) a logic high; it remains activated until the third index pulse following the last operation which uses the Read/Write head. Reading or Writing does not occur until a minimum of 10 milliseconds after the HDL signal is made active. If executing the Type II Commands with the E flag off, there is no 10 millisecond delay and the head is assumed to be engaged. The delay is determined by sampling of the Head Load Timing (HLT) input every 10 milliseconds. A low logic state input, generated from the Head Load output transition and delayed externally, identifies engagement of the head against the diskette. In the Seek and Step commands, the head is loaded at the start of the command execution when the h bit is a logic 1. In a verify command, the head is loaded before stepping to the destination track on the diskette whenever the h bit is a logic 0.

Disk Read Operation

The 2.0 MHz external clock provided to the device is internally divided by 4 to form the 500 kHz clock rate for data transfer. When reading data from a diskette, this divider is synchronized to transitions of the Read Data (FDDATA) input. When a transition does not occur on the 500 kHz clock active state, the clock divider circuit injects a clock to maintain a continuous 500 kHz data clock. The 500 kHz data clock is further divided by 2 internally to separate the clock and information bits. The divider is phased to the information by the detection of the address mark.

In the internal data read and separation mode, the Read Data input toggles from one state to the opposite state for each logic 1 bit of clock or information. This signal can be derived from the amplified, differentiated, and sliced Read Head signal, or by the output of a flip-flop toggling on the Read Data pulses. This input is sampled by the 2 MHz clock to detect transitions.

The chip can also operate on externally separated data, as supplied by methods such as phase-lock loop, one-shots, or variable frequency oscillators. This is accomplished by grounding the External Data Separator ($\overline{XTDS}$) input. When the Read Data input makes a high-to-low transition, the information input to the FDDATA line is clocked into the Data Shift Register. The assembled 8-bit data from the Data Shift Register are then transferred to the Data Register.

The normal sector length for Read or Write operations with the IBM 3740 format is 128 bytes. This format or binary multiplex of 128 bytes will be adopted by setting a logic 1 in bit 3 of the Read Track and Write Track commands. Additionally, a variable sector length feature is provided which allows an indicator recorded in the ID Field to control the length of the sector. Variable sector lengths can be read or written in Read or Write commands respectively by setting a logic 0 in bit 0 of the command word. The sector length indicator specifies the number of 16-byte groups, or 16 x N, where N is equal to 1 to 256 groups. An indicator of all zeros is interpreted as 256 sixteen-byte groups.

Disk Write Operation

After data is loaded from the processor into the Data Register, and is transferred to the Data Shift Register, data will be shifted serially through the Write Data (WD) output. Interlaced with each bit of data is a positive clock pulse of 0.5 microsecond duration. This signal may be used to externally toggle a flip-flop to control the direction of write current flow.

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When writing is to take place on the diskette, the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing, the first data byte must be loaded into the Data Register in response to a Data Request from the INS1771-1 before the Write Gate signal can be activated.

Writing is inhibited when the Write Protect ($\overline{WPRT}$) input is a logic 0, in which case any Write command is immediately terminated, an interrupt is generated, and the Write Protect status bit is set. The Write Fault ($\overline{WF}$) input, when activated, signifies a writing fault condition detected in disk drive electronics such as failure to detect write current flow when the Write Gate (WG) is activated. On detection of this fault, the INS1771-1 terminates the current command and sets the Write Fault bit (bit 5) of the Status Register. The Write Fault ($\overline{WF}$) input should be made inactive when the Write Gate (WG) output becomes inactive.

Whenever a Read or Write command is received, the INS1771-1 samples the Ready input. If this input is logic 0, the command is not executed and an interrupt is generated. The Seek or Step commands are performed regardless of the state of the Ready input.

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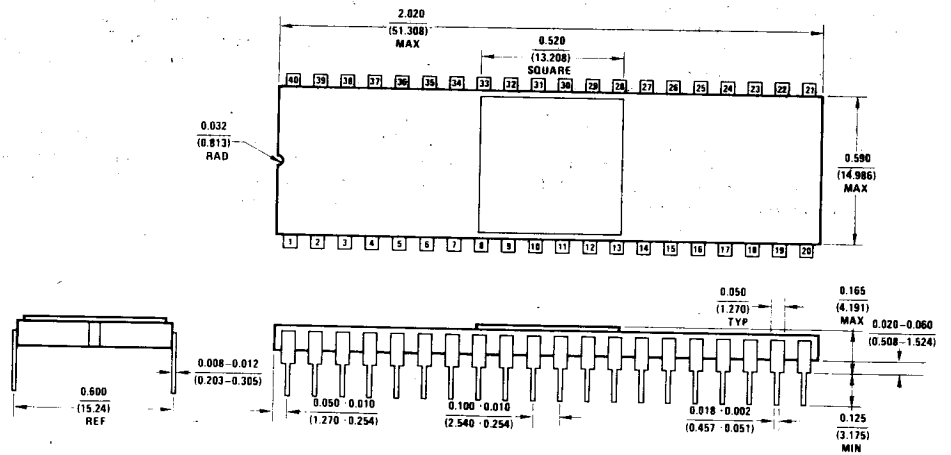
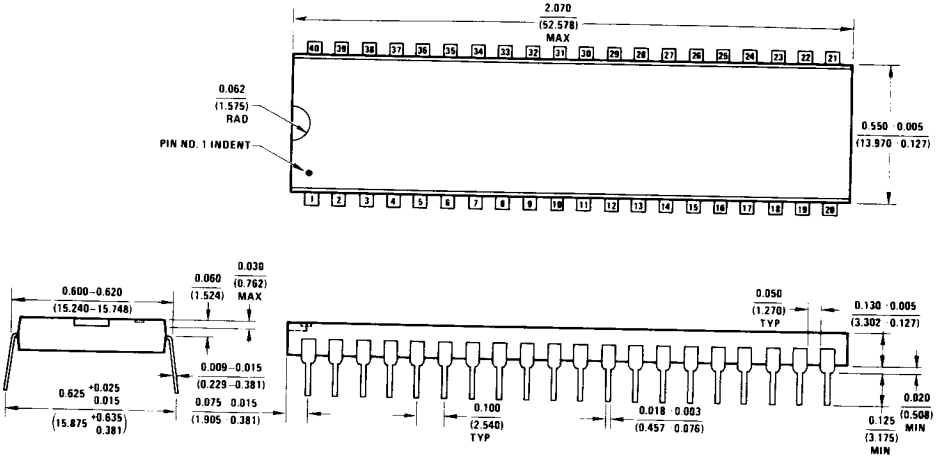
Physical Dimensions



Ceramic Dual-In-Line Package (D)
Order Number INS1771D-1
NS Package Number J40A



Plastic Dual-In-Line Package (N)
Order Number INS1771N-1
NS Package Number N40A

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