HD49219MP

T-77-21

16-bit A/D Controller

HD49219MP can be used to configure a serial interface 16-bit A/D converter for R-DAT and other digital audio systems, when used in combination with the HA12131MP or HA12132MP.

Functions

- A/D controller LSI for DAT and other digital audio equipment
- 2ch serial interface A/D converter can be configured in combination with one HA12131MP or one HA12132MP

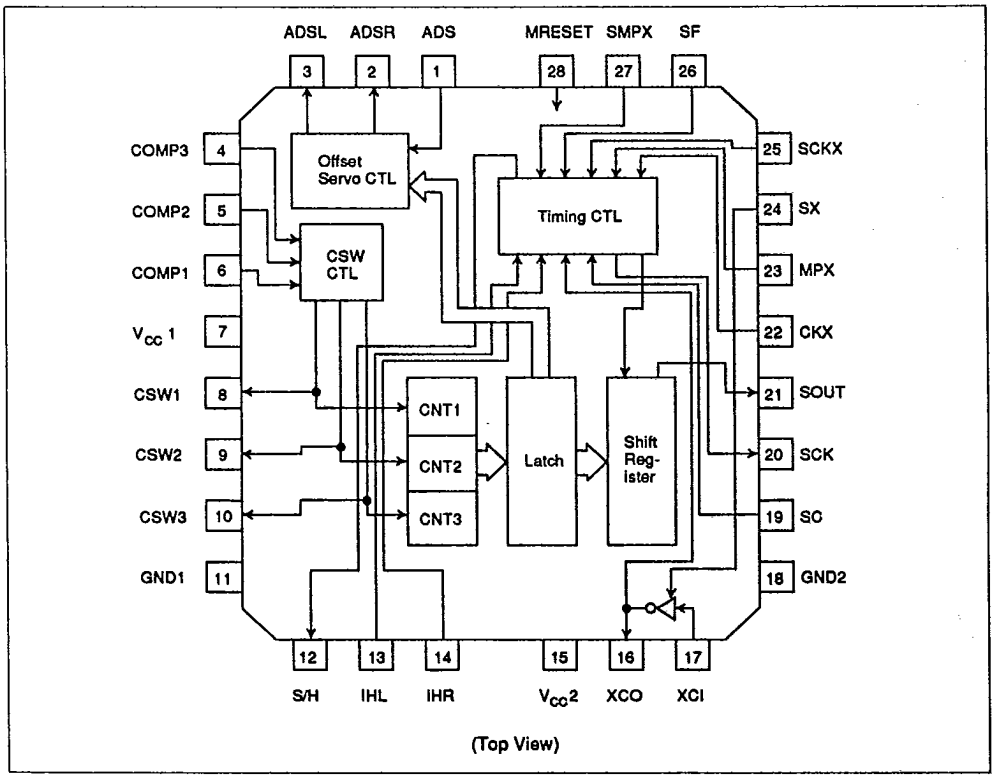
Features

- Two serial interface formats
- On-chip offset servo interface
- In combination with HA12131MP, configures a high-luminance serial interface 16-bit A/D converter
- In combination with HA12132MP, configures a 5V single source serial interface 16-bit A/D converter

Ordering Information

Type No.	Package
HD49219MP	MP-28

Pin Arrangement and Block Diagram



(Top View)

T-77-21

Pin Functions

Pin No.	Symbol	I	O	Connection Point	Function	L	H	Specification
1	ADS	O			Offset servo-switch	Duty 50%	ON	CR
2	ADSR		O	HA12131MP or HA12132MP	Offset servo Rch signal output			
3	ADSL		O	HA12131MP or HA12132MP	Offset servo Lch signal output			
4	COMP3	O		HA12131MP or HA12132MP	Comparator input 3			
5	COMP2	O		HA12131MP or HA12132MP	Comparator input 2			
6	COMP1	O		HA12131MP or HA12132MP	Comparator input 1			
7	$V_{CC}1$			+5V	Digital power supply			
8	CSW1		O	HA12131MP or HA12132MP	Current switch 1 signal output			
9	CSW2		O	HA12131MP or HA12132MP	Current switch 2 signal output			
10	CSW3		O	HA12131MP or HA12132MP	Current switch 3 signal output			
11	GND1			GND	A/D GND			
12	S/H		O	HA12131MP or HA12132MP	S/H signal output			
13	IHL	O			Lch output switch	OFF	ON	CR
14	IHR	O			Rch output switch	OFF	ON	CR
15	$V_{CC}2$			+5V	A/D power supply			
16	XCO		O	X'tal	Oscillation output terminal			
17	XCI	O		X'tal	Oscillation input terminal			
18	GND2			GND	Digital GND			
19	SC	O			System clock switch	1/3	1/6	CR
20	SCK		O	Signal processor LSI	System clock signal output			HS
21	SOUT		O	Signal processor LSI	Serial data signal output			CO
22	CKX	O		Signal processor LSI	Serial data clock			C
23	MPX	O		Signal processor LSI	Lch / Rch switch			C
24	SX	O		Microcomputer	Oscillation halt switch	OFF	ON	CR
25	SCKX	O			Serial mode switch	CKX17	CKX16	CR
26	SF	O		Microcomputer	fs switch	32kHz	48kHz	CR
27	SMPX	O			MPX mode switch	External	Internal	CR
28	MRESET	O			Master reset	Reset	Normal	CR

Functional Description

HD49219MP is a control LSI for HA12131MP and HA12132MP.

The HD49219MP/HA12131MP combination configures a high-luminance serial interface A/D converter, while the HD49219MP/HA12132MP combination forms a single supply 5V serial interface A/D converter. HA12131MP and HA12132MP include such analog functions as integration amplifier and sample hold amplifier, while HD49219MP includes integration period count logic. This distribution of processes allows the configuration of a low-dissipation serial interface A/D converter.

A/D Operation

HA12131MP and HA12132MP A/D conversion is performed using 3-segment cascade integration, the principle of which is illustrated in Figure 2. This method accumulates an electrical charge equivalent to the input voltage in a capacitor, and sequentially performs rough, medium and detailed integration using three fixed current supplies which are weighted in the ratio $2^{10} : 2^5 : 2^0$. Each period is counted and measured, and half of the sampling cycle is used for actual sampling, while integrating conversion is performed in the remaining half.

In the first half-cycle, an electrical charge equivalent to the input signal is accumulated in Ca (Figure 2), and then SW1 switches ON to start discharge by $2^{10}i3$. An the high order 6-bit counter counts until Vout becomes equal to Va, causing comparator C1 to invert. Next, SW1 switches OFF, SW2 switches ON and the middle 5-bit counter counts until Vout becomes equivalent to Vb. Finally, SW 2 switches OFF, SW3 switches ON and the low order 5-bit counter counts until Vout becomes equal to Vc.

Since the ratios of currents i1 through i3 are weighted in the ratio $2^{10} : 2^5 : 2^0$, arrangement of the counter output in series produces 16-bit A/D conversion data. The following is the formula for conversion of sampled analog voltage Vout:

$$Vout = (t1 \cdot 2^{10} i3 + t2 \cdot 2^5 i3 + t3 \cdot i3)/Ca$$

Xt + t1, Yt + t2, and Zt + t3 represent times that are integer multiples of the clock cycle (t = 1/36.864), and their counts are digital converted values. Actual conversion includes dead time caused by elimination of the range immediately following supply switching, in which integration characteristics and linearity are inferior. The Xt,. Yt, and Zt in Figure 2 actually includes dead time, and $t1 \times 2^{10} + t2 \times 2^5 + t3$ (t1 = integer in range of 0 to 63, t2 = integer in range of 0 to 31, t3 = integer in range of 0 to 31) are digital converted data. Aligning the 6-bit, 5-bit and 5-bit count data provides 16-bit digital data.

HD49219MP counts the CSW1 to CSW3 PWM signals and outputs two types of serial interface formats. Figure 3 shows the A/D conversion timing chart.

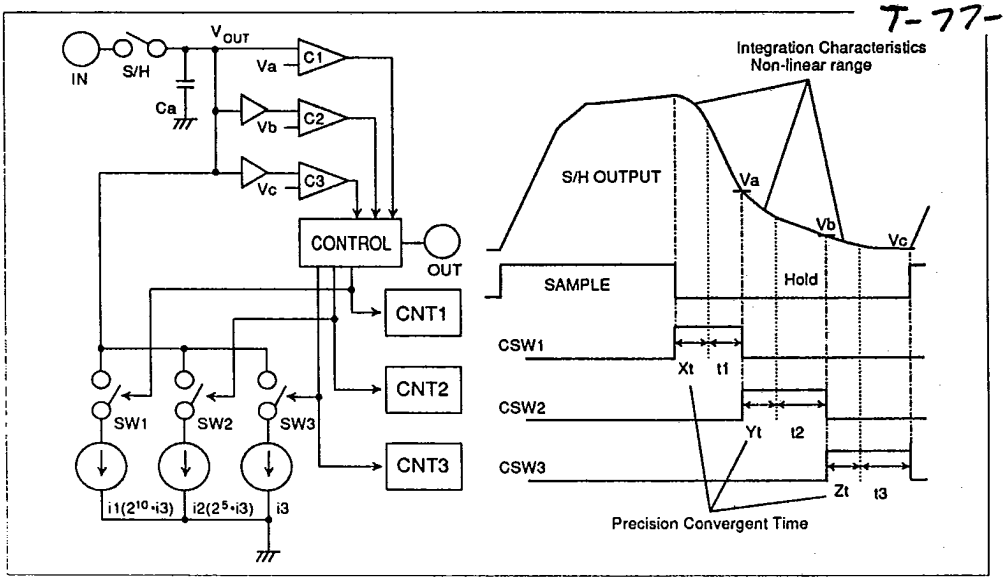


Figure 2. Principle of 3-segment Cascade Integration A/D Operation

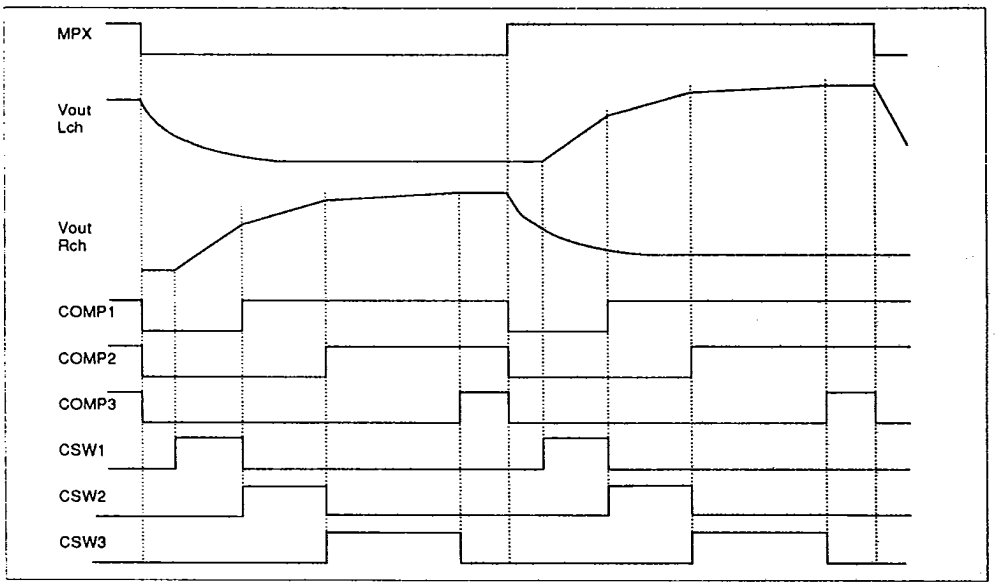


Figure 3. A/D Conversion Timing Chart

Offset Servo

When A/D converter DC offset is generated, the signal processor LSI outputs digital zero data during REC/MUTE (no signal recording), causing the offset to create a pop sound during playback. In order to cancel this offset, HD49219MP outputs duty converted PWM signals from ADSL and ADSR, in accordance with the upper three bits of both the Lch and Rch's 16-bit data. This PWM signal is integrated by an external integrator, and the resulting value is added to the buffer amp to cancel the offset.

PCM Data b15 MSB	b14	b13	Output Duty
0	1	1	0/8
0	1	0	1/8
0	0	1	2/8
0	0	0	3/8
1	1	1	5/8
1	1	0	6/8
1	0	1	7/8
1	0	0	8/8

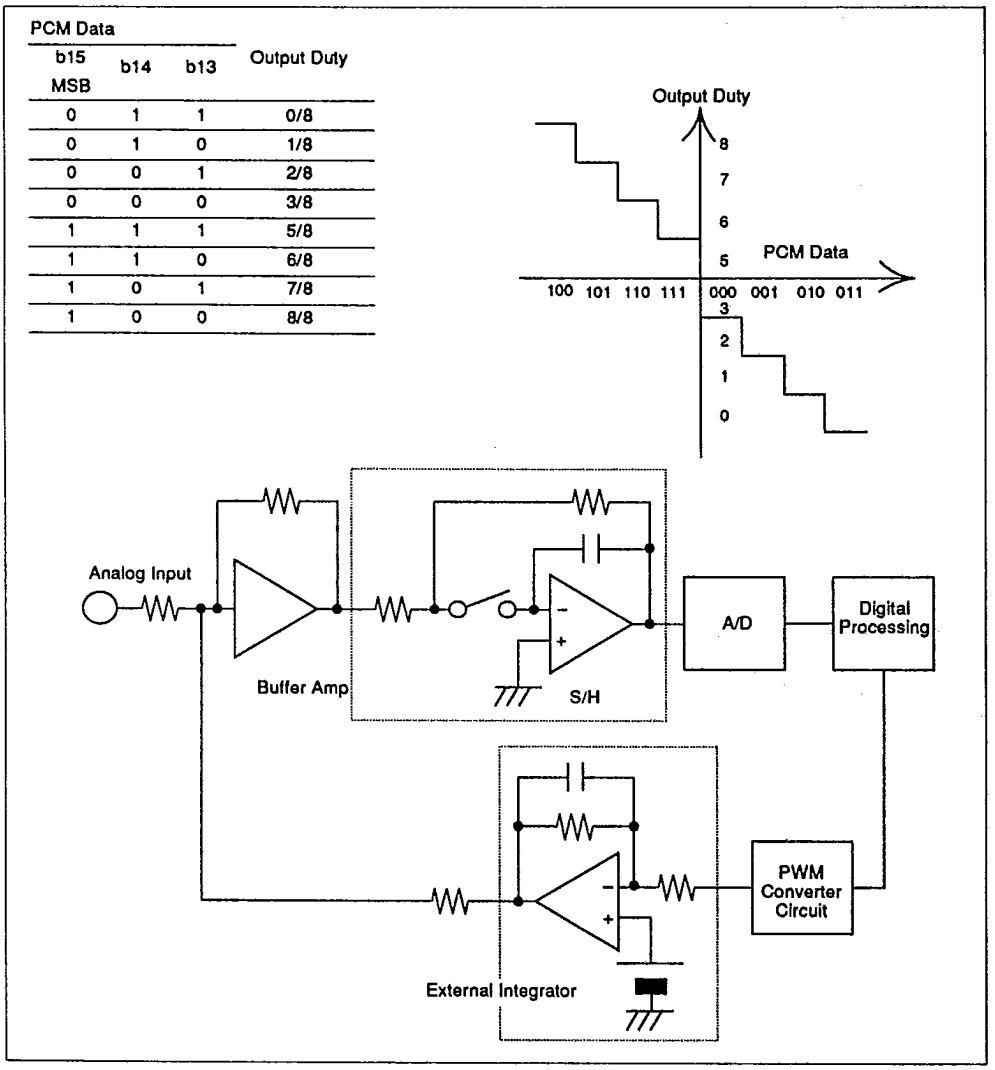


Figure 4. Offset Servo Principle

HD49219MP Operation and Application

Connect a 36.864MHz (768 × 48kHz) crystal to XCO and XCI for 48kHz and 32kHz sampling. HD49219 counts the integration period according to this clock frequency.

HD49219MP begins operation with the input of MPX, which is reoutput from S/H. Notes that when SMPX = L, the externally input MPX is output directly, but when SMPX = H, the MPX is internally synchronized before output. Also, SCK is in the idle state when SMPX = L, and in the output state when SMPX = H. The HA12131MP or HA12132MP used in the system receives the signal for A/D conversion.

The integration periods are counted by HD49219MP in accordance with the handshake interface which uses CSW1 to CSW3 and COMP1 to COPM3, and PCM data is output in the serial interface format selected by SCKX. The offset servo operates when ADS = H. The upper 3 bits of the PCM data are decoded, and PWM signals are output from ADSL and ADSR.

Mode Settings

HD49219MP operation is controlled using the mode setting pins.

1. Initialize mode switching
   MRESET is used to switch the initialize mode as shown to the right.

MRESET = 'L'	MRESET = 'H'
Reset	Normal

2. Normal/Adjust mode switching
   IHL and IHR is used to switch the Normal/Adjust mode as shown to the right.

	IHR = 'L'	IHR = 'H'
IHL = 'L'	Disable	Rch adjust mode Offset servo Duty 50%
IHL = 'H'	Lch adjust mode Offset servo Duty 50%	Normal

3. fs switching
   SF is used to switch the fs mode as shown to the right.

SF = 'L'	SF = 'H"
32kHz	48kHz

4. Serial interface mode switching
   SCKX is used to switch the serial interface mode as shown to the right. Interface formats are shown below.

SCKX = 'L'	SCKX = 'H'
CKX17 mode	CKX16 mode

• Serial interface format

There are two types of HD49219MP serial interface formats, one of which is selected by SCKX.

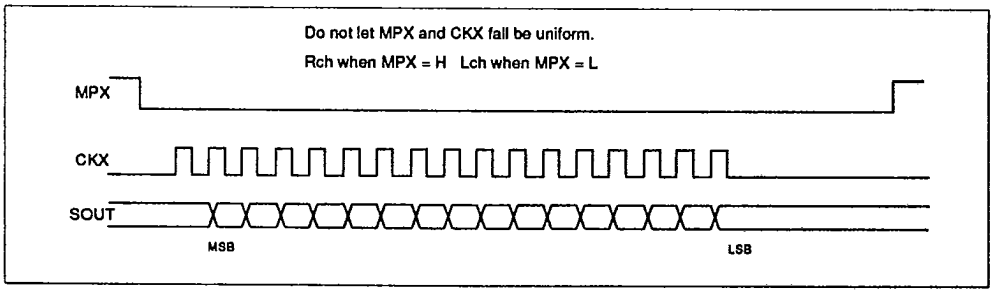


Figure 5. CKX17 Mode Timing Chart

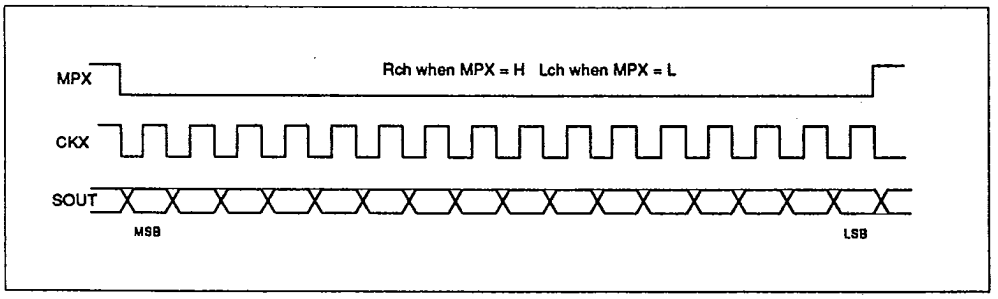


Figure 6. CKX 16 Mode Timing Chart

5. Offset servo adjustment mode switching
   ADS is used to switch the offset servo adjustment mode as shown to the right.

ADS = 'L'	ADS = 'H'
Offset servo adjustment mode (PWM Duty 50%)	Normal

6. System clock switching
   SC is used to switch the system clock as shown to the right. In the table to the right, X'tal = 36.864MHz is used.

SC = 'L'	SC = 'H'
12.288MHz	6.144MHz

7. Synchronous MPX/Asynchronous MPX switching
   SMPX is used to switch between synchronous MPX/asynchronous MPX as shown to the right. SCK is stopped when SMPX = L.

SMPX = 'L'	SMPX = 'H'
Asynchronous MPX mode (External MPX)	Synchronous MPX mode (Internal MPX)

8. Quenching mode switching
   SX is used to switch the quenching mode as shown to the right.

SX = 'L'	SX= 'H'
X'tal quench state System clock stopped ('L')	X'tal generation state System clock output

- The following shows the general methods of SMPX and SX use.

	SMPX = 'L'	SMPX = 'H'
SX ='L'	Asynchronous A/D converter, A/D not used (Advantageous at point of dissipation and noise by making SX = L)	Synchronous A/D converter, A/D not used (Advantageous at point of dissipation and noise by making SX = L)
SX = 'H'	Asynchronous A/D converter	Synchronous A/D converter (Most standard use) For example: DAT, DSP and other equipment

Adjustments

HA12131MP and HA12132MP Adjustments

The reference level of the cascade integration A/D comparator should be adjusted so that each counter reaches the full count in case that the full-scale voltage is input after elapsing a certain period of time for precision convergent (longer than non-linear area of the integration characteristics), when operating the current switch of the integration amplifier output, and after having completed the conversion within a half cycle (10.4µs when f_s = 48kHz) of the sampling frequency.

1. In order to protect against counter overflow, the input level is preset so it is 3dB to 6dB less than that of full scale voltage (4Vp-p for HA12131MP, 2.3Vp-p for HA12132MP).
2. Enlarge the integration waveform at pin 9 and pin 36 for HA12131MP/HA12132MP, and confirm the level difference with integrator output. If the waveform does not appear as shown in Figure 7, modulate VR5 and VR 6 (Figure 11) to create a level difference.
3. Monaural operation through either channel can be obtained from terminals IHL and IHR.
4. Apply a trigger pulse at CSW3, and adjust LMR and LML volume of HA12131MP or HA12132MP for a minimum pulse duration of 3.5µs (comparison level for Comparator 2).
5. Apply a trigger pulse at CSW2, and adjust LHR and LHL volume of HA12131MP or HA12132MP for a minimum pulse duration of 1.5µs (comparison level for Comparator 1).
6. Repeat Steps 3, 4, and 5 above for the other channel to adjust comparison levels.

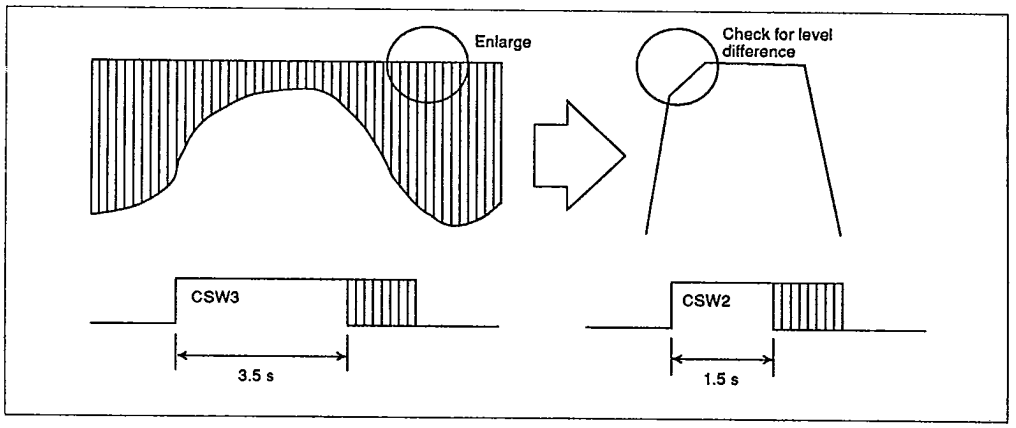


Figure 7. HA12131MP/HA12132MP Adjustment Procedure

Offset Servo Adjustment

The A/D converter DC offset can be compensated using the offset servo. First, however, the DC offset must be adjusted so that offset servo operates at output midpoint value of 0V.

1. With no input signal present, operate one channel from IHR, IHL, and output a duty 50% pulse at ADSL, ADSR.
2. Applying a trigger pulse at S/H of HD49219MP, adjust VR5 and VR6 (Figures 11 and 12) so that MSBs are approximately half 1 and half 0.

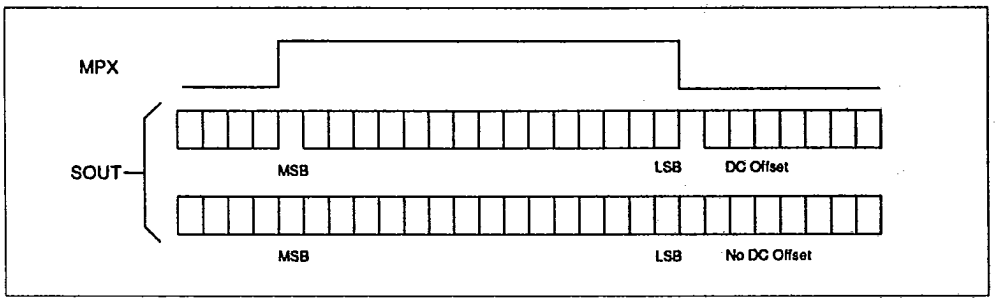
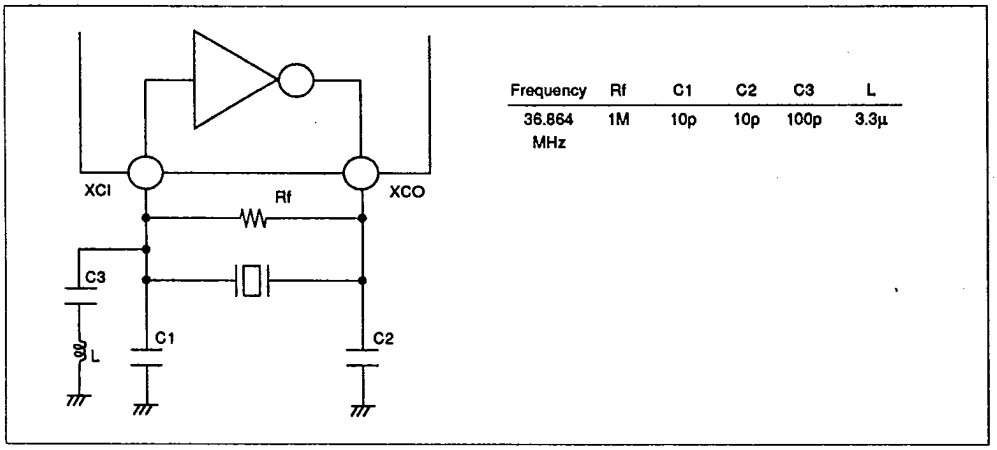


Figure 8. Offset Servo Adjustment

Recommended Components

Oscillator

The following shows a sample external connection for KINSEKI X'tal (HC-49/U).



Frequency	Rf	C1	C2	C3	L
36.864 MHz	1M	10p	10p	100p	3.3µ

Figure 9. Oscillator Circuit Sample

Filter

The following shows a sample external connection for the TOKO APQ25-099N and YC208BLRE-5290N filters.

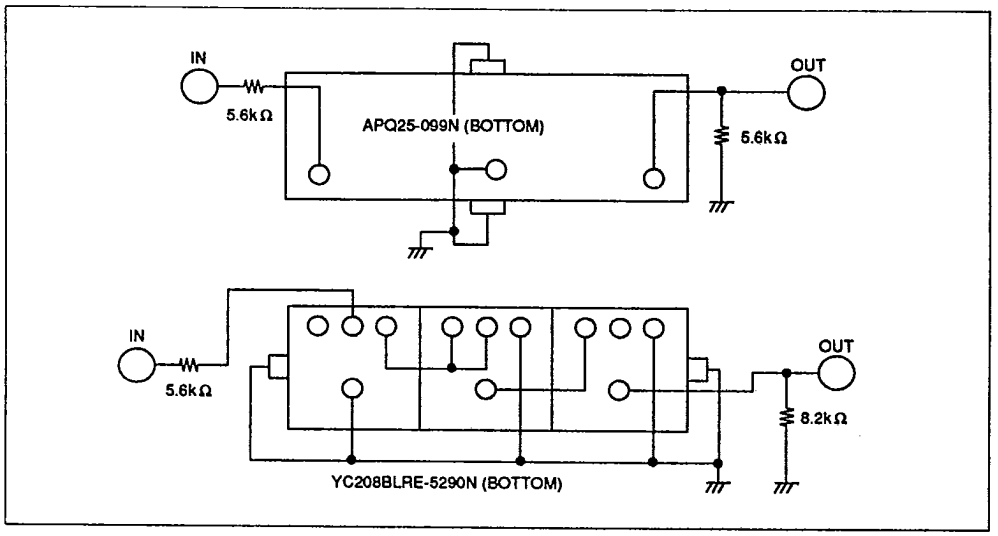


Figure 10. Filter Circuit Example

PCB Precautions

1. Position HD49219MP as close as possible to HA12131MP/HA12132MP, and keep COMP1 to COMP3, CSW1 to CSW3 wiring as short as possible.
2. GND1 and $V_{cc}2$ are susceptible to distortion and noise. When designing patterns, use bypass capacitor, keep wiring thick and short, and keep supply line impedance low.

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Terminal Voltage	V_T	−0.3 to V_{CC} +0.3 (Max 7.0)	V
Power Dissipation	P_T	400	mW
Operating Temperature	T_{opr}	−20 to +75	°C
Storage Temperature	T_{stg}	−55 to +125	°C

Electrical Characteristics (V_{CC} = 5V, Ta = 25°C)

Item		Symbol	Applicable Terminal	Min.	Typ.	Max.	Unit	Test Condition
Supply Voltage		V_{CC}	$V_{CC}1$, $V_{CC}2$	4.5	5	5.5	V	
Input Voltage	'H' level	V_{IH1}	C, CR	$0.8V_{CC}$	—	—	V	
	'L' level	V_{IL1}		—	—	$0.2V_{CC}$	V	
Input Leak Current		I_L	C	−1	—	+1	µA	$0<Vi<V_{CC}$
Input Terminal Pullup Resistance		R_{PU}	CR	10	20	40	kΩ	
Output Voltage (1)	'H' level	V_{OH1}	CO	$V_{CC}-0.5$	—	—	V	$-I_{OH}$ = 0.4mA
	'L' level	V_{OL1}		—	—	0.4	V	I_{OL} = 0.4mA
Output Voltage (2)	'H' level	V_{OH2}	HS	$V_{CC}-0.5$	—	—	V	$-I_{OH}$ = 0.4mA
	'L' level	V_{OL2}		—	—	0.4	V	I_{OL} = 0.6mA
Operating Current		I_{CC}		—	20	—	mA	

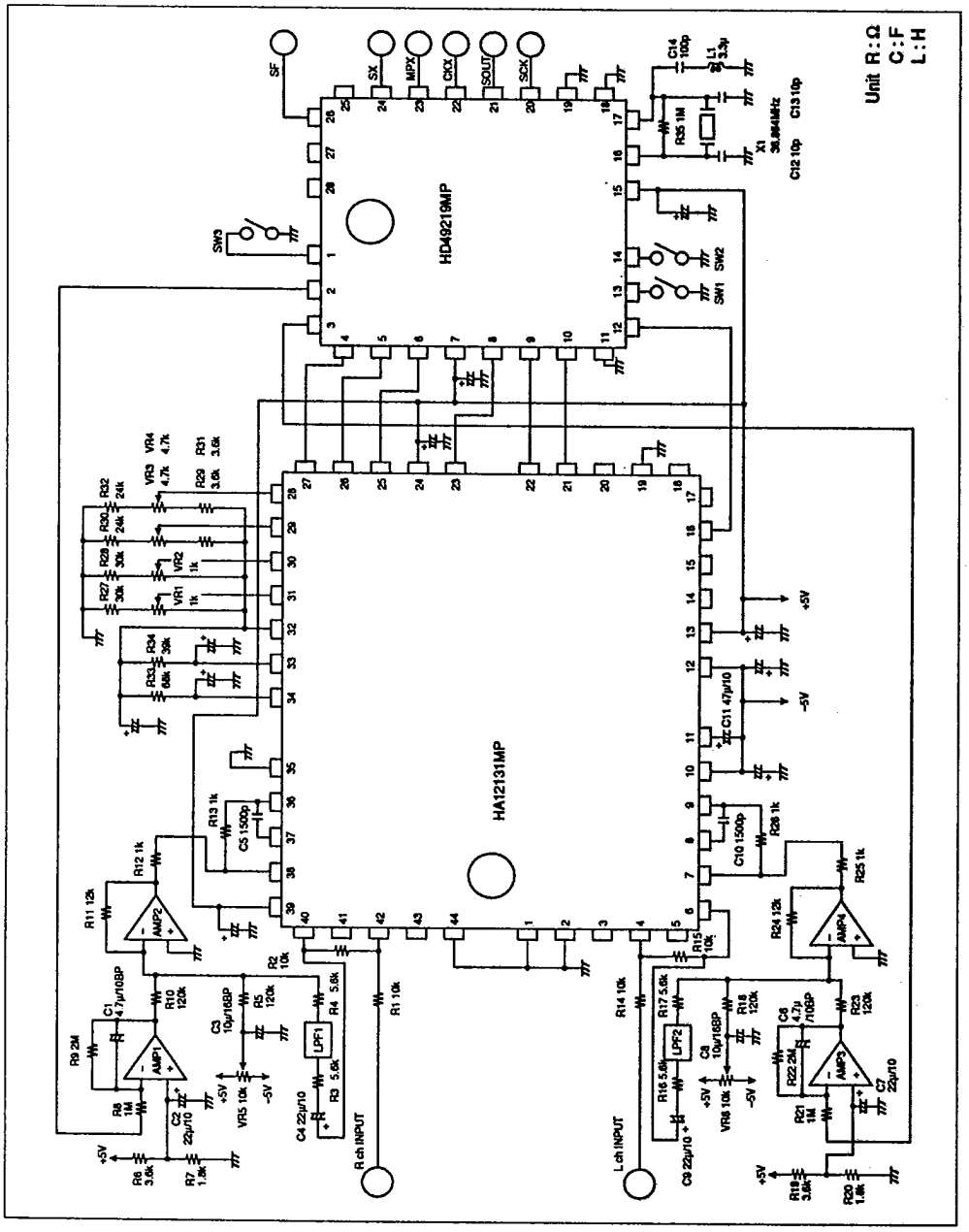


Figure 11. Normal Sampling 2ch Circuit Example