FAIRCHILD
SEMICONDUCTOR ™

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FIN7216-01
Multi-Gigabit Quad PHY

General Description

The FIN7216-01 is a quad channel 8-bit encoding/decoding serializer/deserializer integrated circuit. These transceivers are designed for flexible transfer and recovery of serialized data for use in Fibre Channel and Gigabit Ethernet and other applications that require reliable high speed data transfers. The chip operates as an interface between busses, backplanes, or other high bandwidth systems and subsystems. This IC provides full rate operation for maximum data transfer per channel of 1088Mb/s (8 bits at 136MHz) as well as half rate operation for a minimum transfer of 392Mb/s (8 bits at 49 MHz). The chip consists of a X20/X10 clock generator, four 8b/10b encoders, serializers/deserializers, clock/data recovery units, decoders, and elastic buffers. It can also be used as a quad 10-bit transceiver.

Applications

- Backplane interconnect
- Transceivers
  - Proprietary
  - Fibre Channel
  - Gigabit Ethernet
- Bus extension
- Link redundancy

Features

- Quad transceivers
- Data rates between 0.98 Gbps to 1.36 Gbps and 0.49 Gbps to 0.68 Gbps
- ANSI X3T11 Fibre Channel and IEEE 802.3z Gigabit Ethernet compliance
- Aggregate raw data rate of over 8 Gigabits per second full duplex
- PECL TX Outputs and Rx Inputs with redundancy
- 8b/10b Encode and Decode per channel
- Optional EnDec bypass for Ten Bit Interface (TBI)
- Elastic buffers for channel to channel cable deskewing and alignment
- Transmit and receive rate matching via K28.5 Symbol IDLE insertion/deletion
- Align output to local REFCLK or to recovered clock for received data
- PECL Receive Signal detect for both primary and redundant inputs
- PECL Receive Signal cable equalization
- Per channel serial Transmit to Receive loopback mode
- Per channel parallel Receive to Transmit internal loopback modes
- Baud rate clock developed from clock multiplier
- Automatic lock to reference clock
- JTAG 1149.1 compliant boundary scan for TTL I/O
- Built-In Self Test (BIST)
- 3.3V power supply, less than 2.5W
- 256 pin 27 x 27mm BGA package
- Alternate source for VSC7216-01, VSC7217
- System Level BIST from transmit to receive device
- No external capacitors required
- Optional control of BIST through JTAG Port
- Maximum user generated clock frequency is equal to 1/10 or 1/20 transmit frequency
- No heat sink required under most operating conditions

Ordering Code:

Order Number	Package Number	Package Description
FIN721601G	BGA256A	256-Ball Thermally-Enhanced Ball Grid Array (TBGA), JEDEC MO-149, 1.27mm Pitch, 27mm Square

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Logic Diagrams

Transmitters
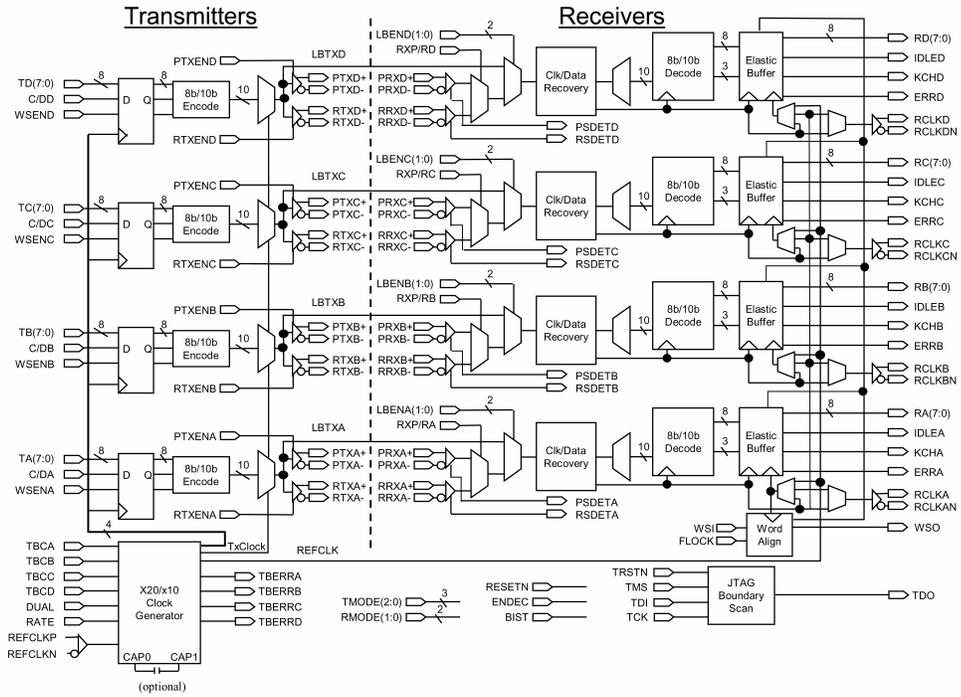
Receivers

Logic Diagrams (Continued)

Transmitter
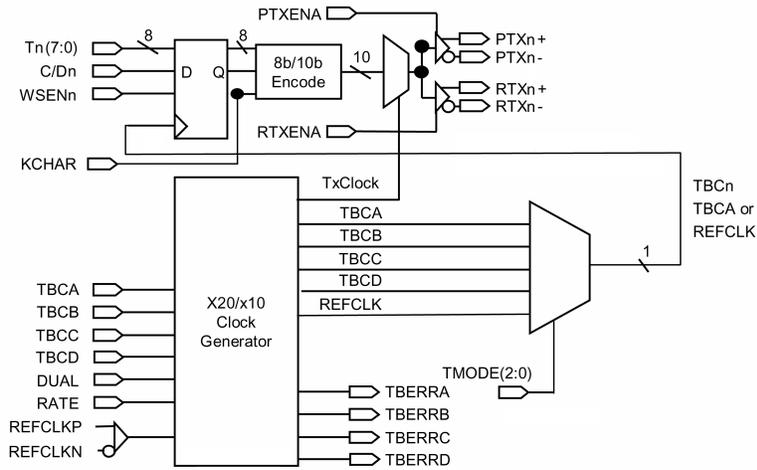
Receiver
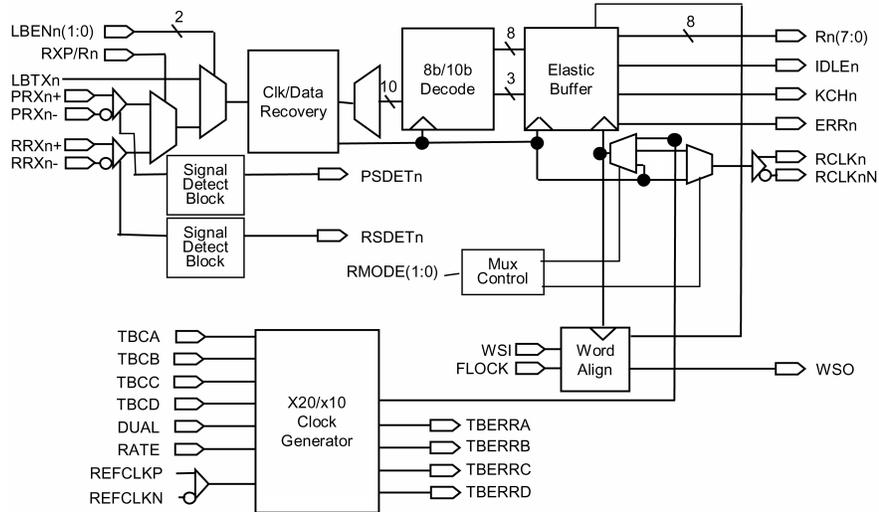
Pin Descriptions

In this document, each of the four channels are identified as channel A, B, C or D. When discussing a signal on any specific channel, the signal will have the channel letter embedded in the name, e.g., TA(7:0). When referring to the common behavior of a signal which is used on each of the four channels, a lower case "n" is used in the signal name, e.g., Tn(7:0). Differential signals (e.g., PTXA+ and PTXA-) may be referred to as a single signal, i.e. PTXA, by dropping reference to the "+" and "-". REFCLK refers either to the PECL/TTL input pair REFCLKP/REFCLKN, which can be differential PECL (using both REFCLKP and REFCLKN) or single-ended TTL (using REFCLKP and leaving REFCLKN open).

Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	PRXC+	PRXC-	RRXC+	RRXC-	TD4	C/DD	VSSD	REFCLKP	TC0	TC4	VSSD	TC7	TRSTN	TDI	TCK	RC0	RC3	RC4	VSST	ERRC
B	RRXD+	RRXD-	RXP/RC	TMODE2	TD0	TD2	TD5	WSEND	TBCC	TC3	VDDD	C/DC	TMS	VDDT	RC2	VSST	VDDT	TBERRC	VDDT	RD0
C	VDDD	RXP/RD	VSSD	VSSD	TD0	TD1	VSSD	TD6	TBCD	TC1	TC6	WSENC	VSSD	VSST	RC6	RC7	IDLEC	VSST	RSDETC	RD3
D	PRXD+	PRXD-	LBENC1	VDDD	TMODE0	TMODE1	TD3	TD7	REFCLKN	TC2	TC5	BIST	VDDD	RC1	RC5	KCHC	VDDT	PSDETC	RD1	VSST
E	RTXD+	RTXD-	LBEND1	VSSD													RCLKNC	RCLKC	VDDT	RD7
F	PTXD+	PTXD-	VDDRD	LBENC0													RD2	VSST	RD4	ERRD
G	VDDRC	VDDPD	RTXEND	LBEND0													RD5	RD6	VDDT	VSST
H	RTXC+	RTXC-	RTXENC	PTXEND													VDDT	KCHD	IDLED	TBERRD
J	PTXC+	PTXC-	VDDPC	PTXENC													PSDETD	VSST	VDDT	RSDETD
K	CAP0	VSSA	VSSD	VSSA					NOT POPULATED								RCLKD	RCLKND	TD0	VDDD
L	CAP1	VDDA	VDDD	VDDA													WSO	VDDT	VSSD	WSI
M	PTXB+	PTXB-	VDDPB	PTXENB													RSDETA	VSST	RCLKNA	RCLKA
N	RTXB+	RTXB-	RTXENB	PTXENA													IDLEA	ERRA	VDDT	VSST
P	VDDRB	VDDPA	RTXENA	LBENA0													VDDT	RA7	KCHA	PSDETA
R	PTXA+	PTXA-	VDDRA	LBENB0													RA3	VSST	RA6	TBERRA
T	RTXA+	RTXA-	LBENA1	VSSD													RCLKB	RA0	VDDT	VSST
U	PRXA+	PRXA-	LBENB1	VDDD	DUAL	RMODE0	TA2	TA6	TBCA	TB3	TB7	RESETN	VSSD	RB2	RB6	ERRB	VDDT	RSDETB	RA2	RA5
V	VDDD	RXP/RA	VSSD	VSSD	VDDD	VSSD	TA3	VDDD	TBCB	TB2	C/DB	ENDEC	RB0	VSST	RB7	KCHB	TBERRB	VSST	PSDETB	RA4
W	RRXA+	RRXA-	RXP/RB	RMODE1	TA0	TA1	TA5	VSSD	TB0	TB4	TB6	KCHAR	FLOCK	VDDT	RB3	VSST	VDDT	IDLEB	VDDT	RA1
Y	PRXB+	PRXB-	RRXB+	RRXB-	TA4	TA7	C/DA	WSENA	TB1	TB5	VDDD	WSENB	RATE	RSVD	VDDD	RB1	RB4	RB5	VSST	RCLKNB

Pin Descriptions

Pin	Name	I/O	Type	Pin Description
6Y, 8U, 7W, 5Y, 7V, 7U, 6W, 5W	TA(7: 0)	I	TTL	Transmit data for channel A, synchronous to REFCLK, TBCA
11U, 11W, 10Y, 10W, 10U, 10V, 9Y, 9W	TB(7:0)	I	TTL	Transmit data for channel B, synchronous to REFCLK, TBCB or TBCA
12A, 11C, 11D, 10A, 10B, 10D, 10C, 9A	TC(7:0)	I	TTL	Transmit data for channel C, synchronous to REFCLK, TBCC or TBCA
8D, 8C, 7B, 5A, 7D, 6B, 6C, 5B	TD(7:0)	I	TTL	Transmit data for channel D, synchronous to REFCLK, TBCD or TBCA
7Y 11V 12B 6A	C/DA C/DB C/DC C/DD	I	TTL	Control/Data for channel n. If C/Dn = LOW, Tn(7:0) is used to generate transmit data. If KCHAR = C/Dn = HIGH, special Kx.y characters are transmitted based upon the value of Tn(7:0). If KCHAR = LOW and C/Dn = HIGH, IDLE characters are transmitted. When ENDEC = LOW, this is equivalent to data bit Tn8.
8Y 12Y 12C 8B	WSENA WSENB WSENC WSEND	I	TTL	Word Sync ENable for channel n. Asserted HIGH for one cycle to initiate transmission of the Word Sync Sequence as defined in Figure 5 and related text. When ENDEC = LOW, this is equivalent to data bit Tn9.
9U 9V 9B 9C	TBCA TBCB TBCC TBCD	I	TTL	Transmit Byte Clock for channel n. Optional input data timing reference for Tn(7:0), WSENn and C/Dn.
12W	KCHAR	I	TTL	Special Kx.y CHARacter enable. When C/Dn is HIGH, KCHAR controls transmit data. When LOW, IDLEs are sent. When HIGH, Kx.y special characters are sent as encoded on Tn(7:0). This is intended to be a static input and cannot be changed on a cycle-by-cycle basis. When ENDEC = LOW, this is equivalent KCHAR = ENCDET signal. (See "Decoder Bypass Mode")
5D 6D 4B	TMODE0 TMODE1 TMODE2	I	TTL	Transmit input data timing MODE. Determines the timing reference for Tn(7:0), WSENn and C/Dn on all channels as defined in Table 3.
20R 17V 18B 20H	TBERRA TBERRB TBERRC TBERRD	O	TTL	Transmit Buffer ERRor for channel n. When HIGH indicates that the elastic limit of the transmit input skew buffer was exceeded, output timing is same as Rn(7:0). A LOW indicates correct reception of the 256-byte incrementing pattern in BIST mode.
1R, 2R 1M, 2M 1J, 2J 1F, 2F	PTXA +/- PTXB +/- PTXC +/- PTXD +/-	O	PECL	Primary differential serial TX outputs for channel n. These pins output serialized transmit data when PTXENn is HIGH. AC-coupling is recommended
1T, 2T 1N, 2N 1H, 2H 1E, 2E	RTXA +/- RTXB +/- RTXC +/- RTXD +/-	O	PECL	Redundant differential serial TX outputs for channel n. These pins output serialized transmit data when RTXENn is HIGH. AC-coupling is recommended.
4N 4M 4J 4H	PTXENA PTXENB PTXENC PTXEND	I	TTL	Primary TX output ENable for channel n. When HIGH PTXn+/- is active; when LOW, PTXn+/- is powered down and the outputs are un-driven.
3P 3N 3H 3G	RTXENA RTXENB RTXENC RTXEND	I	TTL	Redundant TX output ENable for channel n. When HIGH, RTXn+/- is active; when LOW, RTXn+/- is powered down and the outputs are un-driven.
18P, 19R, 20U, 20V, 17R, 19U, 20W, 18T	RA(7:0)	O	TTL	Receive data for channel A. Synchronous to RCLKA/RCLKNA or REFCLK as selected by RMODE(1:0).
15V, 15U, 18Y, 17Y, 15W, 14U 16Y, 13V	RB(7:0)	O	TTL	Receive data for channel B. Synchronous to RCLKB/RCLKNB, RCLKA/RCLKNA or REFCLK as selected by RMODE(1:0).

Pin Descriptions (continued)

Pin	Name	I/O	Type	Pin Description
16C, 15C, 15D, 18A, 17A, 15B 14D, 16A	RC(7:0)	O	TTL	Receive data for channel C. Synchronous to RCLKC/RCLKNC, RCLKA/ RCLKNA or REFCLK as selected by RMODE(1:0).
20E, 18G, 17G, 19F, 20C, 17F, 19D, 20B	RD(7:0)	O	TTL	Receive data for channel D. Synchronous to RCLKD/RCLKND, RCLKA/ RCLKNA or REFCLK as selected by RMODE(1:0).
17N 18W 17C 19H	IDLEA IDLEB IDLEC IDLED	O	TTL	IDLE detect for channel n. When HIGH, an IDLE character has been detected by the decoder and is on Rn(7:0). When ENDEC = LOW, this is equivalent to COMDETn (See "Decoder Bypass Mode")
19P 16V 16D 18H	KCHA KCHB KCHC KCHD	O	TTL	Kx.y CHaracter detect for channel n. When HIGH, a special Kx.y character has been detected by the decoder and is on Rn(7:0). When ENDEC = LOW, this is equivalent to data bit Rn8.
18N 16U 20A 20F	ERRA ERRB ERRC ERRD	O	TTL	ERRor detect for channel n. When HIGH, an invalid 10-bit character or dis-parity error has been detected and the data on Rn(7:0) is invalid. When ENDEC = LOW, this is equivalent to data bit Rn9.
20M 19M 17T 20Y 18E 17E 17K 18K	RCLKA RCLKNA RCLKB RCLKNB RCLKC RCLKNC RCLKD RCLKND	O	TTL	Recovered CLocK outputs for channel n. These outputs are driven from either the channel A or channel n recovered clock, at 1/10 or 1/20 the baud rate, as selected by RMODE(1:0) and DUAL. When unused, RCLKn is LOW and RCLKNn is HIGH.
6U 4W	RMODE0 RMODE1	I	TTL	Receive output data timing MODE. Determines the timing reference for all receive channels' Rn(7:0), IDLEn, KCHn and ERRn output data. Also for the PSDETn, RSDETn and TBERRn outputs, as defined in Table 7.
1U, 2U 1Y, 2Y 1A, 2A 1D, 2D	PRXA+/- PRXB+/- PRXC+/- PRXD+/-	I	PECL	Primary differential serial RX inputs for channel n. These pins receive the serialized input data when LBENn(1) is LOW and RXP/Rn is HIGH; other-wise they are unused. They are internally biased at V_{DD} /2 through a 3.2K resistor to the bias voltage. AC-coupling is recommended.
1W, 2W 3Y, 4Y 3A, 4A 1B, 2B	RRXA+/- RRXB+/- RRXC+/- RRXD+/-	I	PECL	Redundant differential serial RX inputs for channel n. These pins receive the serialized input data when LBENn(1) is LOW and RXP/Rn is LOW; oth-erwise they are unused. They are internally biased at V_{DD} /2 through a 3.2k resistor to the bias voltage. AC-coupling is recommended.
4P 3T 4R 3U 4F 3D 4G 3E	LBENA0 LBENA1 LBENB0 LBENB1 LBENC0 LBENC1 LBEND0 LBEND1	I	TTL	Loop Back ENable for channel n. These inputs control the channel serial or parallel loopback configuration as described in Table 9.
2V 3W 3B 2C	RXP/RA RXP/RB RXP/RC RXP/RD	I	TTL	RX input Primary/Redundant serial input select for channel n. When LBENn(1) is LOW, this input selects PRXn+/- as the RX serial input source when HIGH and RRXn+/- as the serial input source when LOW.
20P 19V 18D 17J	PSDETA PSDETB PSDETC PSDETD	O	TTL	Primary analog Signal DETect, channel n. This output goes HIGH when a signal is detected on PRXn and LOW when no signal is detected. Output timing is the same as Rn(7:0)
17M 18U 19C 20J	RSDETA RSDETB RSDETC RSDETD	O	TTL	Redundant analog Signal DETect, channel n. This output goes HIGH when a signal is detected on RRXn and LOW when no signal is detected. Output timing is the same as Rn(7:0)

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Pin Descriptions (continued)

Pin	Name	I/O	Type	Pin Description
8A 9D	REFCLKP REFCLKN	I	PECL	REFCLK differential Positive and Negative PECL or single-ended TTL inputs. This rising edge of this clock latches transmit data and control into the input register depending on the transmit interface input timing mode (See Table 3). It also provides the reference clock, at 1/10th or 1/20th of the baud rate to the PLL as selected by DUAL. If TTL, connect to REFCLKP but leave REFCLKN open. If PECL, connect both REFCLKP and REF-CLKN.
1K 1L	CAP0 CAP1		Analog	Loop Filter CAPacitor for clock generation PLL. Nominally 0.1µF, amplitude is less than 3V. See the Clock Synthesizer section for more details.
5U	DUAL	I	TTL	DUAL clock Mode. When LOW, REFCLK and RCLKn/RCLKNn are 1/10th the baud rate. When HIGH, they are 1/20th the baud rate
13W	FLOCK	I	TTL	Frequency LOCKed mode. When HIGH indicates that each transmit channel's REFCLK is frequency-locked to the receive channel's word clock. Controls rate matching (IDLE delete/duplicate) logic along with the WSI input as per Table 8.
12D	BIST	I	TTL	Built-In Self Test mode. When HIGH, all transmit channels continuously send a 256 byte incrementing data pattern, and all receive channels signal correct reception of the test pattern with a LOW on the TBERRn outputs.
12V	ENDEC	I	TTL	ENcoder/DECoder enable. When HIGH the FIN7216-01 is configured for 8-bit operation, internal 8b/10b encoding is enabled. When LOW a 10-bit interface is used, internal 8b/10b encoding is bypassed.
12U	RESETN	I	TTL	RESETN input. When asserted LOW, the transmitter input skew buffers and receiver elastic buffers are re centered, all flip-flops cleared, and all synchronized state machines enter LOSS_OF_SYNC state. This pin does not reset the internal PLL's.
20L	WSI	I	TTL	Word Sync Input. Used to control channel alignment and IDLE character insertion/deletion as defined in Table 7.
17L	WSO	O	TTL	Word Sync Output. Used to set initial channel word alignment, and to maintain alignment by controlling IDLE character insertion/deletion.
15A	TCK	I	TTL	JTAG Test Access Port test clock input
13B	TMS	I	TTL	JTAG Test Access Port test mode select input
14A	TDI	I	TTL	JTAG Test Access Port test data input
19K	TDO	O	TTL	JTAG Test Access Port test data output
13A	TRSTN	I	TTL	JTAG Test Access Port test logic reset input
14Y	RSVD	I	N/A	Reserved Inputs for future use. Set HIGH for compatibility reasons.
13Y	RATE	I	TTL	RATE Mode. When HIGH, FIN7216-01 runs at full data rate (default mode). When asserted LOW, half-speed data rate is selected.
2L, 4L	VDDA		VDD	Analog power supply to PLL.
2K, 4K	VSSA		GND	Analog ground to PLL.
11B, 11Y, 13D, 15Y, 1C, 1V, 20K, 3L, 4D, 4U, 5C, 5V, 8V	VDDD		VDD	Digital power supply.
11A, 13C, 13U, 19L, 3C, 3K, 3V, 4C, 4E, 4T, 4V, 6V, 7A, 7C, 8W	VSSD		GND	Digital ground.
14B, 14W, 17B, 17D, 17H, 17P, 17U, 17W, 18L, 19B, 19E, 19G, 19J, 19N, 19T, 19W	VDDT		VDD	TTL output power supply.
14C, 14V, 16B, 16W, 18C, 18F, 18J, 18M, 18R, 18V, 19A, 19Y, 20D, 20G, 20N, 20T	VSST		GND	TTL output ground.

Pin Descriptions (continued)

Pin	Name	I/O	Type	Pin Description
2P	VDDPA		VDD	PECL Output power supply for PTXA.
3R	VDDRA			PECL Output power supply for RTXA.
3M	VDDPB			PECL Output power supply for PTXB.
1P	VDDRB			PECL Output power supply for RTXB.
3J	VDDPC			PECL Output power supply for PTXC.
1G	VDDRC			PECL Output power supply for RTXC.
2G	VDDPD			PECL Output power supply for PTXD.
3F	VDDRD			PECL Output power supply for RTXD.
				If use of an output is not necessary, leave the power supply pin open.

Clock Synthesizer

The clock synthesizer multiplies the reference frequency of REFCLK by 10 if the DUAL input is LOW, or by 20 if the DUAL input is HIGH. The capacitor connected between CAP0 and CAP1 is optional to damp the common-mode noise- especially from the power supply to the Clock Multiplier circuit. A 0.1uF or greater differential capacitor should again be connected between CAP0 and CAP1. These capacitors should be isolated from noisy signals and are shown in Figure 1.

Differential LVPECL or TTL signals can be connected to REFCLK. When using TTL, connect the input to REFCLKP and leave REFCLKN open. For LVPECL inputs, both REFCLKP and REFCLKN are connected. DC biasing is set internally to VDD/2 on both REFCLKP and REFCLKN.
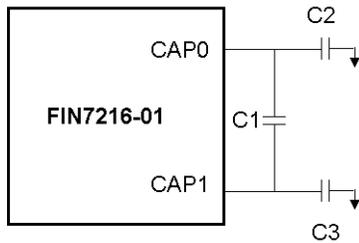
Figure 1a
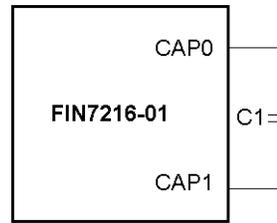
Figure 1b

FIGURE 1. Loop Filter Capacitors (Optional Circuits)

As shown in Table 1, the RATE pin sets the clock generator mode to full or half speed. A HIGH on the RATE pin puts the chip in full-speed mode, while a LOW sets the chip to half-speed. The serial link speed is determined by the REFCLK frequency and clock multiplication factor.

TABLE 1. Using the RATE input to Achieve Half-Speed Operation for 500 Mb/s and 1 Gb/s (Note 1)

RATE Pin	DUAL Pin	Clock Multiplication Factor	Serial Link Speed	Parallel Data Rate	REFCLK Frequency
0	0	x10	500 Mb/s	50 Mb/s	50 MHz
0	1	x20	500 Mb/s	50 Mb/s	25 MHz
1	0	x10	1 Gb/s	100 Mb/s	100 MHz
1	1	x20	1 Gb/s	100 Mb/s	50 MHz

Note 1: Refer to Table 17 for frequency ranges of operation.

Transmitter Functional Description

Transmitter Data Bus

The inputs to each of the four transmit channels include an 8-bit data character, Tn(7:0), and the two control pins, C/Dn and WSENn. The C/Dn input controls the transmission of either a normal data character or a special "K-character". WSENn, when held high for one cycle, starts the transmis-sion of a 16-symbol "Word Sync Sequence" used to align the receive channels. The clocking of these data and con-trol inputs is controlled by REFCLK or the rising edge of TBCn. If TBCn is used, each channel can be clocked by either its own TBCn input or TBCA. TMODE(2:0) deter-mines the transmit input timing mode. See Table 3.

TABLE 2. Using the RATE and DUAL Inputs to Achieve the Serial Link Speed Operation

TMODE	Rate	Parallel Data Rate	Dual	Clock Division Factor	REFCLK Frequency	TBCn Clock Frequency	Serial Link Speed
000	0	49 - 68 MHz	1	/ 2	24.5 - 34 MHz		490 - 680 Mbp/s
000	0	49 - 68 MHz	0	/ 1	49 - 68 MHz		490 - 680 Mbp/s
000	1	98 - 136 MHz	1	/ 2	49 - 68 MHz		0.98 - 1.36 Gbp/s
000	1	98 - 136 MHz	0	/ 1	98 - 136 MHz		0.98 - 1.36 Gbp/s
10X	0	49 - 68 MHz	1	/ 2	24.5 - 34 MHz	49 - 68 MHz	490 - 680 Mbp/s
10X	0	49 - 68 MHz	0	/ 1	49 - 68 MHz	49 - 68 MHz	490 - 680 Mbp/s
10X	1	98 - 136 MHz	1	/ 2	49 - 68 MHz	98 - 136 MHz	0.98 - 1.36 Gbp/s
10X	1	98 - 136 MHz	0	/ 1	98 - 136 MHz	98 - 136 MHz	0.98 - 1.36 Gbp/s
11X	0	49 - 68 MHz	1	/ 2	24.5 - 34 MHz	24.5 - 34 MHz	490 - 680 Mbp/s
11X	0	49 - 68 MHz	0	/ 1	49 - 68 MHz	24.5 - 34 MHz	490 - 680 Mbp/s
11X	1	98 - 136 MHz	1	/ 2	49 - 68 MHz	49 - 68 MHz	0.98 - 1.36 Gbp/s
11X	1	98 - 136 MHz	0	/ 1	98 - 136 MHz	49 - 68 MHz	0.98 - 1.36 Gbp/s

TABLE 3. Transmit Interface Input Timing Mode

TMODE(2:0)	Input Timing Reference
000	REFCLK Rising Edge
001 010 011	Reserved
100	TBCA Rising Edge
101	TBCn Rising Edge
110	TBCA Data Eye
111	TBCn Data Eye

If clocking with TBCn, these inputs must be frequency-locked to REFCLK. Phase-locking is not required, since phase drift between TBCn and REFCLK is re-centered by a small skew buffer. The RESETN input, when asserted LOW re-centers the buffers, causing the total phase drift to be limited to ±180° (one half of one byte time). The channel error output, TBERRn, when HIGH indicates that the TBCn to REFCLK ±180° phase drift limit has exceeded the elastic limit of the skew buffer. This means that a channel data byte has been dropped or duplicated. Referencing the input timing to REFCLK eliminates the occurrence of these errors. The TBERRn output timing is the same as the receiver outputs, Rn(7:0). The various output timing refer-ences are controlled by the state of RMODE(1:0). See Table 7.

Figure 2 through Figure 4 show the possible relationships between data and control inputs and the selected input tim-ing source. Figure 2 shows how REFCLK is used as an input timing reference. Figure 3 and Figure 4 show how TBCn is used as an input timing reference.

Note that the REFCLK and TBCn inputs are used internally by a PLL to generate the appropriate edges to clock the input data. The rising edges of REFCLK or TBCn provide the reference edge for the phase detection logic. An inter-nal clock is generated at 1/10th or 1/20th of the baud rate of the selected timing reference depending on the state of DUAL. When DUAL is HIGH and REFCLK is the reference timing, the internal active edges are coincident or halfway between the REFCLK rising edges.

Transmitter Functional Description (Continued)
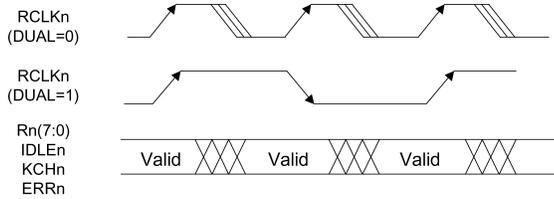
FIGURE 2. Transmit Timing, TMODE(2:0) = 000
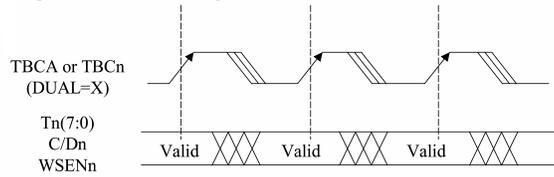
FIGURE 3. Transmit Timing, TMODE(2:0) = 10X
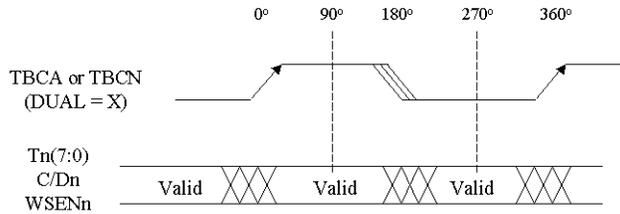
FIGURE 4. Transmit Timing, TMODE(2.0) = 11X

8b/10b Encoder

The FIN7216-01 has an 8b/10b encoder on each channel. These encoders translate the Tn(7:0) 8 bit data into a 10 bit symbol. C/Dn and KCHAR control the transmission of a special Kx.y character. See Table 4. KCHAR is intended to be a static input and is not changed cycle-by-cycle like the other transmitter inputs (Tn(7:0), C/Dn, WSENn). When C/Dn and WSENn are LOW, encoded data is transmitted. If C/Dn is HIGH and KCHAR is LOW, a K28.5 IDLE Character (K28.5 = '0011111010' or '1100000101' depending on current running disparity) is transmitted, regardless of the Tn(7:0) value. If both C/Dn and KCHAR are HIGH, the

Tn(7:0) data pattern determines which Kx.y character is transmitted. See Table 5. All other patterns cause an undefined character to be transmitted. Note, K28.5+ and K28.5- will force current running disparity to be internally set to negative or positive, respectively.

Also, a K28.5+ character is a 10b encoding of the K28.5 character chosen from the 8b/10b encoding table column when the current running disparity is positive (i.e. K28.5 = 110000 0101). Similarly, a K28.5-character is chosen when the current running disparity is negative. (K28.5 = 001111 1010)

TABLE 4. Transmit Data Controls

WSENn	C/Dn	KCHAR	Raw 8-Bit Data	Encoded 10-Bit Output
0	0	X	Dx.y	Encoded Dx.y
0	1	0	X	IDLE Character (K28.5)
0	1	1	See Table 5	Special Kx.y Character
1	X	X	X	16-Character Word Sync Sequence

Transmitter Functional Description (Continued)

TABLE 5. Special Characters (Selected when C/Dn and KCHAR are HIGH)

Code	Tn(7:0)	Comment	Code	Tn(7:0)	Comment
K28.0	000 11100	User Defined	K28.5-	101 01101	User Defined
K28.1	001 11100	User Defined	K28.6	110 11100	User Defined
K28.2	010 11100	User Defined	K28.7	111 11100	Test Only
K28.3	011 11100	User Defined	K23.7	111 10111	User Defined
K28.4	100 11100	User Defined	K27.7	111 11011	User Defined
K28.5	101 11100	IDLE	K29.7	111 11101	User Defined
K28.5+	101 01100	User Defined	K30.7	111 11110	User Defined

Encoder Bypass Mode

When ENDEC is HIGH, the 8b/10b encoding is enabled. However, when ENDEC is LOW, the 8b/10b encoding is bypassed and the FIN7216-01 acts as a 10 bit serial transmitter. Tn0 is transmitted first with C/Dn becoming Tn8, and WSENn becoming Tn9. In this mode, the KCHAR input becomes ENCDET. When ENCDET is HIGH, comma detection and re-synchronization is enabled on all four receivers. Refer to the Decoder Bypass Mode section for a description of this mode of operation in the receiver. When ENDEC is LOW, the transmitter latency is reduced by 10 bit times. This mode is commonly referred to as the Ten Bit Interface (TBI) used in serializers/deserializers for Fibre Channel and Gigabit Ethernet applications.

Word Sync Generation

The FIN7216-01 provides for the generation of channel or word alignment, also known as word sync. If a 4-byte word is input on the four transmit channels for serialization, then the four receive output streams are aligned or synchronized so that the same 4-byte data will be transferred to the receive parallel outputs on the same clock. During the Word Sync Sequence, a unique synchronization point in the serial data stream is used to align the receive channels. This pattern is a sequence of 16 consecutive K28.5 IDLE characters with disparity reversals on the second and fourth characters ("I+ I+ I- I- I+ I- I+ I- I+ I- I+ I- I+ I-" or "I- I- I+ I+ I- I+ I- I+ I- I+ I- I+"). Which sequence is sent is determined by the current running disparity of the transmitter during the serialization of the first IDLE character.

In order to initiate the transmission of the Word Sync Sequence, WSENn on each channel must be asserted HIGH for one character time on the same clock. See Figure 5. During this time, when WSENn is HIGH, the Tn(7:0) and C/Dn inputs are ignored. Additionally, during the next 15 character times, WSENn, Tn(7:0), and C/Dn are ignored. In Figure 5, the Word Sync Sequence is initiated in cycle W1 and transmitted through cycle W16. Normal data transmission (or the transmission of another Word Sync Sequence) resumes in cycle D3. This figure is illustrated assuming that input timing is referenced to REFCLK (e.g., TMODE(2:0) = 000) with the DUAL input LOW. As long as WSENn remains asserted, another Word Sync Sequence will be generated.
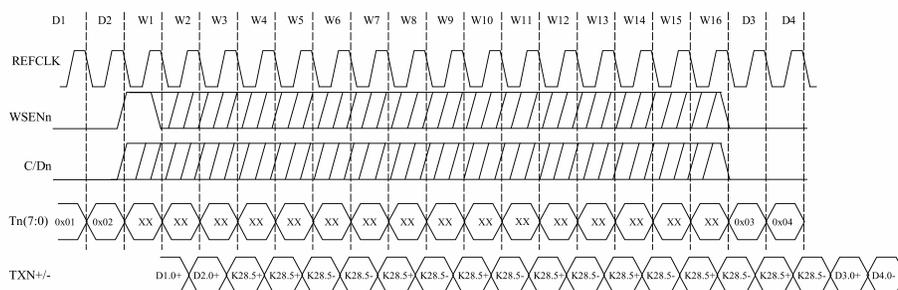
FIGURE 5. Word Sync Sequence Generation

Serializer

Internal to the chip, the 10-bit parallel output of the encoder (or encoder input register if ENDEC is LOW) is fed into a multiplexer that serializes the transmit data using the PLL generated transmit clock. The Least Significant Bit (LSB) is first to transmit. Each transmit channel has both primary (PTXn) and redundant (RTXn) output ports. These are generated from differential PECL output buffers running at either 10 or 20 times the REFCLK rate. These outputs are controlled separately by a primary enable, PTXENn and a redundant enable RTXENn. When either is HIGH, the associated outputs are enabled. When the transmitter outputs are disabled, the associated output buffers are powered down and consume no power. External resistors are not required on the PECL outputs.

Receiver Functional Description

Serial Data Source

Each of the four receive channels on the FIN7216-01 have primary and redundant input ports associated with corresponding serialized transmit outputs. Denoted PRXn and RRXn, these are the inputs to a differential input buffer. Either the PRXn or RRXn serial inputs are selected as the data source by the control pin, RXP/Rn. If RXP/Rn is HIGH, PRXn is the data source. However, when the control input LBENn(1:0) = 10, the transmitter loopback data becomes the source and RXP/Rn is ignored. See Table 6.

TABLE 6. Serial Data Source Selection

LBENn(1:0)	RXP/Rn	Serial Data Source
not equal to 1 0	0	RRXn
not equal to 1 0	1	PRXn
equal to 1 0	X	LBTXn Loopback from Transmitters

Signal Detection

On each receive channel input buffer, there are an analog primary and redundant signal detect output, PSDETn and RSDETn, respectively. These outputs can be used as a diagnostics tool for both the selected and non-selected input. PSDETn or RSDETn goes HIGH when a signal is sensed on receiver differential input pins. The output is asserted low when no signal is sensed. It is recommended a varying bit pattern be applied to the receiver input when using this function. The signal detect circuitry behaves like a re-triggerable one-shot that is triggered by signal transitions, and whose time-out interval ranges from 40 to 80 bit times. The transition density is not checked to make sure that it corresponds to a valid Fibre Channel and Ethernet data stream. The output timing of PSDETn and RSDETn is identical to the low-speed receiver outputs, Rn(7:0), and is controlled by the value of RMODE(1:0). See Table 7.

Receiver Equalization

It is not uncommon for the data to the receiver inputs PRXn/RRXn, to contain a substantial amount of Inter Symbol Interference (ISI) or deterministic jitter. This interference can cause the receiver to introduce errors when recovering data. In order to compensate for the cause of error, an equalizer has been added to each receiver input buffer. The equalizer is designed to boost the high frequency edge response in order to reduce the effects of ISI typically found in copper cables or backplane traces caused by the attenuation of the high frequency content of the signal due to the skin effect.

Clock and Data Recovery

Each receiver channel contain an independent Clock Recovery Unit (CDR). The CDR provides a clean recovered clock by automatically locking onto the selected serial input data, extracting the high-speed clock, and re-timing the data. If the data is not present, the CDR will lock to REFCLK. The recovered clock, RCLKn and RCLKNn, will equal the transmit clock without duty cycle distortion.

The CDR performs bit synchronization during sampling of the incoming serial data. If the CDR is not locked onto the serial data, the decoder output data is invalid, and one or more 8b/10b decoding or disparity errors are generated. If the serial data link is disturbed or broken, the CDR requires a specified amount of time to reacquire and lock onto the data. See AC timing Characteristics for "Data Acquisition Lock Time" (Table 16).

Deserializer and Character Alignment

The re-timed serial data from each of the CDR's is fed into the deserializer and converted into a 10 bit character. The receiver recognizes the character boundary in the data pattern by detecting a special comma character ('0011111xxx' or '1100000xxx' depending on the current running disparity). It is important to note that this pattern is found in three special Fibre characters, K28.1, K28.5 and K28.7, however, K28.5 is chosen as the unique IDLE character. Only K28.1 and K28.5 should be used in normal operation. The K28.7 character should be used for only test and characterization.

Character alignment occurs when the deserializer synchronizes the 10-bit character boundary to a "comma" pattern in the incoming serial data stream. If the receiver identifies a "comma" pattern in the incoming data stream which is misaligned to the current character boundary the receiver will re-synchronize the recovered data in order to align the data to the new "comma" pattern. Re-synchronization ensures that the "comma" character is output on the internal 10-bit bus so that bits 0 through 9 equal '0011111xxx' or '1100000xxx'. If the "comma" pattern is aligned with the current character boundary, re-synchronization will not change the current alignment. Re-synchronization is always enabled and cannot be turned off when ENDEC is HIGH. After character re-synchronization the FIN7216-01 ensures that within a link, the 8-bit data sent to the transmitting FIN7216-01 will be recovered by the receiving FIN7216-01 in the same bit locations as the transmitter (i.e., Tn(7:0) = Rn(7:0)). When ENDEC is LOW, "comma" detection and alignment are enabled only if KCHAR is HIGH.

10b/8b Decoder

The 10b/8b decoder converts the 10 bit character data from the deserializer into an 8b data byte and three status bits. An Out-of Band Error is generated on the receiver status bus if the 10 bit character does not represent a valid value. Additionally, a Disparity Error is generated if the current running disparity of the pattern does not match the expected disparity value. The decoder detects the reception of a K-character and recognizes the unique K28.5 IDLE from the other K values. The status information is used in conjunction with the loss of synchronization State Machine status and FIFO error information to provide prioritized receiver output status information. See Table 9.

Elastic Buffer and Channel De-skewing

The elastic buffer on each receive channel acts as an interface between the recovered clock domain and the output clock domain for the decoded data and status information. The decoded data and status information is written into the buffers by the recovered clock, and is read during the selected output clock. This provides for the transfer of decoded data from the timing control of the channel's recovered clock to the timing control of the output clock. The elastic buffers also facilitate channel alignment and rate matching by the insertion/deletion of K28.5 IDLE characters if the channel's recovered clock and output clock are not frequency locked.

When initializing the chip or the link, the elastic buffers are re-centered under three conditions. When RESETN goes LOW, the entire chip is initialized and the read/write point-

Receiver Functional Description (Continued)

ers are re-centered in each elastic buffer. Additionally, the elastic buffer is re-centered when a comma character changes the receive character's boundary. Lastly, the buffer is re-centered whenever the synchronization point in the Word Sync Sequence is received (see section on Word Alignment). Note that re-centering can result in the loss or duplication of decoded character data and status information.

The user should cause a Word Sync sequence to re-center all elastic buffers in the event of the change in transmit timing (e.g. phase shifts in TBCn) or phase/alignment shifts in the receiver. This prevents data corruption that could be caused by the shifts.

The receiver output recovered data pins is output on pins Rn(7:0). The status pins are IDLEn, KCHn and ERRn. The receive outputs are timed to either REFCLK, Channel As recovered clock (RCLKA/RCLKNA), or to its own recovered clock (RCLKn/RCLKNn) as selected by RMODE (1:0). See Table 7. Similarly, the transmitter skew buffer error outputs TBERRn and the analog signal detects (PSDETn/RSDETn) are referenced to the selected output timing. When RMODE(1:0) = 01 is selected, the REFCLK leads the valid data window. When RMODE(1:0) = 00, REFCLK is near the center of the valid data window.

TABLE 7. Receive Interface Output Timing Mode

RMODE(1:0)	Output Timing Reference
0 0	REFCLK (Centered)
0 1	REFCLK (Leading)
1 0	RCLKA/RCLKNA
1 1	RCLKn/RCLKNn

The term "word clock" will be used for whichever clock, REFCLK, RCLKA/RCLKNA or RCLKn/RCLKNn, is selected as the output timing reference. When RMODE(1:0) = 1X each channel's complementary RCLKn/RCLKNn runs at 1/10th or 1/20th the incoming data baud rate as selected by DUAL. When RCLKA/RCLKNA is selected as the word clock, the other channels' RCLKn/RCLKNn clocks are duplicates of the A channel clock. When REFCLK is selected, the decoded data and status information outputs are timed to REFCLK and each channel's RCLKn/RCLKNn outputs are held in a constant LOW/HIGH state, respectively. If DUAL is HIGH, the data are synchronously clocked out on both positive and negative edges of the selected word clock at 1/20th the baud rate. If DUAL is LOW, the data are clocked out on only the rising edge of the word clock at 1/10th the data baud rate. See Figure 6 through Figure 8.
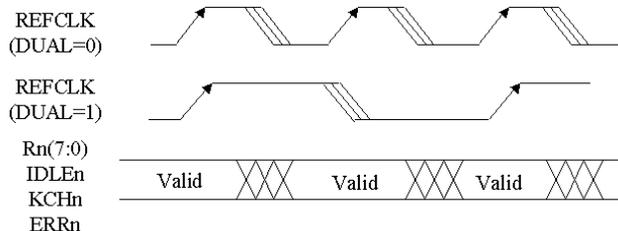
FIGURE 6. Receive Timing, RMODE(1:0) = 00 (REFCLK Centered)
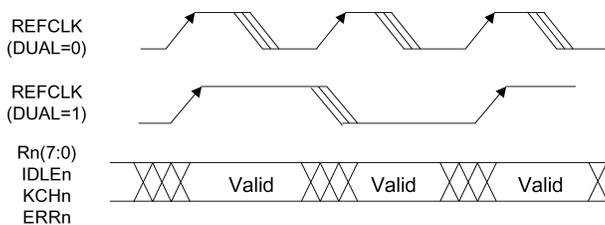
FIGURE 7. Receive Timing, RMODE(1:0) = 01 (REFCLK Leading)
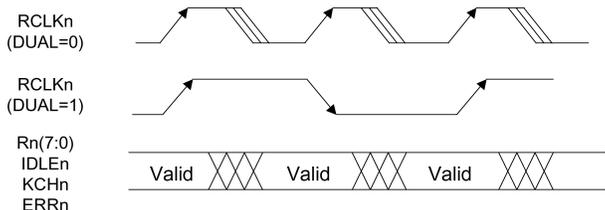
FIGURE 8. Receive Timing, RMODE(1:0) = 1X

Receiver Functional Description (Continued)

The decoded data is clocked into the elastic buffer by the channel's recovered clock and the word clock clocks the data out of the buffers. In order to eliminate rate matching in RMODE(1:0) = 0X, the transmitting device's REFCLK must be frequency-locked to the receiver's word clock. Otherwise, the frequency drift between the recovered clock (which is frequency-locked to the transmitter's REFCLK) and the word clock causes the channel's elastic buffer to gradually fill or empty.

The FIN7216-01 automatically performs rate matching to compensate for any frequency differences between the transmitter's REFCLK and the word clock. The FIN7216-01 does this by deleting or adding IDLE characters. In order to enable rate matching, FLOCK must be LOW. However, the configuration of WSI determines whether the channels are individually aligned or aligned in parallel. See "Word Alignment" section. The system design must guarantee that the frequency at which IDLEs are simultaneously transmitted on each channel accommodates the frequency differences in the system architecture. The IDLE density requirements must be met, or Under-run/Over-run errors could result. Additionally, a continuous stream of IDLE characters should be avoided when rate matching is enabled. The IDLE addition/deletion logic uses the value of the status bits (See Table 9.) to detect the K28.5 IDLE character. The use of continuous IDLE characters will force the FIN7216-01 into the RESYNC state (see Figure 10). The RESYNC mode produces a status bit sequence which has higher priority than the status bit sequence to signal the K28.5 IDLE characters.

The elastic buffers performs at a maximum phase drift of +2 or -2 serial clock bit times between re-synchronizations. This sets a maximum limit on the data "packet" length between K28.5 IDLE characters. This maximum packet length is a function of the differences in frequency of the transmitting device's REFCLK and receiving device's REF-CLK.

Let $\Delta\phi$ represent phase drift in bit times, and let 2(pi) represent one full 10-bit character of phase drift. Limiting phase drift to two bit times means the following inequality must be satisfied:

$$(1) \qquad \Delta\phi \leq \{0.2 \times 2\ pi\}$$

Let L be the number of 10-bit characters transmitted, and let Δf be the frequency offset in ppm. The total phase drift in bit times is given by:

$$(2) \qquad \Delta\phi = \{\Delta f / 10^6\} \times 2\ pi\ L$$

A simple expression for maximum packet length as a function of frequency offset is derived by substituting (2) in (1) and solving for L:

$$(3) \qquad L \leq \{0.2 \times 10^6\}/\Delta f$$

As an example, if the frequency offset is 200ppm, the maximum packet length should not be more than 1K bytes. To increase the maximum packet length L, decrease the frequency offset Δf. Note that if only one K28.5 is transmitted between "packets" of data, it might be dropped during compensation for phase drift. If an IDLE is needed between packets, no less than two K28.5 characters must be transmitted between packets.

Word Alignment

In the Word Alignment mode on the FIN7216-01, all four Tn(7:0) channels on the transmitting device are viewed as a 32-bit word, and the receiving device will recover this identical word. For example, if a transmit pattern was 'ABCD', 'EFGH', 'IJKL', etc., the receiver should not recover data words as 'ABGD', 'EFKH', 'IJOL', etc. The transmit channels must obtain the input data on a common clock (TMODE(2:0) = 000 or 1X0) and the receive channels must present the output data on a common word clock (RMODE(1:0) = 0X or 10).

The receiver's elastic buffer deskews the four channels and aligns them to a common word clock. The elastic buffer can accommodate up to ±6 bit times of channel skew (12 bit times between any two channels) which compensates for circuit imperfections, differences in transmission delay, and jitter. See "Using Multiple FIN7216-01s in Parallel" section. Word alignment requires that a synchronization point be recognized across the aligned receive channels within the ±6 bit time window. In the FIN7216-01, the synchronization point is the first four characters in the Word Sync Sequence (either K28.5+ K28.5+ K28.5- K28.5- or K28.5- K28.5- K28.5+ K28.5+). For example, if channel-to-channel skew is introduced in a 32-bit system, all transmit channels must initiate Word Sync Sequence simultaneously. When the sync point is detected, the recovered data is repositioned in the elastic buffers to align all four channels, and any channel-to-channel skew is removed. Thereafter, all normal data characters are word aligned. In this mode one or two of the final twelve K28.5 IDLE characters in the Word Sync Sequence may be deleted or duplicated in order to correctly recover the transmitted 32-bit word.

Rate matching is accomplished in the World aligned mode by adding or deleting K28.5 IDLE characters simultaneously across the aligned receive channels. The data streams must contain IDLEs inserted simultaneously on all transmit channels according to the IDLE density requirements.

Connecting a device's WSI input to the Master WSO output enables word alignment. The FLOCK and WSI inputs control whether the device will perform rate matching and whether the matching is done on each individual channel or across parallel aligned channels. When WSI is not connected to WSO, word alignment is disabled. When either FLOCK is HIGH or WSI is held LOW, rate matching is disabled. See Table 8.

Receiver Functional Description (Continued)

TABLE 8. Word Alignment and Rate Matching Control

FLOCK	WSI Source	Word Alignment	Rate Matching
0	0	Off	Off
0	1	Off	Enabled, Independent Channels
0	WSO	Enabled	Enabled, Aligned Channels
1	0	Off	Off
1	1	Off	Off
1	WSO	Enabled	Off

Table 8 defines the conditions for word alignment and rate matching. There are essentially four modes of operation.

1. Both word alignment and rate matching are disabled (rows 1, 4, and 5).

2. Rate matching is enabled with independently operating channels. Word alignment is disabled and IDLEs will be duplicated/deleted independently in each channel as needed (row 2).

3. Both word alignment and rate matching are enabled. The receive channels are aligned to the master WSO, and IDLE words will be dropped/duplicated across the aligned channels as required (row 3).

4. Word alignment is enabled and rate matching is disabled. This mode of operation is appropriate for a frequency-locked application where it is desired to align the receive channels without altering the received data streams (row 6).

Using Multiple FIN7216-01s in Parallel

With the use of word alignment mode, multiple FIN7216-01s can be used to provide wider bus widths. In order for word alignment to function properly across multiple devices, the following must occur. Each transmit channel's input data must share a common clock. Also, a common word must be shared clock for all of the receive channels output data. This requires that all transmitting devices use identical REFCLKs, and that TMODE(2:0) = 000 (inputs clocked by REFCLK) or TMODE(2:0) = 1X0 (inputs clocked by TBCA). If inputs are clocked by TBCA, then all transmitting devices must use identical TBCAs. Since all receive channels must use a common word clock, the receiving devices must also use identical REFCLKs and it must be selected as the word clock for all receive channels (RMODE(1:0) = 0X).

If the transmitting and receiving devices' REFCLKs are not identical, then rate matching is required (see Elastic Buffer and Channel Deskew section). Rate matching is accomplished in word aligned mode by adding or deleting IDLE characters simultaneously across all aligned receive channels. One FIN7216-01 is chosen as the "Master" and its' WSO output is driven to the WSI inputs of all the receiving FIN7216-01s, including itself. The Master provides control via the WSO/WSI connection to simultaneously add or drop IDLES on all FIN7216-01s in the case of transmitters that are not frequency locked to the receivers.

WSO uses a simple 3-bit serial protocol, synchronous to the Master channel's word clock. WSO indicates the required synchronization action to all channels of all FIN7216-01s. A steady LOW level indicates no action.

"101" indicates a Word Sync Event has been identified by the Master device's Channel A. The relative timing relationship between receiving a Word Sync Event by each individual channel and receiving '101' allows the channels to perform the initial synchronization to the Master device's Channel A. Once all of the channels have performed the initial synchronization, a '110' on WSO indicates that the next IDLE encountered in the receive data stream should be deleted by all channels. '111' indicates that an IDLE should be inserted by all channels after the next IDLE encountered in the receive data stream. Note that Channel A of the Master device must be an active channel.

Decoder Bypass Mode

When ENDEC is asserted LOW, the FIN7216-01 operates as a 10-bit transceiver. The 8b/10b decoder is bypassed and each receiver channel outputs a 10-bit character Rn(9:0). The outputs KCHn and ERRn become bit Rn8 and Rn9, respectively. As previously noted in the "Encoder Bypass Mode" section, the KCHAR inputs becomes ENCDET which controls comma detection (COMDET) and re-synchronization (byte alignment). When ENCDET is HIGH, the IDLEn output becomes COMDET and is asserted HIGH when the comma pattern is detected in the current 10-bit data character. When ENCDET is LOW, no re-synchronization (byte alignment) or comma detection is performed. In this mode (ENDEC = 0), only the '0011111XXX' version of the comma+ pattern is recognized. The 10-bit interface is commonly found in serializers/deserializers for Fibre Channel (TR/X3.18–199x) and Gigabit Ethernet applications.

When ENDEC is LOW, the circuitry that performs word alignment and insertion/deletion of IDLE characters is disabled. Since rate matching (see elastic buffer and channel deskewing) is disabled, it is necessary that the word clock source must be frequency-locked to the transmitting device in each channel. This can be done by selecting RMODE(1:0) = 11. For other values of RMODE(1:0), frequency lock must be guaranteed by the system design. When in the X20 clock multiplier mode (DUAL = 1) and RMODE(1:0) = 1X, the output character in each channel containing the comma pattern (0011111XXX) is timed to RCLKn/RCLKNn such that COMDET is asserted on the falling of RCLKn. This is accomplished without stretching or slivering the recovered clock by adjusting the latency through the elastic buffer. When the comma pattern changes the framing boundary, any data characters prior to a COMDET transition on the falling edge of RCLKn may be corrupted.

Receiver Functional Description (Continued)

Data not encoded/decoded (Bypass Mode)

TX & RX Clocks, must be Frequency locked

TX Latency reduced by 10bc

ENDEC Pin
(Encoder / Decoder)

Data is encoded/decoded (8 Bit Mode)

The RX elastic buffer can be exercised

0

1

KCHn, ERRn pins become **Rn8, Rn9**
C/Dn, WSENn pins become **Tn8, Tn9**
IDLEn = COMma **DET**ect **(COMDETn)**

KCHAR = ENable **C**omma **DET**ect **(ENCDET)**

KCHAR=0

KCHAR=1

No Action

If DUAL = 1 &
RMODE = 1X

FALSE

TRUE

COMDETn
will assert
on Rising
edge of
RefCLK /
RCLKn

COMDETn
will assert
on Falling
edge of
RCLKn

Note: 0=False, 1=True

WSENn =

0

1

C/Dn =

0

1

Encode &
Serialized
Tn(7:0)

KCHAR =

0

1

K28.5
Character

Encode data
on Tn(7:0)
using Special
K-character
Table

Complete
The 16 -
Character
Word
Sync
Sequence

FIGURE 9. FIN7216-01 ENDEC Flow Control

Receiver State Machine

Each channel has a Loss of Synchronization State Machine (LSSM) detects loss of bit, channel, word and word clock synchronization. The three LSSM state conditions, LOSS_OF_SYNC; RESYNC; and SYNC_ACQUIRED, are diagrammed in Figure 10. Upon power-up, the LSSM enters loss of Sync State. After power-up, the receiver LSSM goes into a RESYNC state when the 10-bit data character contains a valid comma character. A valid non-comma character causes the receiver to enter a SYNC_ACQUIRED state, indicating normal receive operation. The LSSM will re-enter RESYNC if four consecutive words with comma or a comma indicating a change of framing boundary is transmitted. A LOSS_OF_SYNC is entered after the invalid transmission counter reaches state 4 (see Figure 10). This operation is accomplished using a simple up-down counter that increments/decrements on an invalid/valid 8B/10B encoded transmission. The LSSM will stay in LOSS_OF_SYNC until a valid comma transmission is received; then the state changes back to RESYNC. As noted earlier, the RESYNC state is entered whenever the 10B framing boundary is changed or the Word Sync Sequence is received. When ENDEC is LOW, the ERRn, KCHn and IDLEn outputs are re-defined and the decoder and associated LSSM logic in each channel is unused. The states of ERRn, KCHn, and IDLEn are show in Table 9. The received data is available in all states of the LSSM.

Receiver Functional Description (Continued)
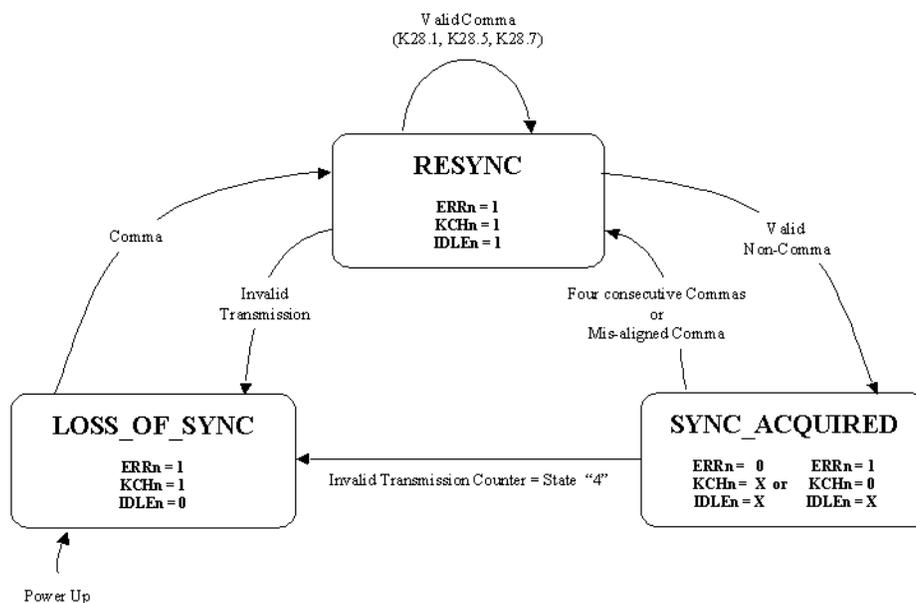
**FIGURE 10. State Diagram of the Loss of Synchronization State Machine
(see application note for more detail)**
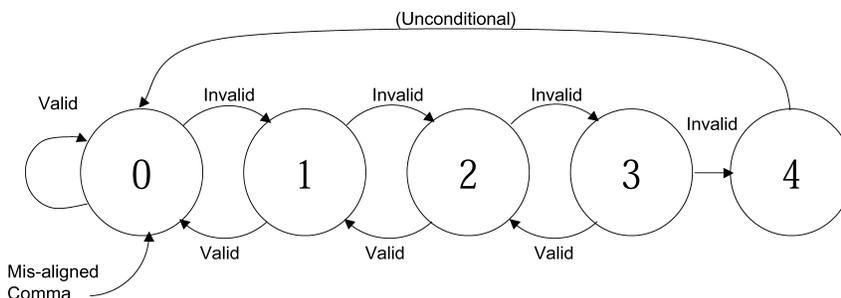
FIGURE 11. State Diagram of the Invalid Transmission counter

Link Status Outputs

Multiple error conditions are encoded in each channel of the receiver and reported on the output status pins, ERRn, KCHn and IDLEn. Some conditions can occur simultaneously, so the states are ranked by priority. See Table 9. In the case where two or more states apply, the higher priority condition is reported (1 is highest priority). For example, if both IDLE Detected and RESYNC occur, only a RESYNC is reported because it has higher priority. The current link status asserted on the ERRn, KCHn, and IDLEn outputs will be timed such that they are synchronous to the appropriate data on the parallel output bus (Rn9:0). The only exception to this is the Under-run/Over-run indication, which is asserted coincident with the duplicated character when an under-run occurs, and is asserted following the deleted character (i.e., on the cycle where the deleted character should have appeared) when overrun occurs.

Receiver Functional Description (Continued)

TABLE 9. Receiver Status Signals

ERRn	KCHn	IDLEn	Priority	Link Status
0	0	0	7	Valid Data Transmission: A valid 10B data character with correct disparity was received. The correctly decoded version of this character is on Rn(7:0)
0	0	1	1	Under-run/Over-run Error: The elastic buffer has not been able to add/drop an IDLE when required. Data on Rn(7:0) is invalid
0	1	0	6	Kx.y Special Character Detected (not IDLE): A valid 10B special character with correct disparity was received. The correctly decoded version of this character, per Table 4, is on Rn(7:0)
0	1	1	5	IDLE Detected: A valid IDLE character (K28.5) with correct disparity was received. The correctly decoded version of this character, per Table 4, is on Rn(7:0)
1	0	0	3	Out-of-Band Error Detected: A character was received which was not a valid 10B data or control character. Data on Rn(7:0) is invalid
1	0	1	4	Disparity Error Detected: A valid 10B character was received which did not have the expected disparity. Rn(7:0) is invalid
1	1	0	2	Loss of Synchronization: The receiver state machine is in the Loss-of-Sync state. Data on Rn(7:0) is invalid.
1	1	1	2	RESYNC: The receiver state machine is in the Re-Synchronization state. Data on Rn(7:0) is a decoded version of K28.1, K28.5, or K28.7.

Loopback Operation

Each channel has a loop back enable pin, LBENn(1:0), that controls an internal loopback data path in order to provide for on-chip diagnosis. See Table 10.

TABLE 10. Loopback Mode Selection

LBENn(1:0)	Loopback Mode
00	Normal Operation
01	Internal Parallel Loopback
10	Internal Serial Loopback
11	Reserved

When LBENn(1:0) = 10, the Serial Loopback configuration is selected. In this mode, a path (LBTXn) is enabled between the transmitter's serial data and the input of the CDR. This means that parallel data enters the local device on Tn(7:0), is encoded, serialized, looped-back, deserialized, and decoded when ENDEC is HIGH. This configuration allows for the verification of operation of the FIN7216-01 prior to establishing an external connection. LBENn does not affect the data on PTXn/RTXn outputs. When ENDEC is LOW TN(9:0) is serialized, looped back, and deserialized.

When LBEN(1:0) = 01, parallel loopback is selected. In Parallel Loopback mode, an internal *REFCLK copy is

used in the receiver as the word clock and TMODE(2:0) is internally set to 000, which causes the parallel loopback data from the receiver to be frequency-locked to the device's REFCLK. However, the receiver parallel output data timing that is normally set by the value of RMODE(1:0) will not match the normal operation system timing. Because of this, the parallel output data should be ignored.

When ENDEC is HIGH, the Rn(7:0) outputs are looped back to the Tn(7:0) inputs (Figure 12). WSENn does not have a loopback source and is internally connected to a logic LOW. KCHAR is internally connected to a logic HIGH. The C/Dn input is internally connected to the KCHn output to allow a data character, special character, or IDLE (K28.5) to be looped back properly. When the link is in the Loss of Sync (LOS) or RESYNC states, C/Dn is asserted and the data path is set to 0xBC so that an IDLE will be transmitted. This guarantees that IDLE and special characters will be correctly looped back along with normal data, and also has the effect of looping back the data received as a normal data character when a disparity error, out-of-band character, or under-run/over-run link status condition occurs.

When ENDEC is LOW, Rn(9:0) are looped back to TN(9:0).
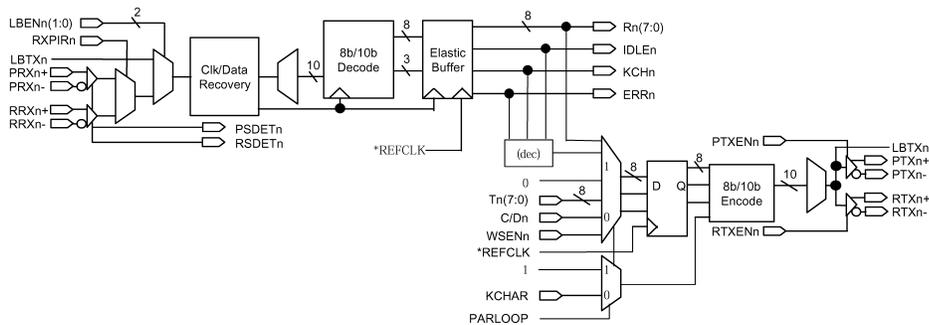
FIGURE 12. Parallel Loopback Mode Operation

Receiver Functional Description (Continued)

The parallel loopback mode provides for rate-matching in the receiver elastic buffers in the same manner as in normal operation. This avoids receiver over-run/under-run errors in the local device if it and the remote transmitter's REFCLK are not frequency-locked. Please note that the LBENn(1:0), RXP/Rn, PTXENn, RTXENn and BIST inputs must all be configured appropriately in order for end-to-end parallel loopback to function correctly in a user environment. Parallel Loopback mode is internally disabled when BIST mode is enabled.

Built-In Self Test Operation

When BIST is asserted HIGH, the Built-In Self Test is enabled, and TMODE(2:0) is internally set to a value of 000. ENDEC is internally asserted HIGH after initiation of the BIST mode. A Word Sync Sequence is then sent by the transmitter which re-centers the elastic buffers in the receive channel. Then, a 256 byte incrementing data pattern (prior to encoding) is sent repeatedly by all transmit channels followed by three unique (K28.5) IDLE characters. Note that this incrementing pattern plus three IDLEs will cause both disparities of each data character and the

IDLE character to be transmitted, and contains a sufficient IDLE density for any application requiring IDLE insertion/deletion. If the receiver word clock is not frequency locked to the transmitter's REFCLK, the user conditions the device appropriately to IDLE insertion/deletion. (see Table 8, Word Alignment and Rate Matching Control)

Each receiver recognizes this incoming data pattern and any errors will be detected. Each receiver indicates that the pattern is received correctly by the assertion of a LOW on TBERRn. A HIGH on TBERRn means that an error has occurred. When BIST transitions from LOW to HIGH during the initiation of this mode, TBERRn is asserted HIGH.

TBERRn is reset LOW once the transmission of one or more IDLE characters followed by a 256 byte sequential pattern with no errors has occurred. Each receive channel functions independently and are not word-aligned. Please note that Serial Loopback mode and receiver output timing mode selection via RMODE(1:0) operate independently of BIST mode, but BIST mode disables Parallel Loopback mode.
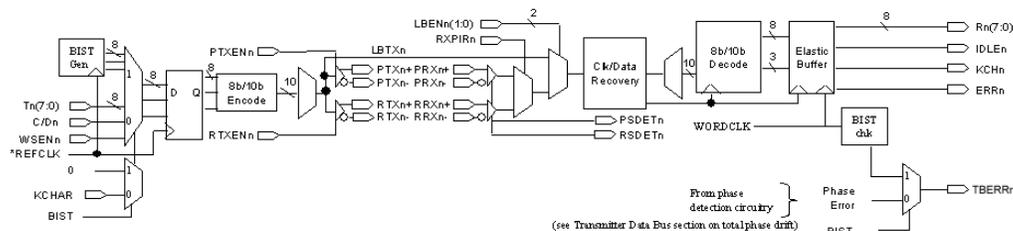
FIGURE 13. BIST Mode Operation

Power Up

During the power up sequence, the chip initializes, the input skew buffers and the receiver elastic buffers are re-centered, all flip-flops are cleared, and all synchronized state machines enter LOS.

Absolute Maximum Ratings(Note 2)

Power Supply Voltage (any V_{DDX})	-0.5V to +3.8V
PECL Differential Input Voltage	-0.5V to V_{DD} +0.5V
TTL Input Voltage	-0.5V to 5.5V
TTL Output Voltage	-0.5V to V_{DD} +0.5V
TTL Output Current	50 mA
PECL Output Current	50 mA
Case Temperature Under Bias (T_C)	-55ºC to +125ºC
Storage Temperature (T_{STG})	-65ºC to +150ºC
HBM ESD Level	>2000V

Recommended Operating Conditions

Supply Voltage (V_{DD})	+3.3V ± 5%
Operating Temperature Range	0°C Ambient to 95°C Case

Note 2: Absolute maximum ratings are DC values beyond which the device may be damaged or have its useful life impaired. The datasheet specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside datasheet specifications.

DC Electrical Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
TTL Outputs (Rn(7:0), KCHn, IDLEn, ERRn, RCLKn/RCLKNn, TBERRn, PSDETn, RSDETn, WSO)						
V_{OH}	TTL Output HIGH Voltage	I_{OH} = -1.0 mA	2.4			V
V_{OL}	TTL Output LOW Voltage	I_{OL} = +1.0 mA			0.5	V
I_{OZ}	TTL Output Leakage Current	When Set to High-Impedance State Through JTAG.			±100	µA
TTL Inputs (TBCn, Tn(7:0), C/Dn, WSENn, KCHAR, RATE, BIST, LBENn(1:0), TMODE(2:0), RMODE(1:0), DUAL, PTXENn, RTXENn, RXP/Rn, RESETN, ENDEC, WSI, FLOCK, TRSTN, TDI, TDO, TMS, TCK)						
V_{IH}	TTL Input HIGH Voltage		2.0		5.5	V
V_{IL}	TTL Input LOW Voltage		0		0.8	V
I_{IH}	TTL Input HIGH Current	V_{IN} = 2.4V			20	µA
I_{IL}	TTL Input LOW Current	V_{IN} = 0.5V			-100	µA
PECL Inputs (REFCLK/REFCLKN)						
V_{IH}	PECL Input HIGH Voltage		V_{DD} - 1.1		V_{DD} - 0.7	V
V_{IL}	PECL Input LOW Voltage		V_{DD} - 2.0		V_{DD} - 0.8	V
I_{IH}	PECL Input HIGH Current	V_{IN} =$V_{IH(MAX)}$			200	µA
I_{IL}	PECL Input LOW Current	V_{IN} =$V_{IL(MIN)}$	-20			µA
ΔV_{IN}	PECL Input Differential Peak-to-Peak Voltage Swing	(Note 3)	200			mV
V_{CM}	PECL Input Common-Mode Voltage		V_{DD} -1.5		V_{DD} - 0.7	V
V_{BIAS}	REFCLKP/REFCLKN, PRXn+/-, and RRXn+/- Internal Input Bias Voltage			V_{DD} /2		V
PECL Outputs (PTXn±, RTXn±)						
ΔV_{OUT}	PECL Differential Peak-to-Peak Output Voltage Swing	| PTXn+ - PTXn- | (Note 3) 50Ω to GND. External Pull-Down Resistors Not Required.	500		1300	mV
PECL Inputs (PRXn±, RRXn±)						
ΔV_{IN}	PECL Input Differential Peak-to-Peak Voltage Swing		200		1300	mV
Miscellaneous						
V_{DD}	Power Supply Voltage	3.3V +/- 5%	3.14		3.47	V
P_D	Power Dissipation	Maximum at 3.47 V, at Max Operating Frequency,		1.9	2.3	W
I_{DD}	Supply Current	Redundant I/O Off, Outputs Open.			660	mA

Note 3: Single-ended measurement results are quoted here. Differential techniques used in Fibre Channel would yield values that are twice the magnitude. See diagram below.

AC Electrical Characteristics

In the following tables, "bc" refers to encoded bit clock period. For example, At the max rate of 1.36 Gbps, bc» 735 ps
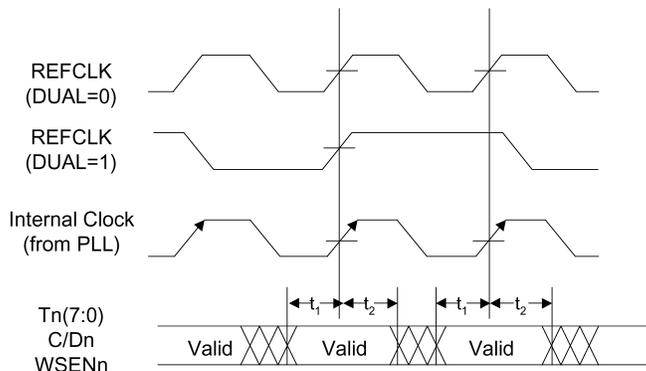
FIGURE 14. Transmit Input Timing Waveforms with TMODE = 000
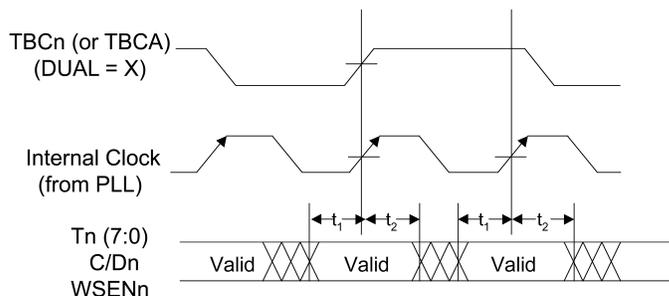
FIGURE 15. Transmit Input Timing Waveforms with TMODE = 10X

TABLE 11. Transmit Input AC Characteristics with TMODE = 000 or TMODE = 10X

Symbol	Parameters	Conditions	Min	Max	Units
t_1	Input Setup Time to the Rising Edge of REFCLK or TBCn	Measured between the valid data level of the input and the 1.4V point of REFCLK or TBCn	1.5		ns
t_2	Input Hold Time after the Rising Edge of REFCLK or TBCn		1.0		ns
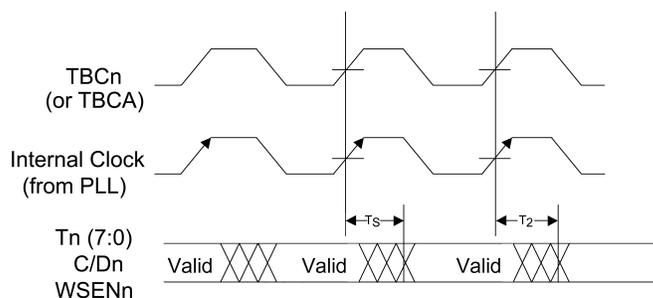
FIGURE 16. Transmit Input Timing Waveforms with TMODE = 11X (ASIC-Friendly Timing)

TABLE 12. Transmit Input AC Characteristics with TMODE = 11X

Symbol	Parameters	Conditions	Min	Max	Units
t_S	Input Skew Relative to the Rising Edge of TBCn or TBDA	Measured between the valid data level of the input and the 1.4V point of TBCn or TBCA. bc = bit clock.		2.2	bc

AC Electrical Characteristics (Continued)
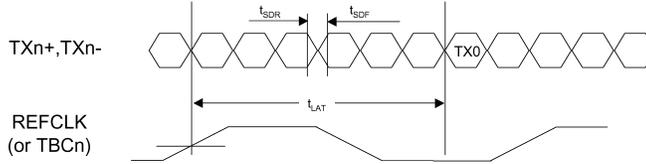
FIGURE 17. Transmit Serial Timing Waveforms

TABLE 13. Transmit Serial AC Characteristics

Symbol	Parameters	Conditions	Min	Max	Units
t_{SDR} t_{SDF}	TXn+/- Rise and Fall Time	Measured between 20% to 80% of the valid data level.		330	ps
t_{LAT}	Latency, REFCLK to TX0	ENDEC = 1 TMODE = 000	22bc – 0.5ns	22bc + 1.0ns	
	Latency, TBCA to TX0	ENDEC = 1 TMODE = 10X	36bc + 0.7ns	38bc + 1.8ns	bc + ns
	Latency, TBCB/C/D to TX0	ENDEC = 1 TMODE = 101	32bc + 0.7ns	42bc + 1.8ns	
t_J	Serial Data Output Total Jitter (p-p)	IEEE 802.3z Clause 38.69,		192	ps
t_{DJ}	Serial Data Output Deterministic Jitter (p-p)	IEEE 802.3z Clause 38.69,		80	ps
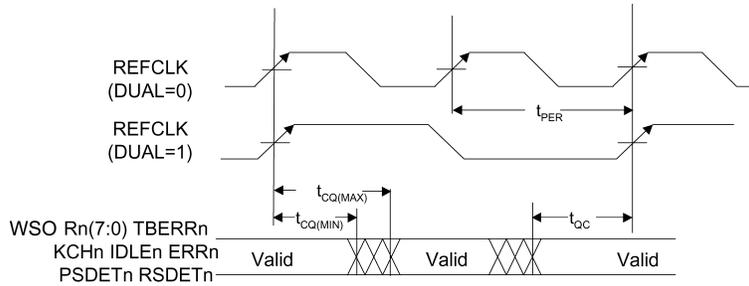
FIGURE 18. Receive Output Timing Waveforms with RMODE = 00 or 01

TABLE 14. Receive Outputs AC Characteristics with RMODE = 00 or 01

Symbol	Parameters	Conditions	Min	Max	Units
t_{CQ}	REFCLK Rising Edge to TTL Output Transition	RMODE = 00; bc = bit clock	2.3 ns - 0 bc	5.5 ns - 0 bc	ns
t_{CQ}	REFCLK Rising Edge to TTL Output Transition	RMODE = 01; bc = bit clock	2.3 ns - 2 bc	5.5 ns - 2 bc	ns
t_{QC}	TTL Output Transition to REFCLK Rising Edge		$t_{PER} - t_{CQ(MAX)}$	$t_{PER} - t_{CQ(MIN)}$	ns

AC Electrical Characteristics (Continued)

RCLKn/RCLKNn (DUAL=0)

RCLKn/RCLKNn (DUAL=1)

t_{PER}

$t_{CQ(MAX)}$

$t_{CQ(MIN)}$

t_{QC}

WSO Rn(7:0) TBERRn
KCHn IDLEn ERRn
PSDETn RSDETn

Valid   Valid   Valid
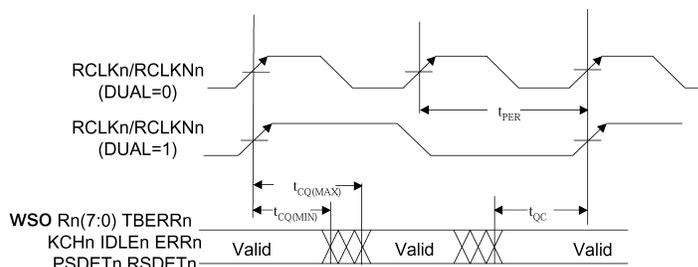
FIGURE 19. Receive Output Timing Waveforms with RMODE = 10 or 11

TABLE 15. Receive Outputs AC Characteristics with RMODE = 10 or 11

Symbol	Parameters	Conditions	Min	Max	Units
t_{CQ}	RCLKn/RCLKNn Rising Edge to TTL Output Transition	RMODE = 10 or 11 bc = bit clock	-1.25 ns + 4 bc	1.25 ns + 4 bc	ns
t_{QC}	TTL Output Transition to RCLKn/RCLKNn Rising Edge		t_{PER} - $t_{CQ(MAX)}$	t_{PER} - $t_{CQ(MIN)}$	ns
DC	RCLKn/RCLKNn Duty Cycle	Measured at 1.4 V;DUAL = 1	50% - 1 ns	50% + 1 ns	ns

t_4

t_3
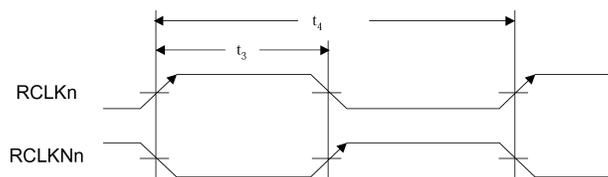
RCLKn

RCLKNn

FIGURE 20. RCLKn and RCLKNn Timing Waveforms with DUAL = 1

TABLE 16. General Receive AC Characteristics

Symbol	Parameters	Conditions	Min	Max	Units
t_3	Delay Between Rising Edge of RCLKn to Rising Edge of RCLKNn	t_{RX} is the bit period of the incoming data on Rx.	10 x t_{RX} -500	10 x t_{RX} +500	ps
Δt_3	RCLKn to RCLKNn Skew $Delay = \dfrac{10}{fbaud} \pm \Delta t3$	Deviation of RCLKn Rising Edge to RCLKNn Rising Edge. Nominal Delay is 10 bi	-500	500	ps
t_4	Period of RCLKn and RCLKNn	Whether or not locked to Serial Data, independent of DUAL Input.	0.99 x t_{REFCLK}	1.01 x t_{REFCLK}	
Δt_4	Deviation of RCLK/RCLKN Period from REFCLK Period $t_{RCLK} = t_{REFCLK} \pm \Delta t_4$	Whether or not locked to Serial Data, independent of DUAL Input.	-1.0	1.0	%
t_r, t_f	Output Rise and Fall Time	Between $V_{IL(MAX)}$ and $V_{IH(MIN)}$ into 10pF load		2.4	ns
R_{LAT}	Latency from RX0 to REFCLK or RCLK	ENDEC = 1, Re-center only	68.25bc - 0.6ns	81.25bc + 1.5ns	bc + ns
		ENDEC = X, Re-center + Drift	48.5bc - 1.6ns	102.5bc + 4.1ns	
t_{LOCK} (Note 4)	Data Acquisition Lock Time	Using K28.5+/K28.5-pattern.		100	bc
t_{JTD}	Receive Data Total Jitter Tolerance (p-p)	IEEE 802.3z Clause 38.69, tested on a sample basis at 1.25 Gbps.		600	Ps
D_{JTD}	Receive Data Deterministic Jitter Tolerance (p-p)	IEEE 802.3z Clause 38.69, tested on a sample basis at 1.25 Gbps.		370	Ps

Note 4: The probability of correct data acquisition and recovery is 99% per FC-PH 4.3 Section 5.3.

REFCLK

t_H

t_L

$V_{IH(MIN)}$

$V_{IL(MAX)}$
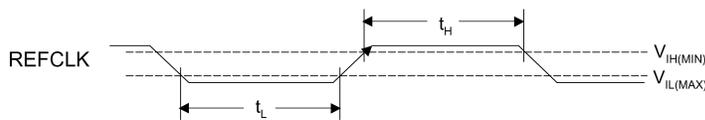
FIGURE 21. REFCLK Timing Waveforms

AC Electrical Characteristics (Continued)

TABLE 17. Reference Clock Requirements

Symbol	Parameters	Conditions	Min	Max	Units
FR	Frequency Range	DUAL = 0, RATE = 1	98	136	MHz
		DUAL = 1, RATE = 1	49	68	
		DUAL = 0, RATE = 0	49	68	
		DUAL = 1, RATE = 0	24.5	34	
FO	Frequency Offset	| REFCLK (Tx) - REFCLK (Rx) | = max offset between Tx and Rx device REFCLKs on one serial link.	-200	200	ppm
DC	REFCLK Duty Cycle	Measured at 1.4V	35	65	%
t_H, t_L	REFCLK and TBC Pulse Width		3		ns
t_{RCR}, t_{RCF}	REFCLK Rise and Fall Time	Between $V_{IL(MAX)}$ and $V_{IH(MIN)}$		1.5	ns
REFCLK Jitter	REFCLK Jitter	Peak-to-Peak Jitter at FIN7216-01 REFCLK Input.		100	ps

TTL Input and Output Rise and Fall Time

Serial Input Rise and Fall Time

Receiver Input Eye Diagram Jitter Tolerance Mask
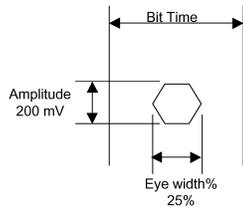
FIGURE 22. Parametric Measurement Information

TTL AC Output Load

Serial Output Load
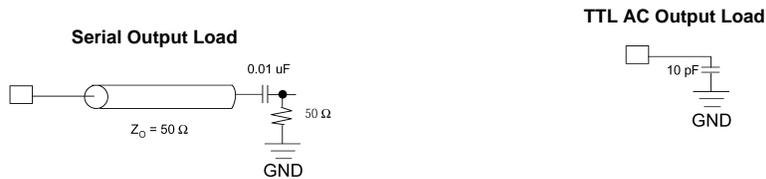
FIGURE 23. Parametric Test Load Circuit

Package Thermal Considerations

The FIN7216-01 is packaged in a 256-pin, 27mm, thermally-enhanced BGA in a 20x20 array which offers excellent electrical characteristics, good thermal performance and small size. This package uses an industry-standard footprint. The package construction is shown in Figure 24.
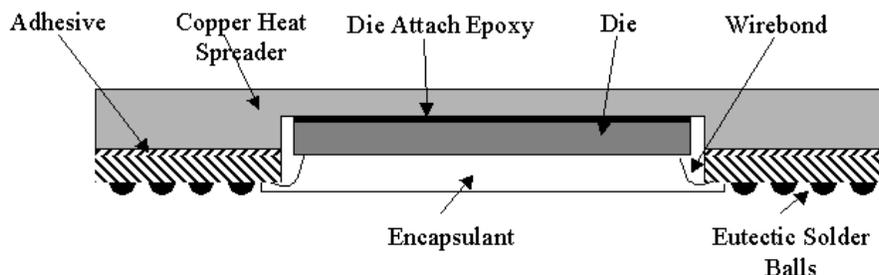
FIGURE 24. Thermal Resistance

TABLE 18. Thermal Resistance

Symbol	Description	Value	Units
θ_{ca}	Thermal Resistance from case-to-ambient in still air including conduction through the leads.	13	°C/W
θ_{ca-100}	Thermal Resistance from case-to-ambient with 100 LFM airflow	11.5	°C/W
θ_{ca-200}	Thermal Resistance from case-to-ambient with 200 LFM airflow	10.5	°C/W
θ_{ca-400}	Thermal Resistance from case-to-ambient with 400 LFM airflow	9.5	°C/W
θ_{ca-600}	Thermal Resistance from case-to-ambient with 600 LFM airflow	8.7	°C/W

Moisture Sensitivity Level

This device is rated at with a Moisture Sensitivity Level 3 rating.

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Physical Dimensions inches (millimeters) unless otherwise noted

A 27±0.2
B
PIN A1 ID
27±0.2

// 0.15 C   0.9±0.1   1.4 MAX /G\
C
SEATING PLANE   0.15 C   0.6 ±0.1
DETAIL "Z"

0.2 C
TOP VIEW

DETAIL "Z"
24.13
C   SIDE VIEW

45°   0.5
1.27

(1.435)   0.5
45°

DETAIL "V"   DETAIL "Y"
Y
(1.435)
14.56MAX

DETAIL "W"   A   1   20   DETAIL "X"   Ø0.75±0.1
14.56MAX   0.3 M C A B
/F\   0.15 M C   (256 BALLS)
BOTTOM VIEW
17 18 19 20
45°
1.1   0.5
1 2 3 4
PIN A1 CHAMFER
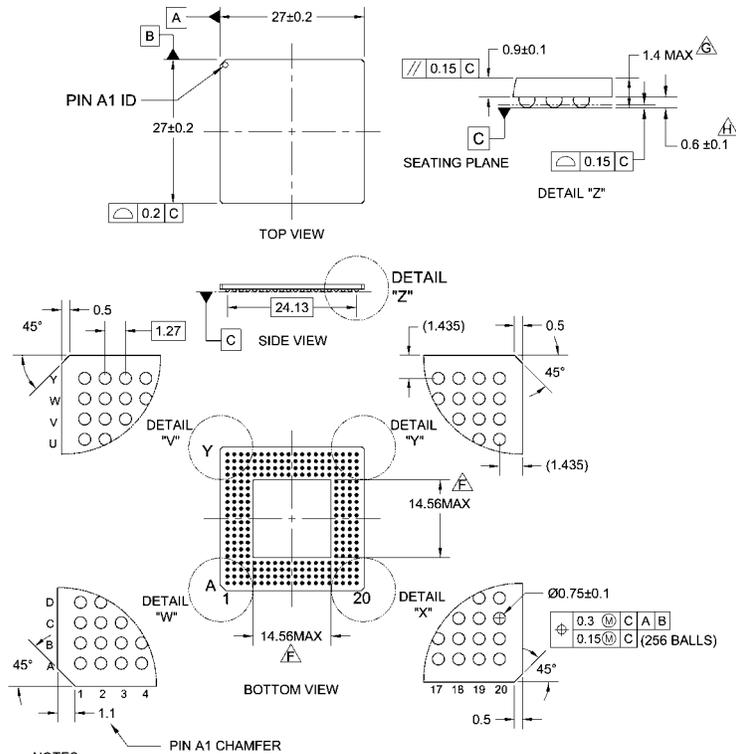
NOTES:
A) ALL DIMENSIONS IN MILLIMETERS.
B) CONFORMS TO JEDEC MO-149. Varaition (BG-2X)
C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
D) ROW NAMING ORDER;
    A B C D E F G H J K L M N P R T U V W Y
E) COLUMN NAMING ORDER;
    1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20
F) ENCAPSULATION SIZE WILL VARY WITH CAVITY SIZE.
G) MAX STAND OFF FROM PCB AFTER MOUNTING.
H) FREE BALL HEIGHT. NOT ATTACHED TO PCB.

BGA256ArevB

256-Ball Thermally-Enhanced Ball Grid Array (TBGA), JEDEC MO-149, 1.27mm Pitch, 27mm Square
Package Number BGA256A

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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