January 1983

EUROTECHNIQUE

ET2141/ETL2141 Family
4096 × 1 Static Random Access Memories

General Description

These 4096-word by 1-bit static random access memories are fabricated using N-channel silicon-gate technology XMOS. All internal circuits are fully static and therefore require no clocks or refreshing for operation. The data is read out nondestructively and has the same polarity as the input data. Separate input/output pins are provided.

The separate chip select input allows easy memory expansion by OR-tying individual devices to a data bus and automatically powers down the ET2141.

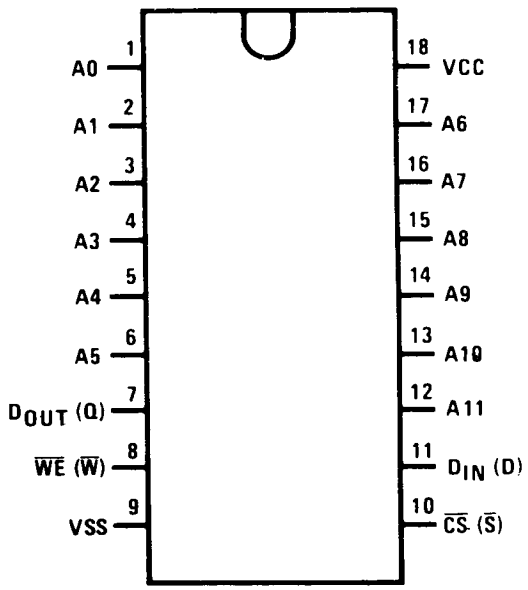
The output is held in high impedance state during write to simplify common I/O applications.

Features

- All inputs and outputs directly TTL compatible
- Static operation - no clocks or refreshing required
- Automatic power down
- Low power 225 mW typical
- High speed - down to 120 ns access time
- Three-state output for bus interface
- Separate Data In and Data Out pins
- Single +5V supply
- Standard 18-pin dual-in-line package

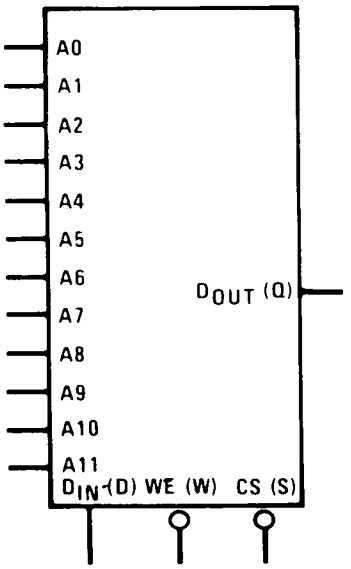
Connection Diagram*

Dual-In-Line Package



TOP VIEW

Logic Symbol*



Pin Names

A0–A11	Address Inputs
WE (W)	Write Enable
CS (S)	Chip Select
DIN (D)	Data In
DOUT (Q)	Data Out
VCC	Power (+5V)
VSS	Ground

Truth Table*

CS (S)	WE (W)	DIN (D)	Dout (Q)	Mode	Power ET 2141
H	X	X	HiZ	Not Selected	Standby
L	L	H	HiZ	Write 1	Active
L	L	L	HiZ	Write 0	Active
L	H	X	Dout	Read	Active

*Symbols in parentheses are industry standard.

Printed in France

Functional Description

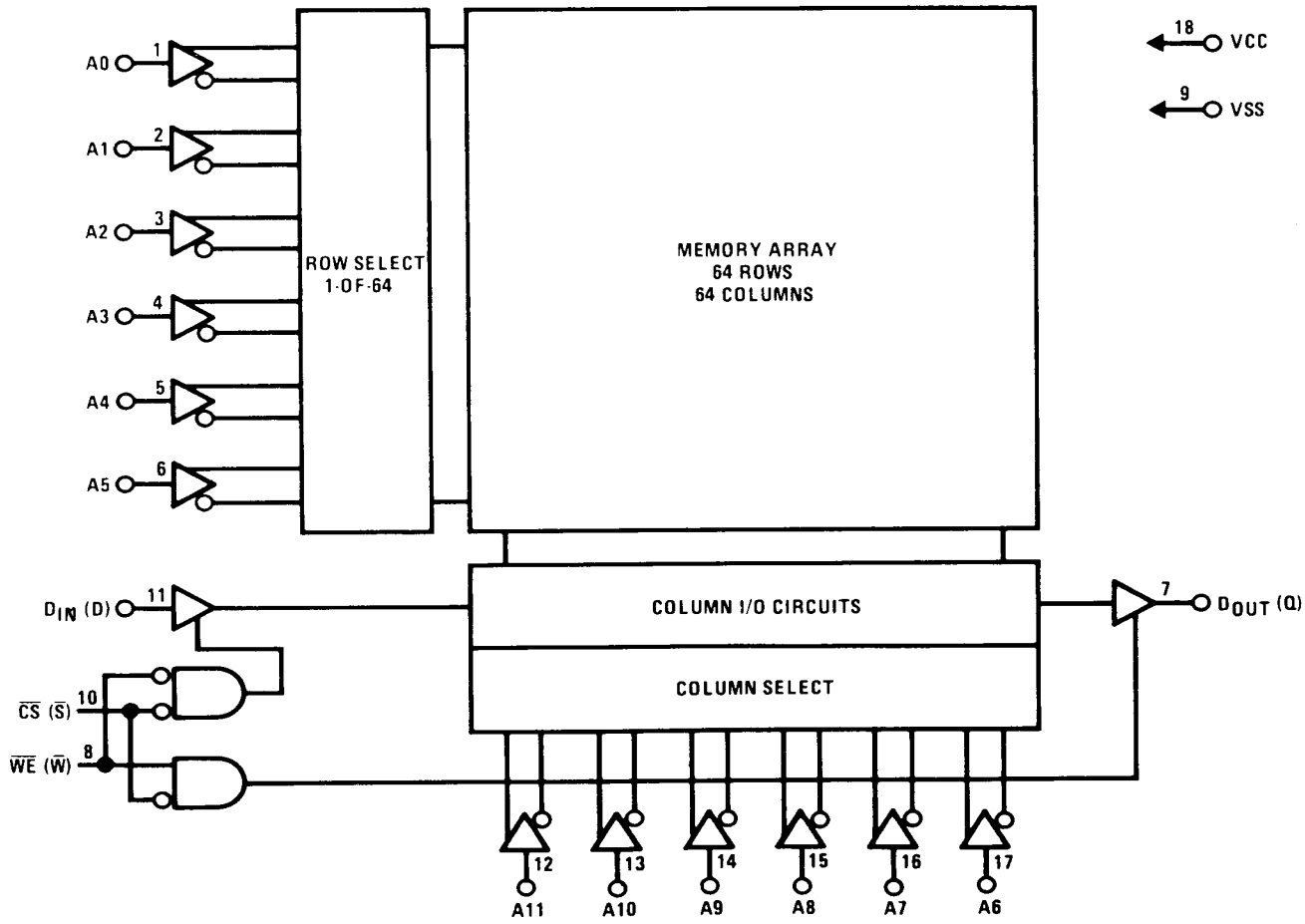
Two pins control the operation of these RAMS-Chip Select ($\overline{CS}$) enables write and read operations and controls TRI-STATING of the data-output buffer. Write Enable ($\overline{WE}$) chooses between READ and WRITE modes and also controls output TRI-STATING. The truth table details the states produced by combinations of the $\overline{CS}$ and $\overline{WE}$ controls. For ET 2141 chip Select deselect the device putting it in the low power Standby mode. READ-cycle timing is shown in the section on Switching Time Waveforms. $\overline{WE}$ is kept high. Independent of $\overline{CS}$, any change in address code causes new data to be fetched and brought to the output buffer. $\overline{CS}$ must be low, however, for the output buffer to be enabled and transfer the data to the output pin.

Address access time, t_A, is the time required for an address change to produce new data at the output pin, assuming $\overline{CS}$ has enabled the output buffer prior to data arrival. Chip Select access time is the time required for $\overline{CS}$ to enable the output buffer and transfer previously fetched data to the output pin. Operation with $\overline{CS}$ continuously held low is permissible.

WRITE-cycle timing is shown in the section on Switching Time Waveforms. Writing occurs only during the time both $\overline{CS}$ and $\overline{WE}$ are low. Minimum write pulse width, t_{WP}, refers to this simultaneous low region. Data set-up and hold times are measured with respect to whichever control first rises. Successive write operations may be performed with $\overline{CS}$ continuously held low $\overline{WE}$ then is used to terminate WRITE between address changes. Alternatively, $\overline{WE}$ may be held low for successive WRITES and $\overline{CS}$ used for WRITE interruption between address change.

In any event, either $\overline{WE}$ or $\overline{CS}$ (or both) must be high during address transitions to prevent erroneous WRITE.

Block Diagram*



*Symbols in parentheses are industry standard.

Absolute Maximum Ratings

Voltage on any Pin Relative to VSS	−3.5V to +7V
Storage Temperature Range	−65°C to +150°C
Power Dissipation	1.2W
DC Output Current	20 mA
Bias Temperature Range	−10°C to +85°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (VCC)	4.5	5.5	V
Ambient Temperature (TA)	0	+70	C

DC Electrical Characteristics TA = 0°C to +70°C, VCC = 5V ±10% (Note 1)

SYMBOL	PARAMETER	CONDITIONS	ET 2141 -2L, -3L, -4L, -5L		ET 2141 -2, -3,		ET 2141 -4, -5		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	
VIH	Logical "1" Input Voltage		2	6	2	6	2	6	V
VIL	Logical "0" Input Voltage		-1	0,8	-1	0,8	-1	0,8	V
VOH	Logical "1" Output Voltage	IOH = −4 mA	2,4		2.4		2,4		V
VOL	Logical "0" Output Voltage	IOL = 8,0 mA		0,4		0,4		04	V
ILI	Input Load Current	VIN = 0 to 5,25 V. VCC = Max		10		10		10	μA
ILO	Output Leakage Current	VO = 4,5V to Gnd $\overline{CS}$ = VIH, VCC = Max		10		10		10	μA
ICC	Power Supply Current	VCC = Max, $\overline{CS}$ = VIL Outputs Open		40		50		70	mA
ISB	Standby Current	VCC = Min to Max $\overline{CS}$ = VIH		5		10		12	mA
IPO	Peak Power ON Current	VCC = Gnd to VCC Min. $\overline{CS}$ = Lower of VCC or VIH (Min)		5		10		12	mA
IOS	Output Short Circuit	Vout = GND to VCC (Note 1)	−140	140	−140	140	−140	140	mA

Capacitance TA = 25 °C, f = 1.0 MHz (Note 2)

Symbol	Parameter	Conditions	ET 2141		Units
			Min	Max	
COUT	Output Capacitance	VOUT = 0V		6	pF
CIN	Input Capacitance	VIN = 0V		5	pF

AC Test Conditions (Note 3)

Input Pulse Levels	
ET 2141	GND to 3.0 V
ETL 2141	
Input Rise and Fall Times	≤ 10 ns
Input and Output Timing Levels	0,8V;2V
Output Load	I OL = 8mA, I OH = -4 mA and 100pF

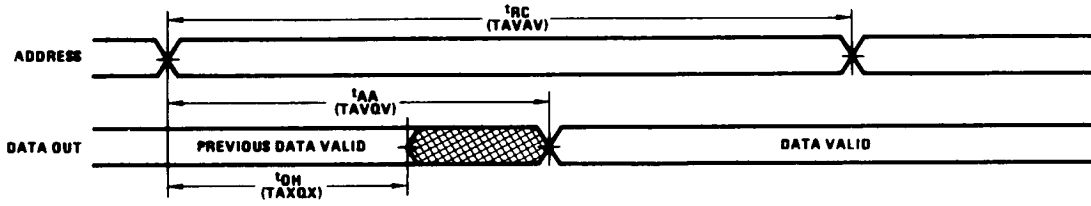
Note 1 : Maximum duration 60 seconds.
Note 2 : This parameter is guaranteed by periodic testing.
Note 3 : These circuits require 500 ns time delay after VCC reaches the specified minimum limit to ensure proper operation after power on. This allows the internally generated substrate bias to reach its functional level.

Read Cycle AC Electrical Characteristics TA = 0°C to +70°C, VCC = 5V ±10%

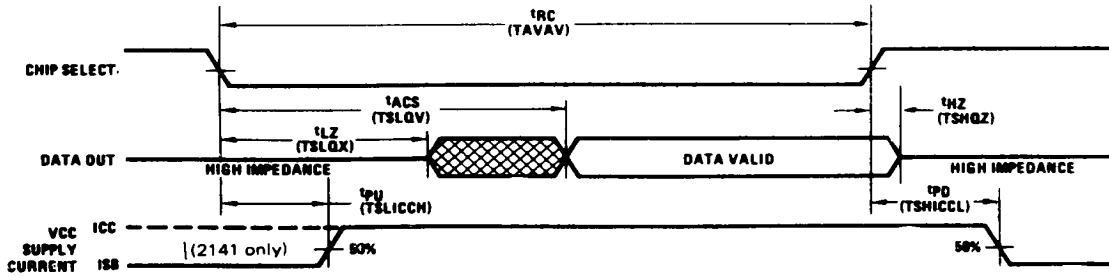
SYMBOL		PARAMETER	ET 2141-2 ETL 2141-2		ET 2141-3 ETL 2141-3		ET 2141-4 ETL 2141-4		ET 2141-5 ETL 2141-5		UNITS
ALTERNATE	STANDARD		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	TAVAV	Read Cycle Time	120		150		200		250		ns
t_{AA}	TAVQV	Adress Access Time		120		150		200		250	ns
t_{ACS1}	TSLQV	Chip Select Access Time (note4)		120		150		200		250	ns
t_{ACS2}	TSLQV	Chip Select Access Time (note5)		130		160		200		250	ns
t_{OH}	TAXQX	Output Hold from Adresse Change	10		10		10		10		ns
t_{LZ}	TSLQX	Chip Selection to output Active	30		30		30		30		ns
t_{HZ}	TSHQZ	Chip Deselection to output Tri-State	0	60	0	60	0	60	0	60	ns
t_{PU}	TSLICCH	Chip Selection to Power Up	0		0		0		0		ns
t_{PD}	TSLICCL	Chip Deselection to Power Down		60		60		60		60	ns

Read Cycle Waveforms*

Read Cycle 1 (Continuous Selection $\overline{CS}$ = VIL, $\overline{WE}$ = VIH)



Read Cycle 2 (Chip Select Switched, $\overline{WE}$ = VIH) (Note 5)



Note 4 : Chip Deselected for a a greater time than 55 ns prior to selection
Note 5 : Chip Deselected for a finite time less than 55 ns prior to selection.

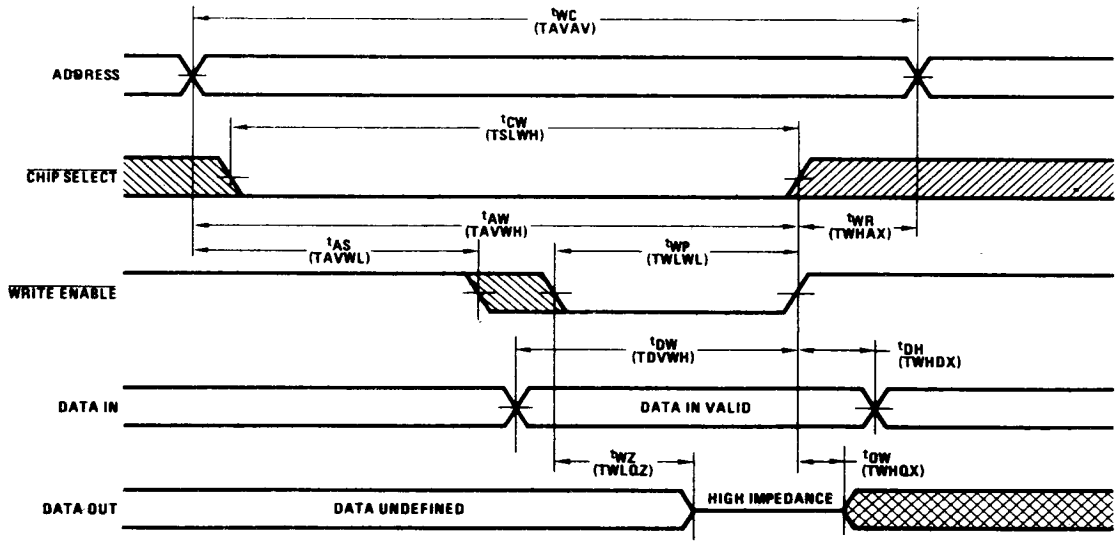
*Symbols in parentheses are industry standard.

Write Cycle AC Electrical Characteristics $T_A = 0^\circ C$ to $+70^\circ C$, $V_{CC} = 5V \pm 10\%$

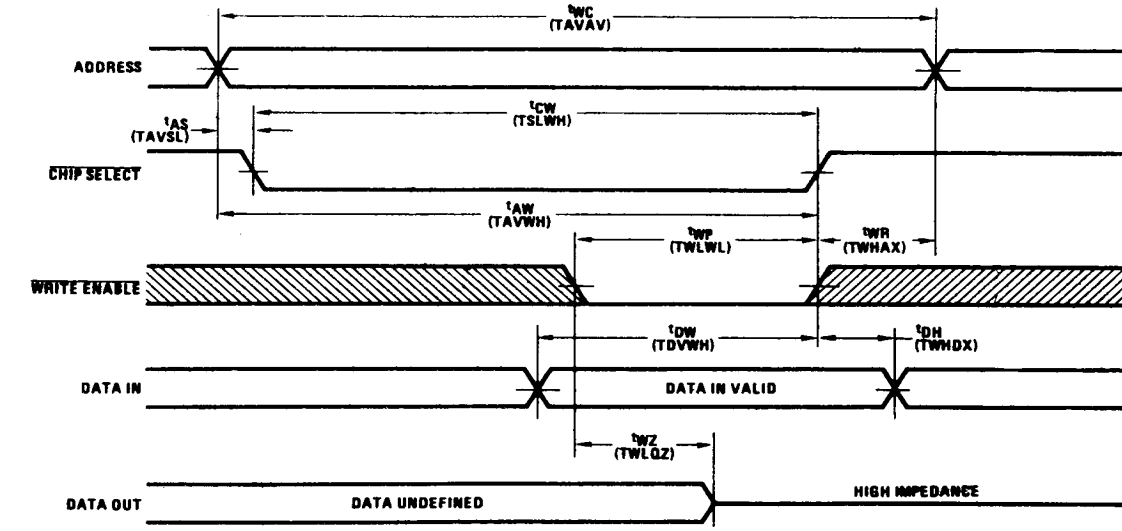
SYMBOL		PARAMETER	ET 2141-2 / ETL 2141-2		ET 2141-3 / ETL 2141-3		ET 2141-4 / ETL 2141-4		ET 2141-5 / ETL 2141-5		UNITS
ALTERNATE	STANDARD		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{WC}	TAVAV	Write Cycle Time	120		150		200		250		ns
t_{CW}	TSLWH	Chip Selection to End of Write	110		135		180		230		ns
t_{AW}	TAVWH	Address Valid to End of Write	110		135		180		230		ns
t_{AS}	TAVWL TAVSL	Address Setup Time	0		0		0		0		ns
t_{WP}	TWLWL	Write Pulse Width	60		60		60		75		ns
t_{WR}	TWHAX	Write Recovery Time	10		15		20		20		ns
t_{DW}	TDVWH	Data Valid to End of Write	50		60		60		75		ns
t_{DH}	TWHDX	Data Hold Time	5		5		5		5		ns
t_{WZ}	TWLQZ	Write Enabled to Output in Hi-Z	10	70	10	80	10	80	10	80	ns
t_{OW}	TWHQX	Output Active from End of Write	5		5		5		5		ns

Write Cycle Waveforms* (Note 5)

Write Cycle 1 (Write Enable Limited)



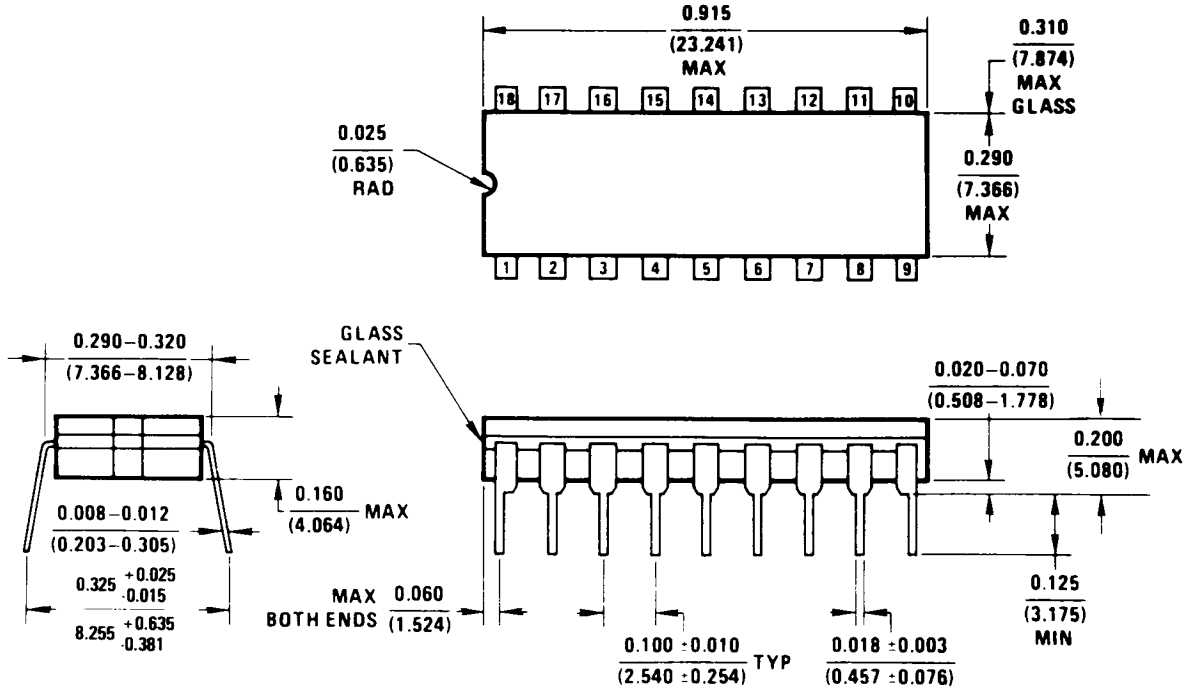
Write Cycle 2 (Chip Select Limited)



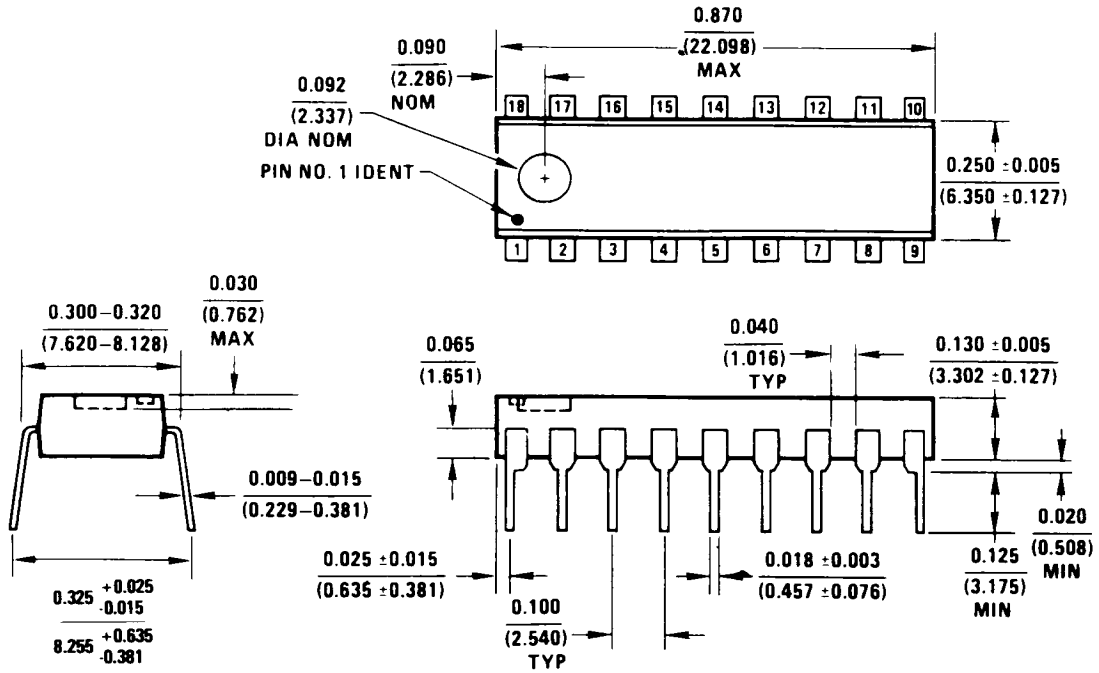
(Note 6): A write occurs during the coincidental low of $\overline{CS}$ and $\overline{WE}$. The output remains TRI-STATE if $\overline{CS}$ and $\overline{WE}$ go high simultaneously. $\overline{WE}$ or $\overline{CS}$ or both must be high during adress transitions.

*Symbols in parentheses are industry standard.

Physical Dimensions inches (millimeters)



Cavity Dual-In-Line (3)
Order Number ET2141J, (-2, -3, -4, -5)
ETL 2141 J (2, -3, -4, -5)
Package Number J18A



Moldel Dual-In-Line Package (N)
Order Number ET 2141 N (-2, -3, -4, -5)
ETL 2141 N (-2, -3, -4, -5)
Package Number N18A

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