131,072-word × 8-bit High Speed CMOS Static RAM *Preliminary*

Description

CXK581021J are 131,072-word × 8-bit high speed CMOS static RAMs suitable for use in high speed and low power applications where battery back up for nonvolatility is required.

Organized as 131,072 words by 8 bits, it operates from a single 5V supply.

Features

- Fast access time : (Access time)
  CXK581021J-47 47ns (Max.)
- Low power operation : (Operation)
  CXK581021J- 47 300mW (Typ. Cycle=Min.)
- Single +5V supply : +5V ± 10%
- Fully static memory ... No clock or timing strobe required.
- Equal access and cycle time.
- Directly TTL compatible : All inputs and outputs.
- Available in 32 pin 400-mil SOJ

32 pin SOJ (Plastic)

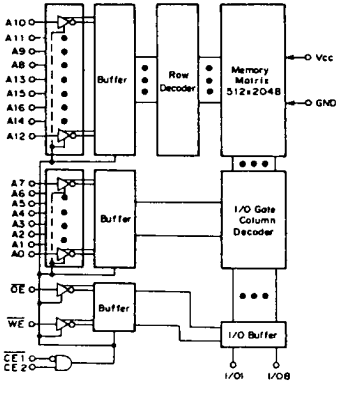
Function

131,072-word × 8-bit static RAM

Structure

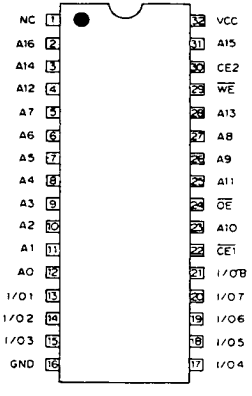
Silicon gate CMOS IC

Block Diagram



Pin Configuration

(Top View)



Pin Description

Symbol	Description
A0 to A16	Address input
I/O1 to I/O8	Data input output
$\overline{CE1}$, CE2	Chip enable 1, 2 input
$\overline{WE}$	Write enable inpuct
$\overline{OE}$	Output enable input
Vcc	+5V Power supply
GND	Ground
NC	No connection

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PE91Z23 - ST

Absolute Maximum Ratings (Ta=25℃, GND=0V)

Item	Symbol	Rating	Unit
Supply voltage	V_{CC}	−0.5 * to +7.0	V
Input voltage	V_{IN}	−0.5 * to Vcc+0.5	V
Input and output voltage	$V_{I/O}$	−0.5 * to Vcc+0.5	V
Allowable power dissipation	P_D	1.0	W
Operating temperature	Topr	0 to +70	℃
Storage temperature	Tstg	−55 to +150	℃
Soldering temperature • time	Tsolder	260•10	℃•sec

* V_{CC}, V_{IN}, $V_{I/O}$=−3.5V Min. for pulse width less than 20ns.

Truth Table

$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	Mode	I/O1 to I/O8	Vcc current
H	×	×	×	Not selected	High Z	I_{SB1}, I_{SB2}
×	L	×	×	Not selected	High Z	I_{SB1}, I_{SB2}
L	H	H	H	Output disable	High Z	I_{CC2}
L	H	L	H	Read	Data out	I_{CC2}
L	H	×	L	Write	Data in	I_{CC2}

× : "H" or "L"

DC Recommended Operating Conditions (Ta=0 to +70℃, GND=0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.2	——	Vcc+0.3	V
Input low voltage	V_{IL}	−0.3 *	——	0.8	V

* V_{IL}=−3.0V Min. for pulse width less than 20ns.

Electrical Characteristics

DC and operating characteristics

(Vcc=5V ± 10%, GND=0V, Ta=0 to +70°C)

Item	Symbol	Test conditions	Min.	Typ. *	Max.	Unit
Input leakage current	I_{LI}	V_{IN}=GND to Vcc	−2	—	2	μA
Output leakage current	I_{LO}	$V_{I/O}$=GND to Vcc, $\overline{CE1}$=V_{IH} or CE2=V_{IL} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}	−2	—	2	μA
Operating power supply current	I_{CC1}	$\overline{CE1}$=V_{IL}, CE2=V_{IH}, V_{IN}=V_{IH} or V_{IL}, I_{OUT}=0mA	—	—	—	mA
Average operating current	I_{CC2}	Cycle=Min., Duty=100%, I_{OUT}=0mA	—	—	130	mA
Standby current	I_{SB1}	$\overline{CE1}$ ≧ Vcc−0.2V or CE2 ≦ 0.2V, V_{IN} ≧ Vcc−0.2V or V_{IN} ≦ 0.2V	—	0.01	2	mA
	I_{SB2}	$\overline{CE1}$=V_{IH} or CE2=V_{IL}, Cycle=Min.	—	—	55	mA
Output high voltage	V_{OH}	I_{OH}=−4.0mA	2.4	—	—	V
Output low voltage	V_{OL}	I_{OL}=8.0mA	—	—	0.4	V

* Vcc=5V, Ta=25°C

I/O capacitance

(Ta=25°C, f=1MHz)

Item	Symbol	Test Conditions	Min.	Max.	Unit
Input capacitance	C_{IN}	V_{IN}=0V	—	7	pF
I/O capacitance	$C_{I/O}$	$V_{I/O}$=0V	—	7	pF

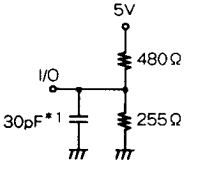
* This parameter is sampled and is not 100% tested.

AC characteristics

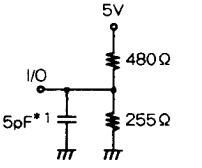
• **AC test conditions** (Vcc=5V ± 10%, Ta=0 to +70°C)

Item	Conditions
Input pulse high level	V_{IH}=3.0V
Input pulse low level	V_{IL}=0V
Input rise time	tr=5ns
Input fall time	tf=5ns
Input and output reference level	1.5V
Output load	Fig. 1

Output Load (1)



Output Load (2)*2



* 1. C_L includes scope and jig capacitances.
* 2. For t_{LZ1}, t_{LZ2}, t_{OLZ}, t_{HZ1}, t_{HZ2}, t_{OHZ}, t_{OW}, t_{WHZ}

Fig. 1

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• **Read cycle**

Item	Symbol	Min.	Max.	Unit
Read cycle time	t_{RC}	47	—	ns
Address access time	t_{AA}	—	47	ns
Chip enable access time ($\overline{CE1}$)	t_{CO1}	—	47	ns
Chip enable access time (CE2)	t_{CO2}	—	47	ns
Output enable to output valid	t_{OE}	—	25	ns
Output hold from address change	t_{OH}	5	—	ns
Chip enable to output in low Z ($\overline{CE1}$, CE2)	t_{LZ1} *, t_{LZ2} *	5	—	ns
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ} *	0	—	ns
Chip disable to output in high Z ($\overline{CE1}$, CE2)	t_{HZ1} *, t_{HZ2} *	0	20	ns
Output disable to output in high Z ($\overline{OE}$)	t_{OHZ} *	0	20	ns
Chip enable to power up time ($\overline{CE1}$, CE2)	t_{PU}	0	—	ns
Chip enable to power down time ($\overline{CE1}$, CE2)	t_{PD}	—	47	ns

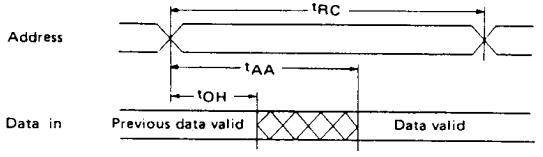
• **Write cycle**

Item	Symbol	Min.	Max.	Unit
Write cycle time	t_{WC}	47	—	ns
Address valid to end of write	t_{AW}	40	—	ns
Chip enable to end of write	t_{CW}	40	—	ns
Data to write time overlap	t_{DW}	20	—	ns
Data hold from write time	t_{DH}	0	—	ns
Write pulse width	t_{WP}	35	—	ns
Address set up time	t_{AS}	0	—	ns
Write recovery time ($\overline{WE}$, $\overline{CE1}$)	t_{WR1}	3	—	ns
Write recovery time (CE2)	t_{WR2}	5	—	ns
Output active from end of write	t_{OW} *	5	—	ns
Write to output in high Z	t_{WHZ} *	0	15	ns

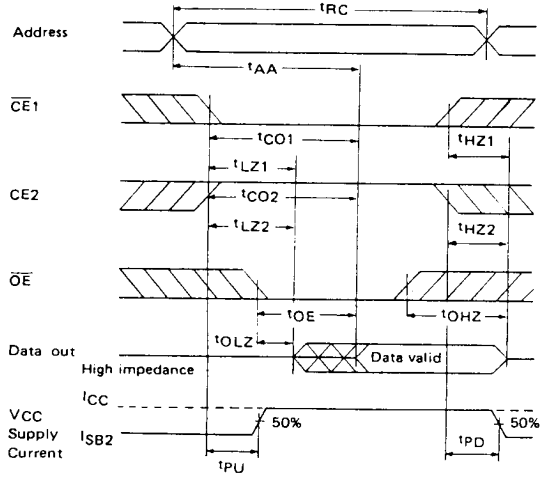
* Transition is measured ± 500mV from steady voltage with specified loading in Fig. 1 (2). This parameter is sampled and not 100% tested.

Timing Waveform

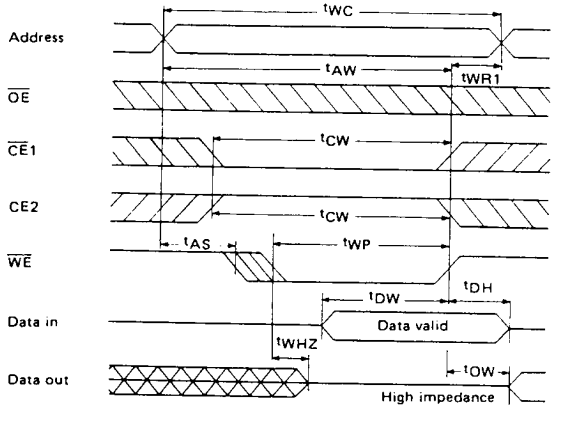
• Read cycle (1) : $\overline{CE1}$=$\overline{OE}$=V_{IL}, CE2=V_{IH}, $\overline{WE}$=V_{IH}



• Read cycle (2) : $\overline{WE}$=V_{IH}



• Write cycle (1) : $\overline{WE}$ control



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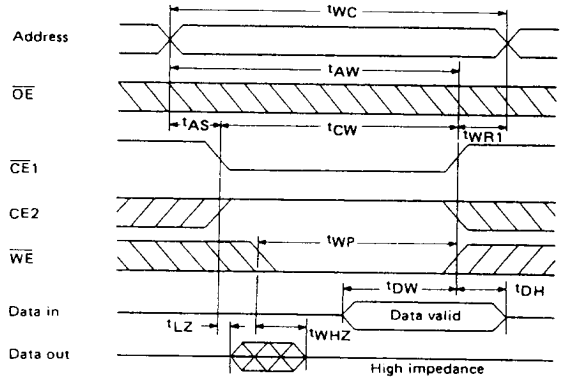
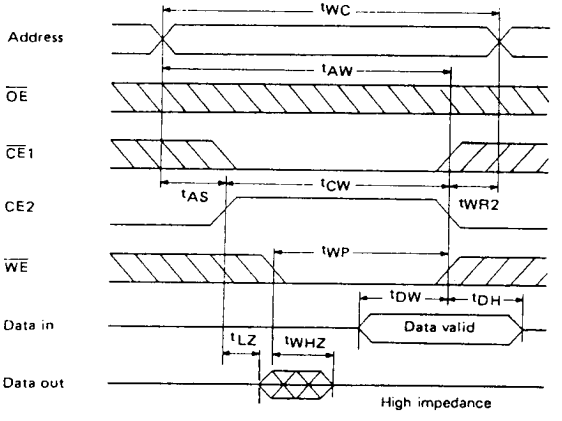
• Write cycle (2) : $\overline{CE1}$ control



• Write cycle (3) : CE2 control



* During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

Data Retention Characteristics

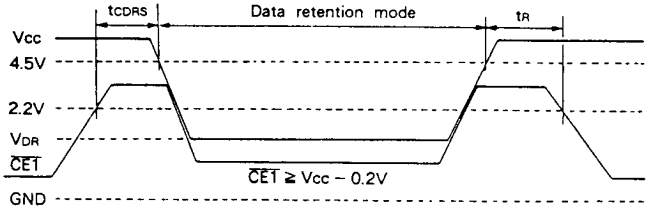
(Ta=0 to 70°C)

Item	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Data retention voltage	V_{DR}	*	2.0	—	5.5	V
Data retention current	I_{CCDR1}	Vcc=3.0V *	—	—	150	μA
	I_{CCDR2}	Vcc=2.0 to 5.5V *	—	0.01	2	mA
Data retention setup time	t_{CDRS}	Chip disable to data retention mode	0	—	—	ns
Recovery time	t_R		5	—	—	ms

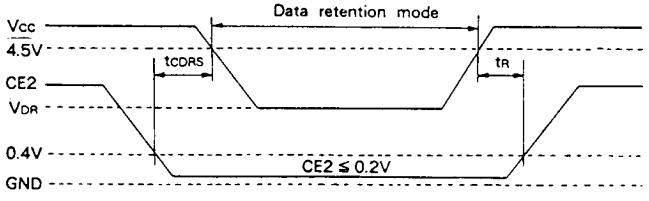
* $\overline{CE1} \geqq Vcc - 0.2V$, $CE2 \geqq Vcc - 0.2V$ ($\overline{CE1}$ control) or $CE2 \leqq 0.2V$ (CE2 control)

Data retention waveform

- Low supply voltage data retention waveform (1) ($\overline{CE1}$ control)



- Low supply voltage data retention waveform (2) (CE2 control)



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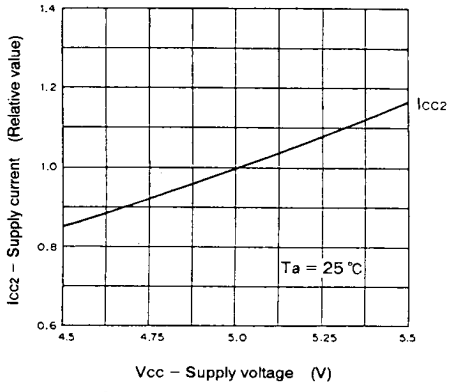
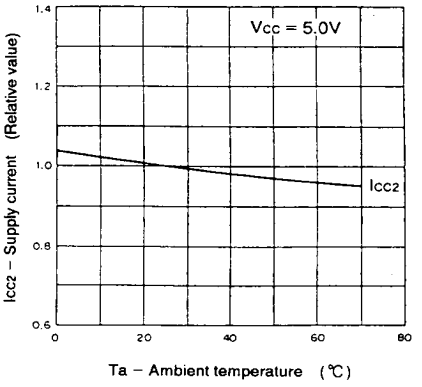
Example of Representative Characteristics

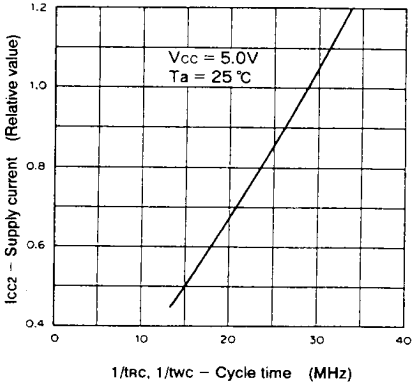
Supply current vs. Supply voltage



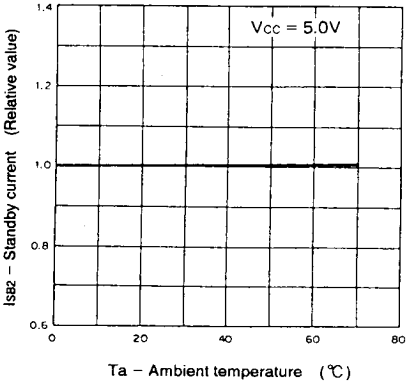
Supply current vs. Ambient temperature



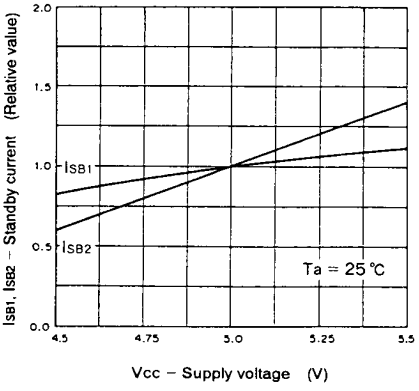
Supply current vs. Cycle time



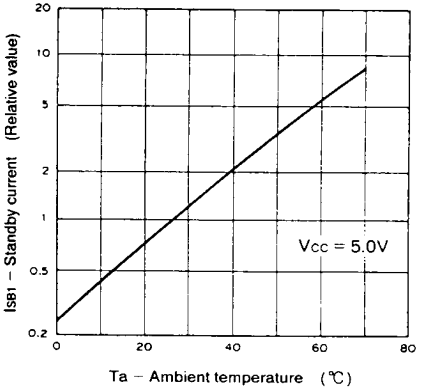
Standby current vs. Ambient temperature



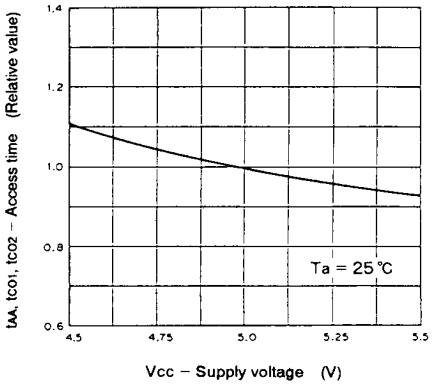
Standby current vs. Supply voltage



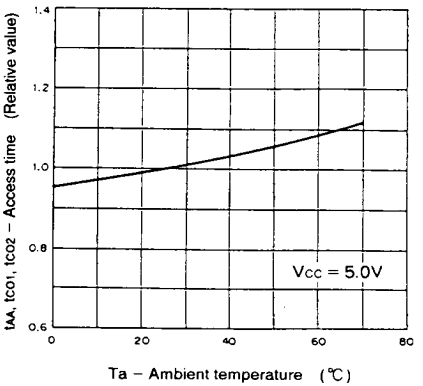
Standby current vs. Ambient temperature



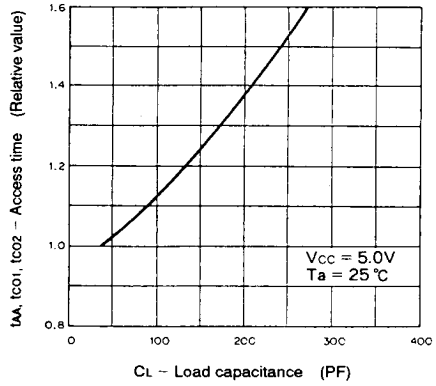
Access time vs. Supply voltage



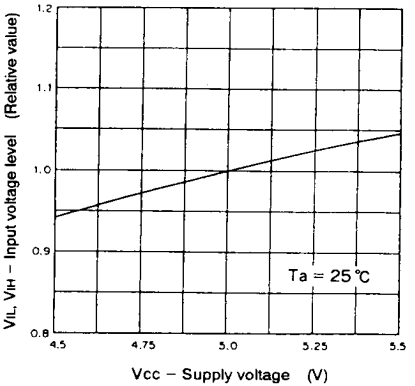
Access time vs. Ambient temperature



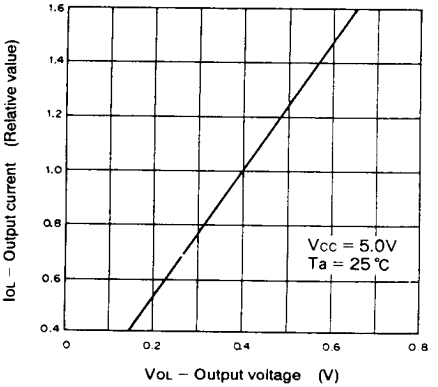
Access time vs. Load capacitance



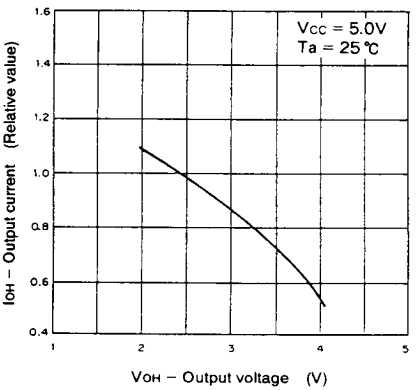
Input voltage level vs. Supply voltage



Output current vs. Output voltage



Output current vs. Output voltage



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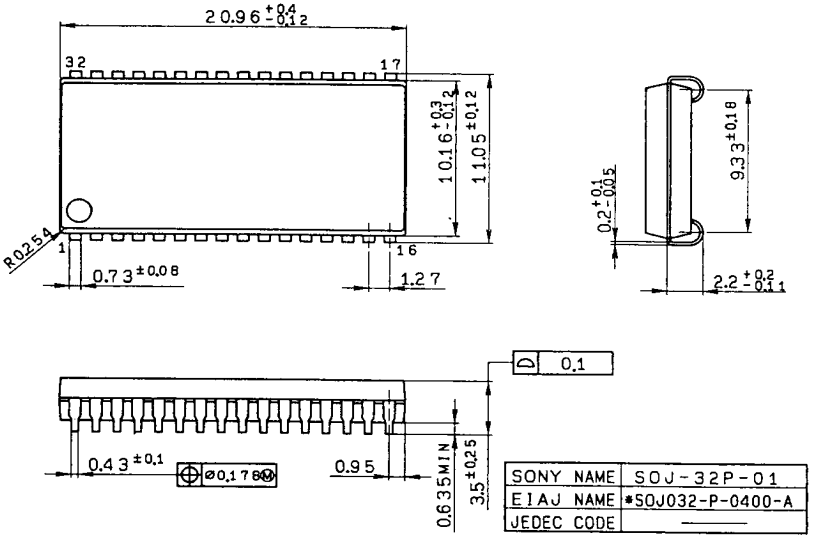
Package Outline Unit : mm

32pin SOJ (Plastic) 400mil 1.3g



SONY NAME	SOJ-32P-01
EIAJ NAME	*SOJ032-P-0400-A
JEDEC CODE	———