REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
F	Table I; Changed the max limit for I_{CC} for device types 06 through 09 from 200 mA to 210 mA. Changed the max limit for I_{CCDR} for device types 06 through 09 from 10.4 mA to 12.8 mA. - sld	98-06-23	K. A. Cottongim

REV																			
SHEET																			
REV	F	F	F	F															
SHEET	15	16	17	18															

REV STATUS OF SHEETS	REV	F	F	F	F	F	F	F	F	F	F	F	F	F
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
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DRAWING APPROVAL DATE
93-01-25

REVISION LEVEL
F

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216-5000

MICROCIRCUIT, HYBRID, MEMORY, DIGITAL, STATIC RANDOM ACCESS MEMORY, CMOS, 512K x 8-BIT

SIZE	CAGE CODE	
A	**67268**	**5962-92078**

SHEET 1 OF 18

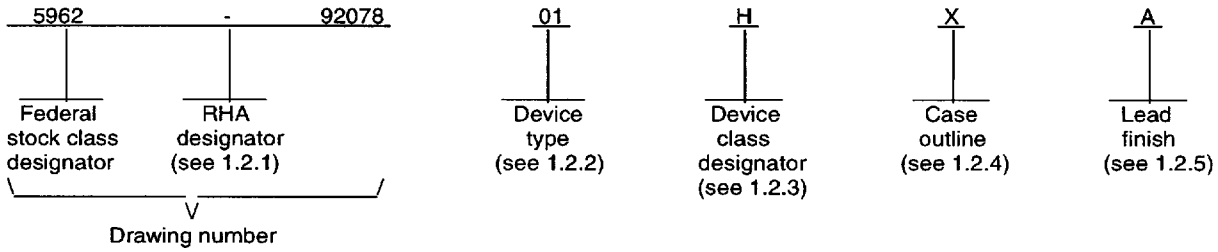
DSCC FORM 2233
APR 97

5962-E401-98

1. SCOPE

1.1 Scope. This drawing documents five product assurance classes, class D (lowest reliability), class E, (exceptions), class G (lowest high reliability), class H (high reliability), and class K, (highest reliability) and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of radiation hardness assurance levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. Device classes H and K RHA marked devices shall meet the MIL-PRF-38534 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	WS512K8-120CQ	SRAM, 512K x 8-bit	120 ns
02	WS512K8-100CQ	SRAM, 512K x 8-bit	100 ns
03	WS512K8-85CQ	SRAM, 512K x 8-bit	85 ns
04	WS512K8-70CQ	SRAM, 512K x 8-bit	70 ns
05	WS512K8-55CQ	SRAM, 512K x 8-bit	55 ns
06	WS512K8-45CQ	SRAM, 512K x 8-bit	45 ns
07	WS512K8-35CQ	SRAM, 512K x 8-bit	35 ns
08	WS512K8-25CQ	SRAM, 512K x 8-bit	25 ns
09	WS512K8-20CQ	SRAM, 512K x 8-bit	20 ns

1.2.3 Device class designator. This device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device performance documentation
D, E, G, H, or K	Certification and qualification to MIL-PRF-38534

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
T	See figure 1	32	Dual-in-line, single cavity
X	See figure 1	32	Dual-in-line, dual cavity
Y	See figure 1	32	Dual-in-line, dual cavity, gull wing leads

1.2.5 Lead finish. The lead finish shall be as specified in MIL-PRF-38534.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
Signal voltage range (any pin)	-0.5 V dc to +7.0 V dc
Power dissipation (P_D)	1 W
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Input low voltage range (V_{IL})	-0.5 V dc to +0.8 V dc
Input high voltage range (V_{IH})	+2.2 V dc to V_{CC} +0.3 V dc
Output low voltage, maximum (V_{OL})	+0.4 V dc
Output high voltage, minimum (V_{OH})	+2.4 V dc
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbook. The following specification, standards, and handbook form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38534 - Hybrid Microcircuits, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

HANDBOOK

DEPARTMENT OF DEFENSE

MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbook are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

3. REQUIREMENTS

3.1 Item requirements. The individual item performance requirements for device classes D, E, G, H, and K shall be in accordance with MIL-PRF-38534. Compliance with MIL-PRF-38534 may include the performance of all tests herein or as designated in the device manufacturer's Quality Management (QM) plan or as designated for the applicable device class. Therefore, the tests and inspections herein may not be performed for the applicable device class (see MIL-PRF-38534). Futhermore, the manufacturers may take exceptions or use alternate methods to the tests and inspections herein and not perform them. However, the performance requirements as defined in MIL-PRF-38534 shall be met for the applicable device class.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38534 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 3.

3.2.4 Timing diagram(s). The timing diagram(s) shall be as specified on figures 4 and 5.

3.2.5 Block diagram. The block diagram shall be as specified on figure 6.

3.2.6 Output load circuit. The output load circuit shall be as specified on figure 7.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full specified operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking of Device(s). Marking of device(s) shall be in accordance with MIL-PRF-38534. The device shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's vendor similar PIN may also be marked as listed in QML-38534.

3.6 Data. In addition to the general performance requirements of MIL-PRF-38534, the manufacturer of the device described herein shall maintain the electrical test data (variables format) from the initial quality conformance inspection group A lot sample, for each device type listed herein. Also, the data should include a summary of all parameters manually tested, and for those which, if any, are guaranteed. This data shall be maintained under document revision level control by the manufacturer and be made available to the preparing activity (DSCC-VA) upon request.

3.7 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to supply to this drawing. The certificate of compliance (original copy) submitted to DSCC-VA shall affirm that the manufacturer's product meets the performance requirements of MIL-PRF-38534 and herein.

3.8 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38534 shall be provided with each lot of microcircuits delivered to this drawing.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38534 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V dc $+4.5$ V dc $\le V_{CC} \le +5.5$ V dc unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
DC PARAMETERS							
Supply current	I_{CC}	$\overline{CS} = V_{IL}$, $\overline{OE} = V_{IH}$, f = 5 MHz, CMOS compatible, V_{CC} = +5.5 V dc	1, 2, 3	01, 02 03 04 05 06- 09		70 80 120 165 210	mA
Standby current	I_{SB}	$\overline{CS} = V_{CC}$, $\overline{OE} = V_{IH}$, f = 5 MHz, CMOS compatible, V_{CC} = +5.5 V dc	1, 2, 3	01, 02 03 04 05 06 07, 08 09		2.5 4.0 45 50 55 60 80	mA
Input leakage current	I_{LI}	V_{CC} = +5.5 V dc, V_{IN} = GND or V_{CC}	1, 2, 3	All		15	µA
Output leakage current	I_{LO}	$\overline{CS} = \overline{OE} = V_{IH}$, V_{OUT} = GND to V_{CC}	1, 2, 3	All		15	µA
Input low voltage	V_{IL}		1, 2, 3	All		0.8	V
Input high voltage	V_{IH}		1, 2, 3	All	2.2		V
Output low voltage	V_{OL}	Device types 01 through 05, I_{OL} = 2.1 mA Device types 06 through 09, I_{OL} = 8.0 mA	1, 2, 3	All		0.4	V
Output high voltage	V_{OH}	Device types 01 through 05, I_{OH} = -1.0 mA Device types 06 through 09, I_{OH} = -4.0 mA	1, 2, 3	All	2.4		V

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V dc $+4.5$ V dc $\le V_{CC} \le +5.5$ V dc unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
DATA RETENTION							
Data retention supply voltage	V_{DR}	$\overline{CS} \ge V_{CC} - 0.2$ V	1,2,3	All	2.0	5.5	V
Data retention current 3/	I_{CCDR}	$V_{CC} = 3.0$ V	1, 2, 3	01, 02 03 04 05 06-09		1.1 1.6 3.0 10.4 12.8	mA
FUNCTIONAL TESTING							
Functional tests		See 4.3.1c	7,8A,8B	All			
READ CYCLE AC TIMING							
Input capacitance 2/	C_{IN}	$V_{IN} = 0$ V dc, f = 1 MHz	4	01 - 05 06 - 09		40 45	pF
Output capacitance 2/	C_{OUT}	$V_{OUT} = 0$ V dc, f = 1 MHz	4	01 - 05 06 - 09		40 45	pF
Read cycle time	t_{RC}	See figure 4	9,10,11	01 02 03 04 05 06 07 08 09	120 100 85 70 55 45 35 25 20		ns
Address access time	t_{AA}	See figure 4	9,10,11	01 02 03 04 05 06 07 08 09		120 100 85 70 55 45 35 25 20	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V dc $+4.5$ V dc $\le V_{CC} \le +5.5$ V dc unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
READ CYCLE AC TIMING - Continued.							
Chip select access time	t_{ACS}	See figure 4	9,10,11	01		120	ns
				02		100	
				03		85	
				04		70	
				05		55	
				06		45	
				07		35	
				08		25	
				09		20	
Output hold from address change	t_{OH}	See figure 4	9,10,11	01-03	15		ns
				04	5		
				05 - 08	3		
Chip select to output in low impedance	t_{CLZ}	See figure 4	9,10,11	01-03	10		ns
				04, 05	5		
				06 - 09	3		
Chip select to output in high impedance	t_{CHZ}	See figure 4	9,10,11	01, 02		50	ns
				03		45	
				04		40	
				05		35	
				06		30	
				07		20	
				08		17	
				09		15	
Output enable to output valid	t_{OE}	See figure 4	9,10,11	01, 02		60	ns
				03		55	
				04		50	
				05		40	
				06		35	
				07		25	
				08, 09		10	
Output enable to output in low impedance	t_{OLZ}	See figure 4	9,10,11	01 - 04	5.0		ns
				05 - 09	0		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$, $V_{SS} = 0$ V dc, $+4.5$ V dc $\le V_{CC} \le +5.5$ V dc unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
READ CYCLE AC TIMING - Continued.							
Output enable to output in high impedance	t_{OHZ}	See figure 4	9,10,11	01, 02		50	ns
				03		45	
				04		40	
				05		30	
				06		25	
				07		20	
				08		15	
				09		12	
WRITE CYCLE AC TIMING							
Address setup time	t_{AS}	See figure 5	9,10,11	All	2		ns
Write cycle time	t_{WC}	See figure 5	9,10,11	01	120		ns
				02	100		
				03	85		
				04	70		
				05	55		
				06	45		
				07	35		
				08	25		
				09	20		
Write pulse width	t_{WP}	See figure 5	9,10,11	01	80		ns
				02	70		
				03	65		
				04, 05	40		
				06	30		
				07	25		
				08	20		
				09	16		
Write recovery time	t_{WR}	See figure 5	9,10,11	All	2		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

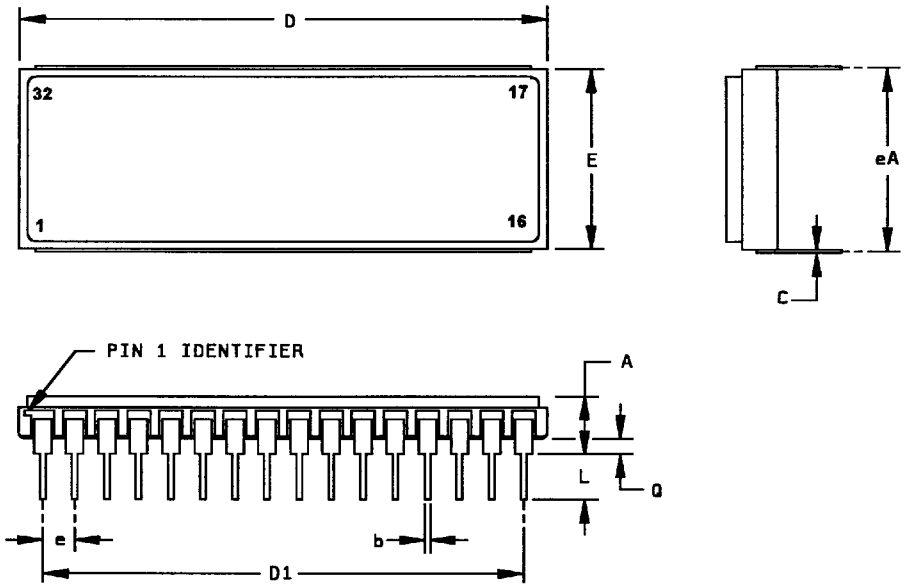
Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V dc $+4.5$ V dc $\le V_{CC} \le +5.5$ V dc unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
WRITE CYCLE AC TIMING - Continued.							
Data valid to end of write	t_{DW}	See figure 5	9,10,11	01, 02	50		ns
				03	45		
				04	40		
				05	30		
				06	25		
				07	20		
				08, 09	15		
Data hold time	t_{DH}	See figure 5	9,10,11	01 - 04	0		ns
				05 - 09	1		
Address valid to end of write	t_{AW}	See figure 5	9,10,11	01	85		ns
				02, 03	75		
				04, 05	50		
				06	30		
				07	25		
				08	20		
				09	16		

1/ Unless otherwise specified; the AC test conditions are as follows:
Input pulse levels: $V_{IL} = 0$ V and $V_{IH} = 3.0$ V.
Input rise and fall times: 5 nanoseconds
Input and output timing reference levels: 1.5 V.
Output loading: See figure 7.
Unless otherwise specified; the DC test conditions are as follows:
$V_{IH} = V_{CC} - 0.3$ V.
$V_{IL} = 0.3$ V.

2/ Parameters shall be tested as part of device characterization and after design and process changes. Parameters shall be guaranteed to the limits specified in table I for all lots not specifically tested.

3/ For device types 01 and 02, the maximum limit for data retention current is 200 µA at +70°C.

Case outline T.

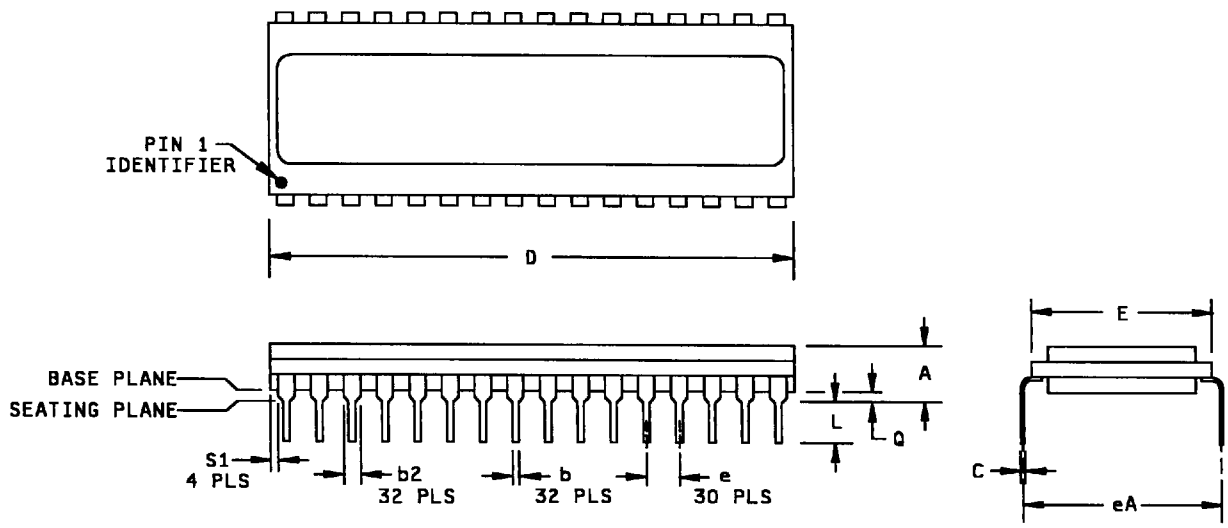


Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	3.56	5.13	0.140	0.202
b	0.41	0.51	0.016	0.020
c	0.20	0.30	0.009	0.012
D	42.01	42.82	1.654	1.686
D1	37.90	38.30	1.492	1.508
E	14.73	15.34	0.580	0.604
e	2.50 BSC		0.100 BSC	
eA	14.99	15.49	0.590	0.610
L	3.18	4.90	0.125	0.193
Q	0.48	1.19	0.019	0.047

NOTES:
1. The U.S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Pin numbers are for reference only.

FIGURE 1. Case outline(s).

Case outline X.

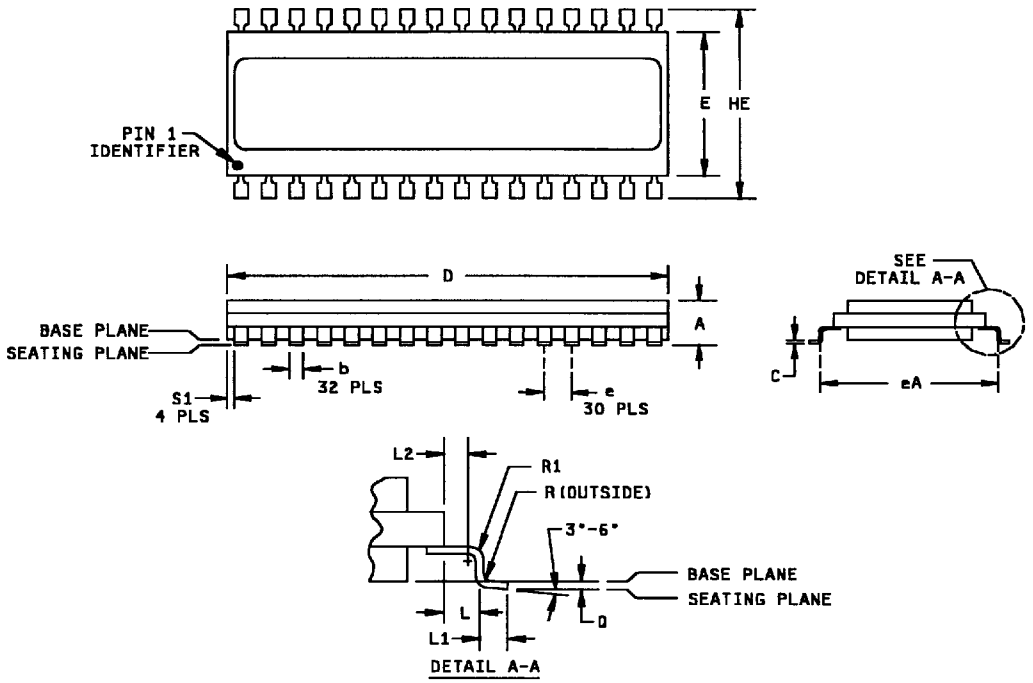


Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	3.68	5.08	0.145	0.200
b	0.41	0.51	0.016	0.020
b2	1.14	1.40	0.045	0.055
C	0.23	0.30	0.009	0.012
D	40.23	41.05	1.584	1.616
E	13.77	14.17	0.542	0.558
e	2.54 BSC		0.100 BSC	
eA	14.99	15.49	0.590	0.610
L	3.18		0.125	
Q	0.64	1.52	0.025	0.060
S1	0.13		0.005	

NOTES:
1. The U.S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.

FIGURE 1. Case outline(s) - Continued.

Case outline Y.



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	3.35	4.29	0.132	0.169
b	1.14	1.40	0.045	0.055
C	0.23	0.30	0.009	0.012
D	40.23	41.05	1.584	1.616
E	13.81	14.12	0.544	0.556
HE	17.91	18.42	0.705	0.725
e	2.54 BSC		0.100 BSC	
eA	15.67	16.59	0.617	0.653
L	1.079 TYP		0.0425 TYP	
L1	1.02	1.27	0.040	0.050
L2	0.698 TYP		0.0275 TYP	
Q	0.08	0.28	0.003	0.011
R	1.02 TYP		0.040 TYP	
R1	0.508 TYP		0.020 TYP	
S1	0.13		0.005	

NOTES:
1. The U.S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.

FIGURE 1. Case outline(s) - Continued.

Device types	01 - 09
Case outlines	All
Terminal number	Terminal connection
1	A18
2	A16
3	A14
4	A12
5	A7
6	A6
7	A5
8	A4
9	A3
10	A2
11	A1
12	A0
13	I/O 0
14	I/O 1
15	I/O 2
16	V_{SS}
17	I/O 3
18	I/O 4
19	I/O 5
20	I/O 6
21	I/O 7
22	CS
23	A10
24	OE
25	A11
26	A9
27	A8
28	A13
29	WE
30	A17
31	A15
32	V_{CC}

FIGURE 2. Terminal connections.

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	A0-A18	Mode	Data I/O	Device
H	X	X	X	Standby	High Z	Standby
L	L	H	Stable	Read	Data out	Active
L	X	L	Stable	Write	Data In	Active
L	H	H	Stable	Out disable	High Z	Active

NOTES:
1. H = V_{IH} = High logic level
2. L = V_{IL} = Low logic level
3. X = Do not care (either high or low)
4. High Z = High impedance state

FIGURE 3. Truth table.

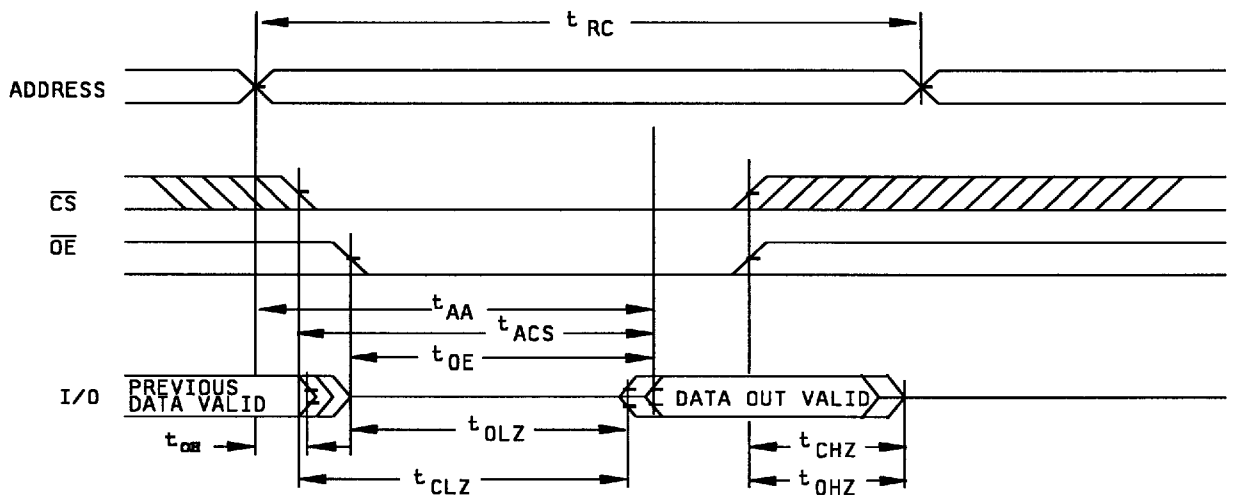


FIGURE 4. Read cycle timing diagram.

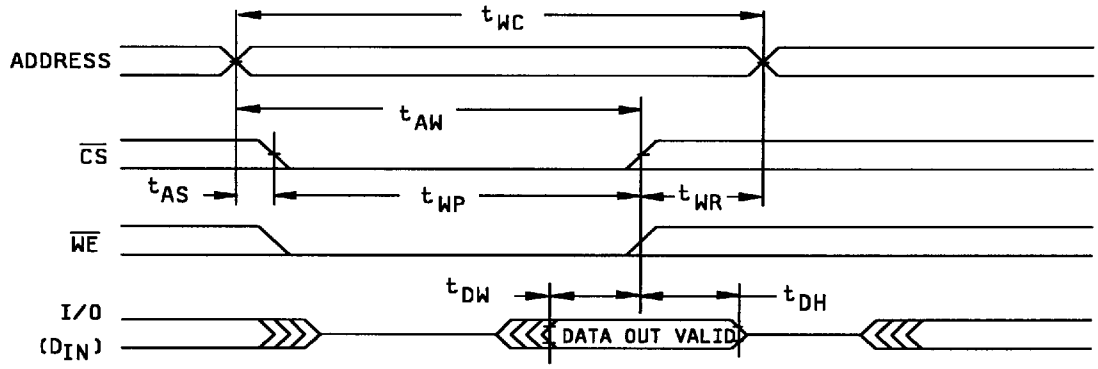


FIGURE 5. Write cycle timing diagram.

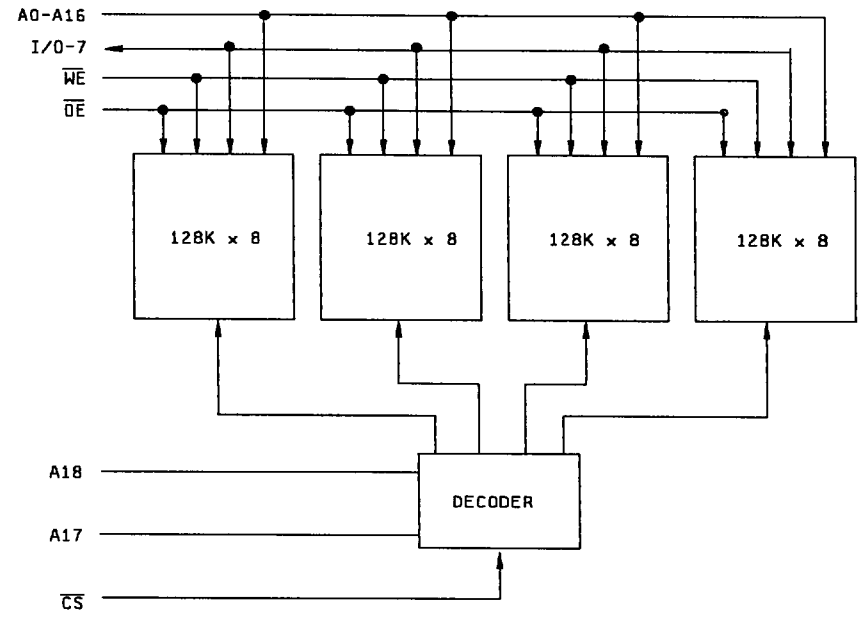
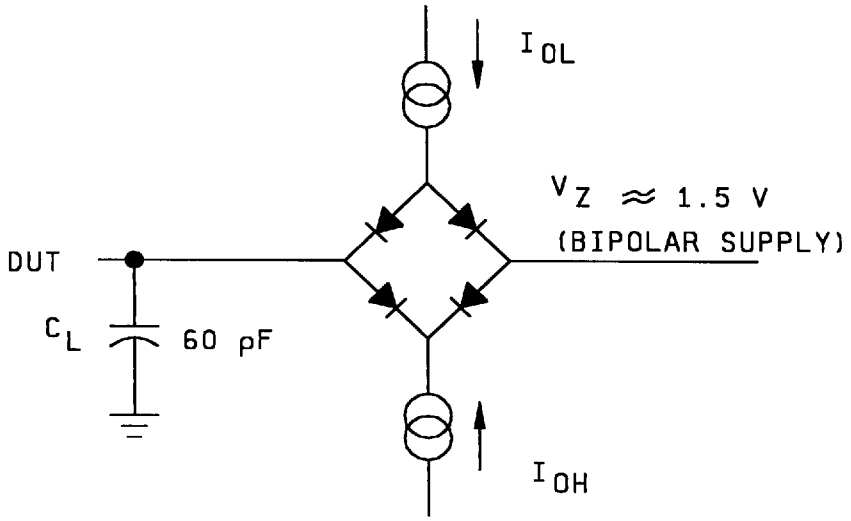


FIGURE 6. Block diagram.



NOTES:
1. V_Z is programmable from -2 V to + 7 V. I_{OH} and I_{OL} are programmable from 0 to 16 mA.
2. Tester impedance, Z_O = 75 ohms.
3. V_Z is typically the midpoint of V_{OH} and V_{OL}, approximately 1.5 V.
4. C_L includes tester jig capacitance.

FIGURE 7. Output load circuit.

TABLE II. Electrical test requirements.

MIL-PRF-38534 test requirements	Subgroups (in accordance with MIL-PRF-38534, group A test table)
Interim electrical parameters	1,4,7,9
Final electrical parameters	1*,2,3,4,7*,8A,8B,9,10, 11
Group A test requirements	1,2,3,4,7,8A,8B,9,10,11
Group C end-point electrical parameters	1,2,3,4,7,8A,8B,9,10,11
MIL-STD-883, group E end-point electrical parameters for RHA devices	Subgroups** (in accordance with method 5005, group A test table)

* PDA applies to subgroups 1 and 7.
** When applicable to this standard microcircuit drawing, the subgroups shall be defined.

4.2 Screening. Screening shall be in accordance with MIL-PRF-38534. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition B. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A as specified in accordance with table I of method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Conformance and periodic inspections. Conformance inspection (CI) and periodic inspection (PI) shall be in accordance with MIL-PRF-38534 and as specified herein.

4.3.1 Group A inspection (CI). Group A inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 shall be omitted.

c. Subgroups 7, 8A, and 8B shall include verification of the truth table on figure 3.

4.3.2 Group B inspection (PI). Group B inspection shall be in accordance with MIL-PRF-38534.

4.3.3 Group C inspection (PI). Group C inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test, method 1005 of MIL-STD-883.

(1) Test condition B. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A as specified in accordance with table I of method 1005 of MIL-STD-883.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.3.4 Group D inspection (PI). Group D inspection shall be in accordance with MIL-PRF-38534.

4.3.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels shall be M, D, R, and H. RHA quality conformance inspection sample tests shall be performed at the RHA level specified in the acquisition document.

a. RHA tests for levels M, D, R, and H shall be performed through each level to determine at what levels the devices meet the RHA requirements. These RHA tests shall be performed for initial qualification and after design or process changes which may affect the RHA performance of the device.

b. End-point electrical parameters shall be as specified in table II herein.

c. Prior to total dose irradiation, each selected sample shall be assembled in its qualified package. It shall pass the specified group A electrical parameters in table I for subgroups specified in table II herein.

d. The devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38534 for RHA level being tested, and meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5 percent, after exposure.

e. Prior to and during total dose irradiation testing, the devices shall be biased to establish a worst case condition as specified in the radiation exposure circuit.

f. For device classes H and K, subgroups 1 and 2 in table V, method 5005 of MIL-STD-883 shall be tested as appropriate for device construction.

g. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38534.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0526.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0512.

6.6 Sources of supply. Sources of supply are listed in QML-38534. The vendors listed in QML-38534 have submitted a certificate of compliance (see 3.7 herein) to DSCC-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 98-06-23

Approved sources of supply for SMD 5962-92078 are listed below for immediate acquisition only and shall be added to QML-38534 during the next revision. QML-38534 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of QML-38534.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9207801HTX	54230	WS512K8-120CQ
5962-9207801HXX	54230	WS512K8-120CQ
5962-9207801HYX	54230	WS512K8-120CLQ
5962-9207802HTX	54230	WS512K8-100CQ
5962-9207802HXX	54230	WS512K8-100CQ
5962-9207802HYX	54230	WS512K8-100CLQ
5962-9207803HTX	54230	WS512K8-85CQ
5962-9207803HXX	54230	WS512K8-85CQ
5962-9207803HYX	54230	WS512K8-85CLQ
5962-9207804HTX	54230	WS512K8-70CQ
5962-9207804HXX	54230	WS512K8-70CQ
5962-9207804HYX	54230	WS512K8-70CLQ
5962-9207805HTX	54230	WS512K8-55CQ
5962-9207805HXX	54230	WS512K8-55CQ
5962-9207805HYX	54230	WS512K8-55CLQ
5962-9207806HTX	54230	WS512K8-45CQ
5962-9207806HXX	54230	WS512K8-45CQ
5962-9207806HYX	54230	WS512K8-45CLQ
5962-9207807HTX	54230	WS512K8-35CQ
5962-9207807HXX	54230	WS512K8-35CQ
5962-9207807HYX	54230	WS512K8-35CLQ

1/ The lead finish shown for each PIN representing a hermetic package is available in lead finishes A or C from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availibility.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9207808HTX 5962-9207808HXX 5962-9207808HYX	54230 54230 54230	WS512K8-25CQ WS512K8-25CQ WS512K8-25CLQ
5962-9207809HTX 5962-9207809HXX 5962-9207809HYX	54230 54230 54230	WS512K8-20CQ WS512K8-20CQ WS512K8-20CLQ

1/ The lead finish shown for each PIN representing a hermetic package is available in lead finishes A or C from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availibility.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
54230	White Microelectronics 3601 East University Drive Phoenix, AZ 85034

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in this information bulletin.