TLE42744

Low Dropout Linear Voltage Regulator

Automotive Power

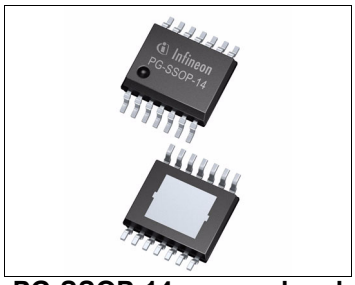
Never stop thinking

1 Overview

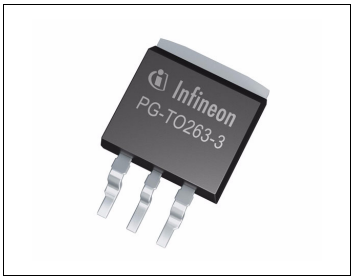
Features

- Very Low Current Consumption
- Output Voltages 5 V and 3.3 V ±2%
- Output Current up to 400 mA
- Very Low Dropout Voltage
- Output Current Limitation
- Reverse Polarity Protection
- Overtemperature Shutdown
- Wide Temperature Range
  From -40 °C up to 150 °C
- Green Product (RoHS compliant)
- AEC Qualified

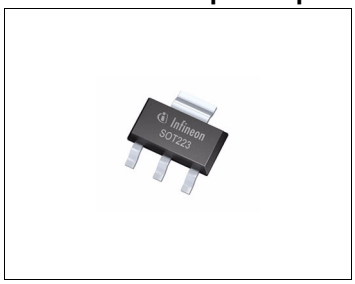
PG-TO252-3



PG-SSOP-14 exposed pad



PG-TO263-3



PG-SOT223-4

Description

The TLE42744 is a monolithic integrated low dropout voltage regulator for load currents up to 400 mA. An input voltage up to 40 V is regulated to $V_{Q,nom}$ = 5 V / 3.3 V with a precision of ±2%. The device is designed for the harsh environment of automotive applications. Therefore it is protected against overload, short circuit and overtemperature conditions by the implemented output current limitation and the overtemperature shutdown circuit. The TLE42744 can be also used in all other applications requiring a stabilized 5 V / 3.3 V voltage.

Due to its very low quiescent current the TLE42744 is dedicated for use in applications permanently connected to V_{BAT}.

Type	Package	Marking
TLE42744DV50	PG-TO252-3	42744V5
TLE42744GV50	PG-TO263-3	42744V5
TLE42744EV50	PG-SSOP-14 exposed pad	42744V5
TLE42744DV33	PG-TO252-3	42744V33
TLE42744GV33	PG-TO263-3	42744V33
TLE42744GSV33	PG-SOT223-4	42744V33

2 Block Diagram

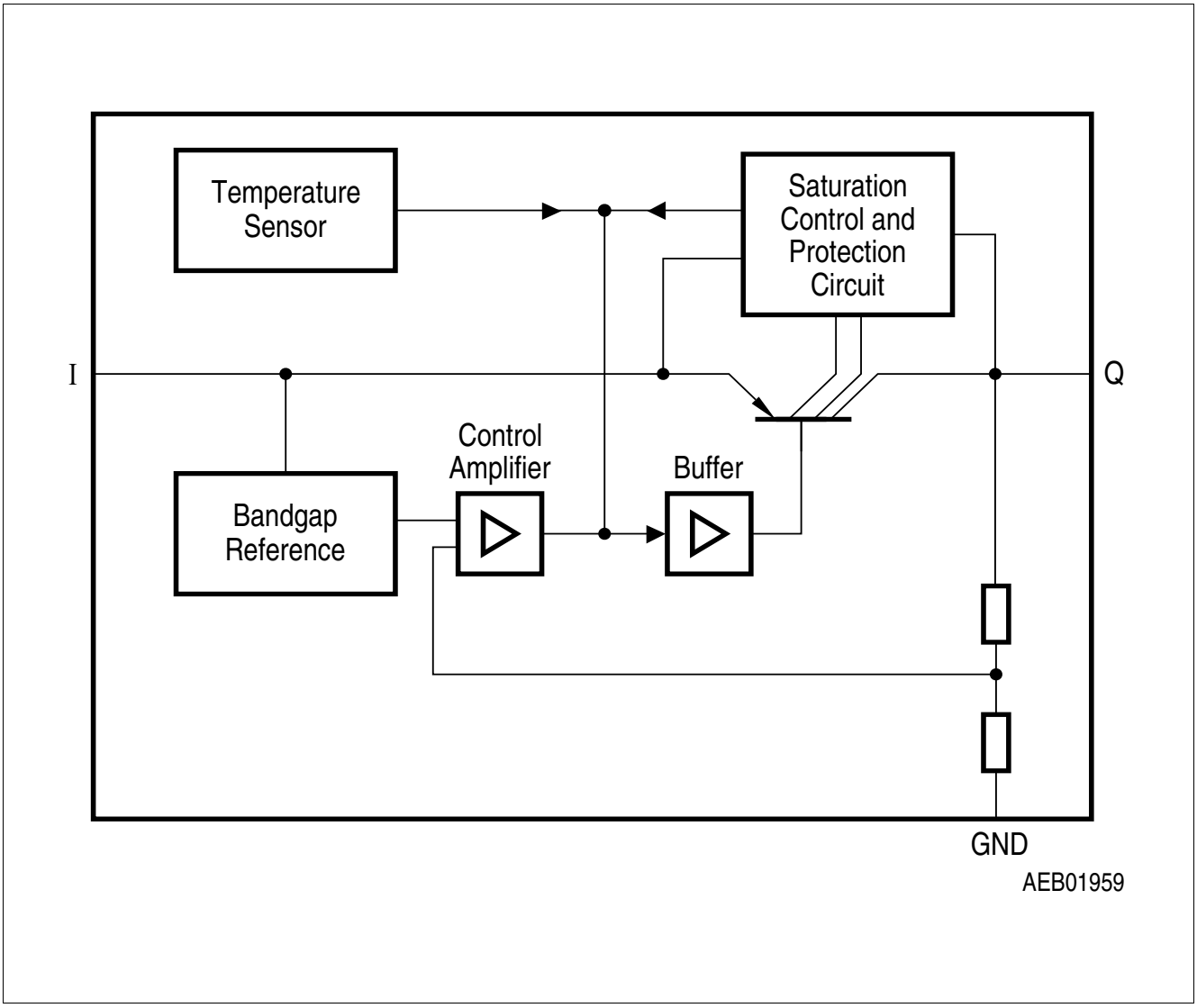


Figure 1 Block Diagram

3 Pin Configuration

3.1 Pin Assignment PG-TO252-3, PG-TO263-3 and PG-SOT223-4

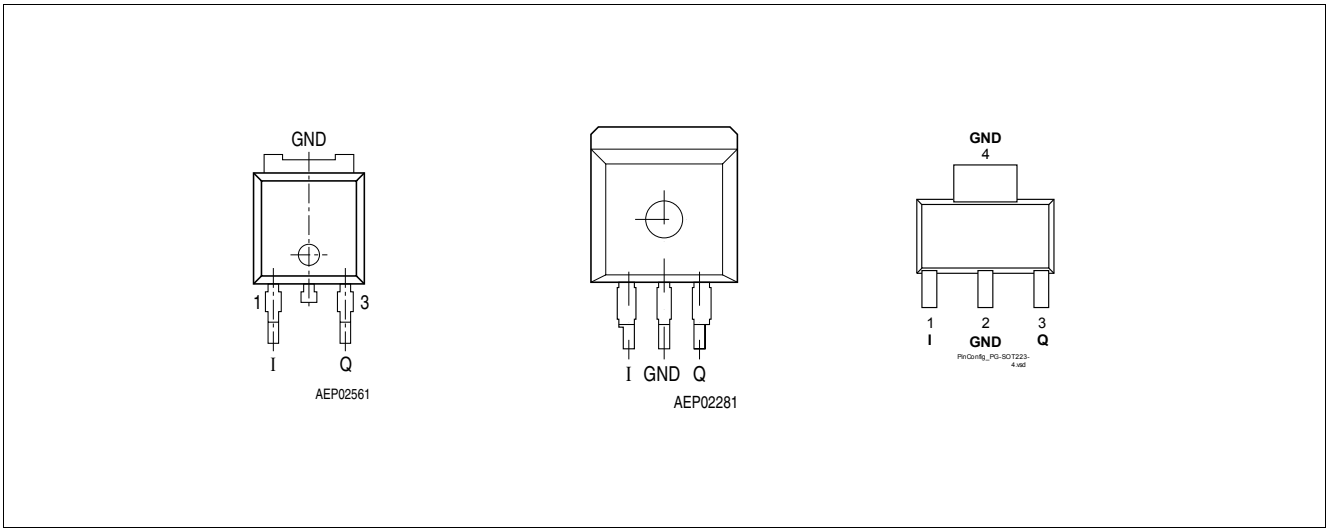


Figure 2 Pin Configuration (top view)

3.2 Pin Definitions and Functions PG-TO252-3, PG-TO263-3and PG-SOT223-4

Pin No.	Symbol	Function
1	I	**Input** block to ground directly at the IC with a ceramic capacitor
2	GND	**Ground** internally connected to heat slug
3	Q	**Output** block to ground with a capacitor close to the IC terminals, respecting the values given for its capacitance and ESR in **“Functional Range” on Page 7**
Heat Slug / 4	–	**Heat Slug** internally connected to GND; connect to GND and heatsink area

3.3 Pin Assignment PG-SSOP-14 exposed pad

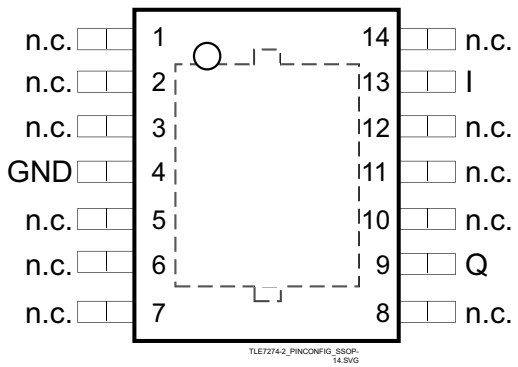


Figure 3 Pin Configuration (top view)

3.4 Pin Definitions and Functions PG-SSOP-14 exposed pad

Pin No.	Symbol	Function
1, 2, 3, 5, 6, 7	n.c.	**not connected** can be open or connected to GND
4	GND	**Ground**
8, 10, 11, 12, 14	n.c.	**not connected** can be open or connected to GND
9	Q	**Output** block to ground with a capacitor close to the IC terminals, respecting the values given for its capacitance and ESR in **“Functional Range” on Page 7**
13	I	**Input** block to ground directly at the IC with a ceramic capacitor
Pad	–	**Exposed Pad** connect to GND and heatsink area

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Absolute Maximum Ratings[1)]
T_j = -40 °C to 150 °C; all voltages with respect to ground, (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Test Condition
			Min.	Max.		
Input I						
4.1.1	Voltage	V_I	-42	45	V	–
Output Q						
4.1.2	Voltage	V_Q	-1	40	V	–
Temperature						
4.1.3	Junction temperature	T_j	-40	150	°C	–
4.1.4	Storage temperature	T_{stg}	-50	150	°C	–
ESD Susceptibility						
4.1.5	ESD Absorption	$V_{ESD,HBM}$	-4	4	kV	Human Body Model (HBM)[2)]
4.1.6		$V_{ESD,CDM}$	-1000	1000	V	Charge Device Model (CDM)[3)] at all pins

1) not subject to production test, specified by design
2) ESD susceptibility Human Body Model “HBM” according to AEC-Q100-002 - JESD22-A114
3) ESD susceptibility Charged Device Model “CDM” according to ESDA STM5.3.1

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

4.2 Functional Range

Pos.	Parameter	Symbol	Limit Values		Unit	Remarks
			Min.	Max.		
4.2.1	Input voltage	V_I	5.5	40	V	TLE42744DV50, TLE42744GV50, TLE42744EV50
4.2.2	Input voltage	V_I	4.7	40	V	TLE42744GV33, TLE42744DV33, TLE42744GSV33
4.2.3	Output Capacitor's Requirements for Stability	C_Q	22	–	µF	1)
4.2.4		$ESR(C_Q)$	–	3	Ω	2)
4.2.5	Junction temperature	T_j	-40	150	°C	–

1) the minimum output capacitance requirement is applicable for a worst case capacitance tolerance of 30%

2) relevant ESR value at f = 10 kHz

Note: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.

4.3 Thermal Resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
TLE42744DV50, TLE42744DV33 (PG-TO252-3)							
4.3.1	Junction to Case[1)]	R_{thJC}	–	3.6	–	K/W	measured to heat slug
4.3.2	Junction to Ambient[1)]	R_{thJA}	–	27	–	K/W	2)
4.3.3			–	115	–	K/W	footprint only[3)]
4.3.4			–	52	–	K/W	300 mm² heatsink area[3)]
4.3.5			–	40	–	K/W	600 mm² heatsink area[3)]
TLE42744GV50, TLE42744GV33 (PG-TO263-3)							
4.3.6	Junction to Case[1)]	R_{thJC}	–	3.6	–	K/W	measured to heat slug
4.3.7	Junction to Ambient[1)]	R_{thJA}	–	22	–		2)
4.3.8			–	74	–	K/W	footprint only[3)]
4.3.9			–	42	–	K/W	300 mm² heatsink area[3)]
4.3.10			–	34	–	K/W	600 mm² heatsink area[3)]

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
TLE42744EV50 (PG-SSOP-14 exposed pad)							
4.3.11	Junction to Case[1)]	R_{thJC}	–	7	–	K/W	measured to exposed pad
4.3.12	Junction to Ambient[1)]	R_{thJA}	–	43	–	K/W	[2)]
4.3.13			–	120	–	K/W	footprint only[3)]
4.3.14			–	59	–	K/W	300 mm² heatsink area[3)]
4.3.15			–	49	–	K/W	600 mm² heatsink area[3)]
TLE42744GSV33 (PG-SOT223-4)							
4.3.16	Junction to Case[1)]	R_{thJC}	–	17	–	K/W	measured to heat slug
4.3.17	Junction to Ambient[1)]	R_{thJA}	–	54	–	K/W	[2)]
4.3.18			–	139	–	K/W	footprint only[3)]
4.3.19			–	73	–	K/W	300 mm² heatsink area[3)]
4.3.20			–	64	–	K/W	600 mm² heatsink area[3)]

1) Not subject to production test, specified by design.

2) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm³ board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

3) Specified R_{thJA} value is according to Jedec JESD 51-3 at natural convection on FR4 1s0p board; The Product (Chip+Package) was simulated on a 76.2 $\times$ 114.3 $\times$ 1.5 mm^3 board with 1 copper layer (1 x 70µm Cu).

5 Electrical Characteristics

5.1 Electrical Characteristics Voltage Regulator

Electrical Characteristics
V_I=13.5 V; T_j = -40 °C to 150 °C; all voltages with respect to ground (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Measuring Condition
			Min.	Typ.	Max.		
Output Q							
5.1.1	Output Voltage	V_Q	4.9	5.0	5.1	V	TLE42744DV50, TLE42744GV50, TLE42744EV50 5 mA < I_Q< 400 mA 6 V < V_I < 28 V
5.1.2	Output Voltage	V_Q	4.9	5.0	5.1	V	TLE42744DV50, TLE42744GV50, TLE42744EV50 5 mA < I_Q<200 mA 6 V < V_I < 40 V
5.1.3	Output Voltage	V_Q	3.23	3.3	3.37	V	TLE42744GV33, TLE42744DV33, TLE42744GSV33; 5 mA < I_Q< 400 mA 4.7 V < V_I < 28 V
5.1.4	Output Voltage	V_Q	3.23	3.3	3.37	V	TLE42744GV33, TLE42744DV33, TLE42744GSV33; 5 mA < I_Q<200 mA 4.7 V < V_I < 40 V
5.1.5	Dropout Voltage	V_{dr}	–	250	500	mV	TLE42744DV50, TLE42744GV50, TLE42744EV50 I_Q = 250 mA V_{dr} = V_I – V_Q [1)]
5.1.6	Load Regulation	$\Delta V_{Q, lo}$	–	20	50	mV	TLE42744DV50, TLE42744GV50, TLE42744EV50; I_Q = 5 mA to 400 mA V_I = 6 V
5.1.7	Load Regulation	$\Delta V_{Q, lo}$	–	40	70	mV	TLE42744GV33, TLE42744DV33, TLE42744GSV33; I_Q = 5 mA to 300 mA
5.1.8	Line Regulation	$\Delta V_{Q, li}$	–	10	25	mV	V_I = 12 V to 32 V I_Q = 5 mA
5.1.9	Output Current Limitation	I_Q	400	600	1100	mA	[1)]
5.1.10	Power Supply Ripple Rejection[2)]	$PSRR$	–	60	–	dB	f_r = 100 Hz; V_r = 0.5 Vpp

Electrical Characteristics

V_I=13.5 V; T_j = -40 °C to 150 °C; all voltages with respect to ground (unless otherwise specified)

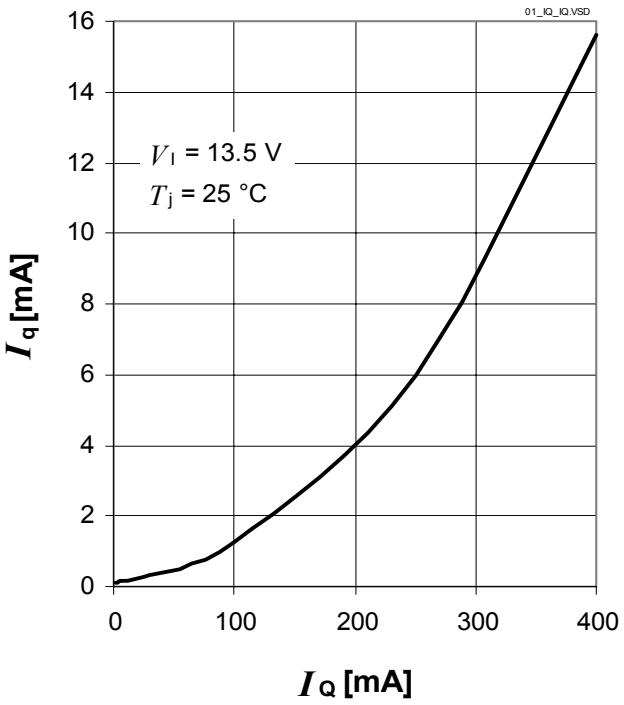
Pos.	Parameter	Symbol	Limit Values			Unit	Measuring Condition
			Min.	Typ.	Max.		
5.1.11	Temperature Output Voltage Drift[2]	$\frac{dV_Q}{dT}$	–	0.5	–	mV/K	–
5.1.12	Overtemperature Shutdown Threshold	$T_{j,sd}$	151	–	200	°C	T_j increasing[2]
5.1.13	Overtemperature Shutdown Threshold Hysteresis	$T_{j,sdh}$	–	25	–	°C	T_j decreasing[2]
Current Consumption							
5.1.14	Quiescent Current $I_q = I_I - I_Q$	I_q	–	100	220	µA	I_Q = 1 mA
5.1.15	Current Consumption $I_q = I_I - I_Q$	I_q	–	8	15	mA	I_Q = 250 mA
5.1.16		I_q	–	15	25	mA	TLE42744DV50, TLE42744GV50, TLE42744EV50; I_Q = 400 mA
5.1.17			–	20	30	mA	TLE42744GV33, TLE42744DV33, TLE42744GSV33; I_Q = 400 mA

1) Measured when the output voltage V_Q has dropped 100 mV from the nominal value obtained at V_I = 13.5 V.

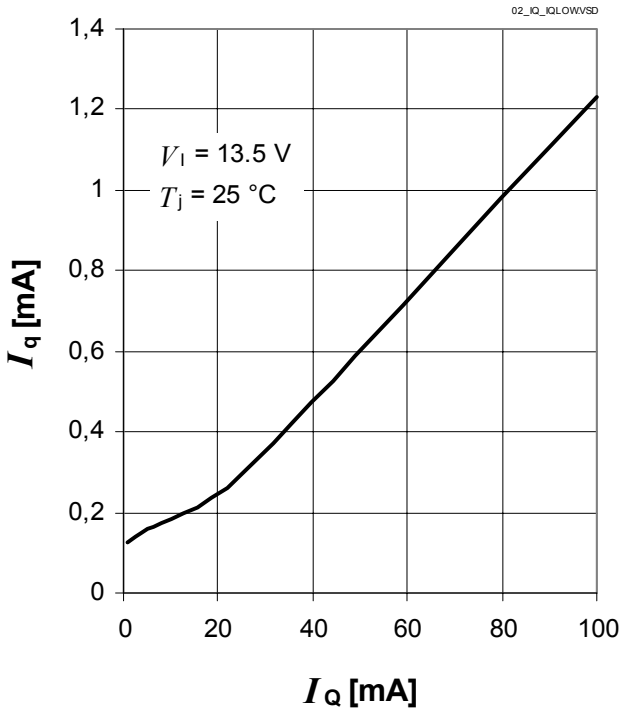
2) not subject to production test, specified by design

5.2 Typical Performance Characteristics Voltage Regulator

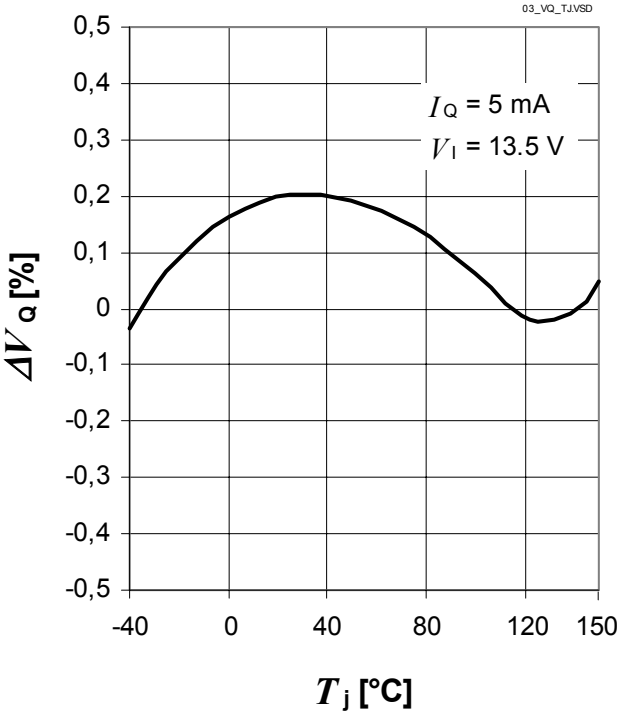
Current Consumption I_q versus Output Current I_Q



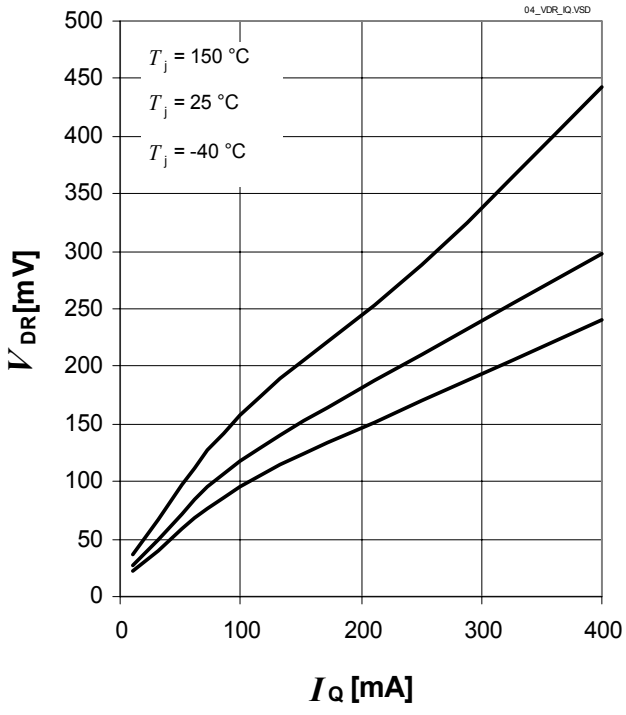
Current Consumption I_q versus Low Output Current I_Q



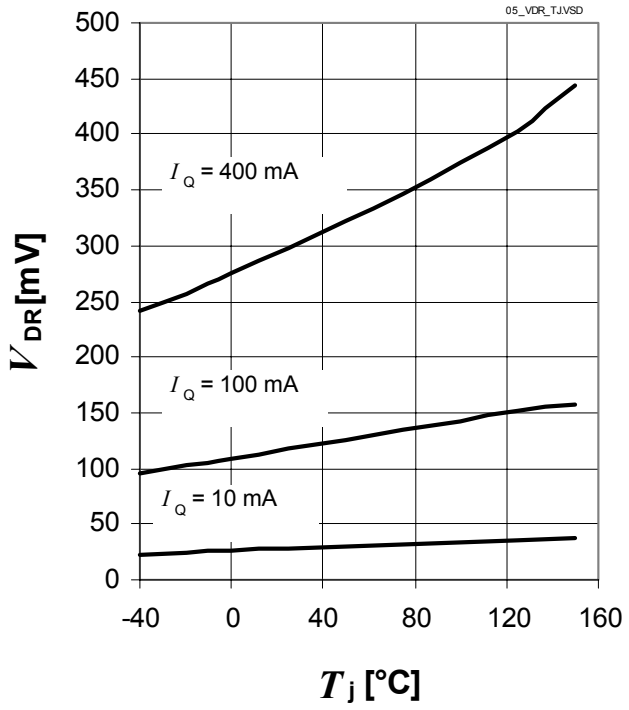
Output Voltage Variation ΔV_Q versus Junction Temperature T_J



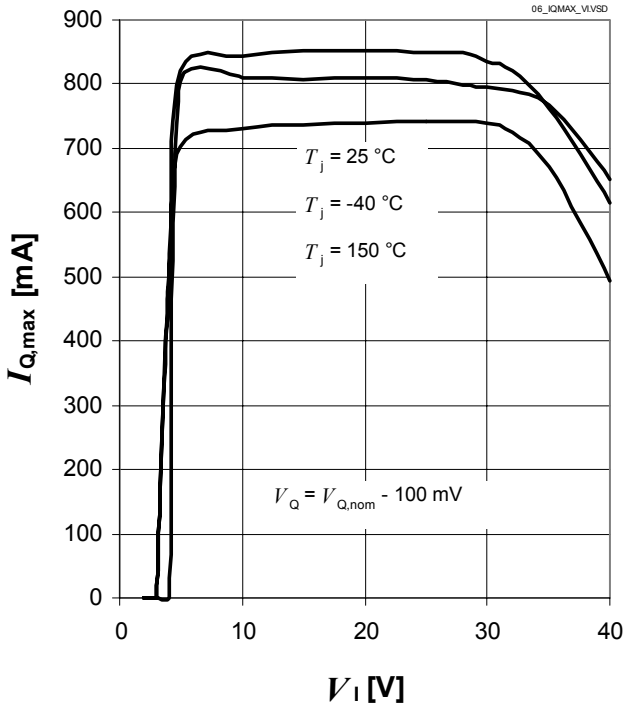
Dropout Voltage V_{dr} versus Output Current I_Q (5 V versions only)



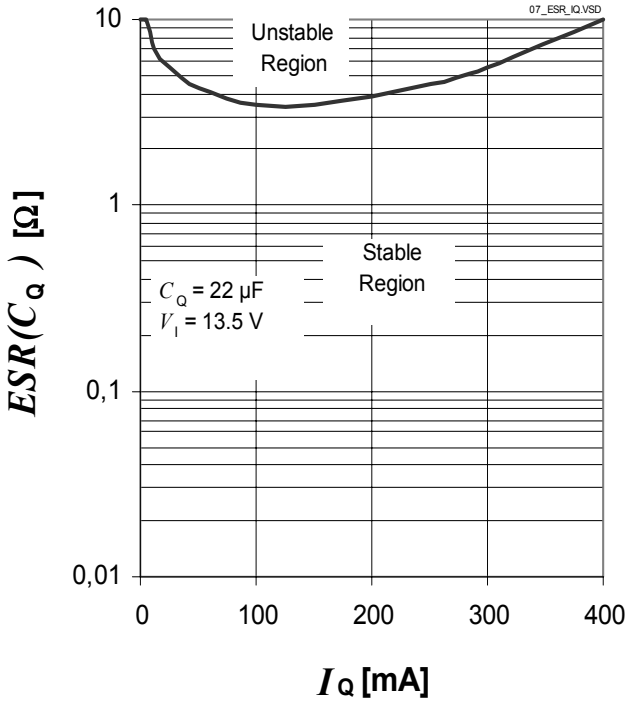
Dropout Voltage V_{dr} versus Junction Temperature (5 V versions only)



Maximum Output Current I_Q versus Input Voltage V_I



Region Of Stability: Output Capacitor's ESR $ESR(C_Q)$ versus Output Current I_Q



6 Package Outlines

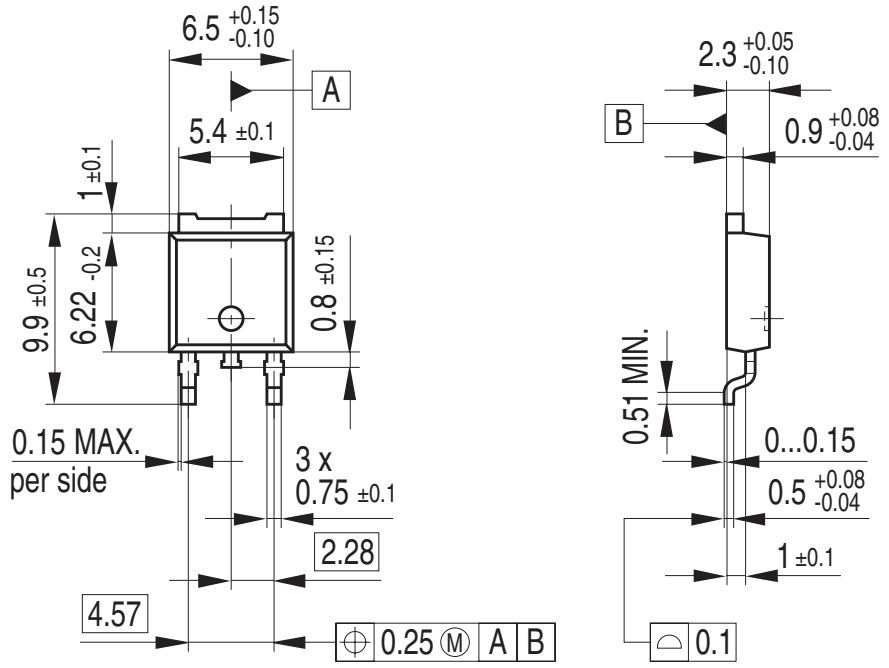


Figure 4 PG-TO252-3

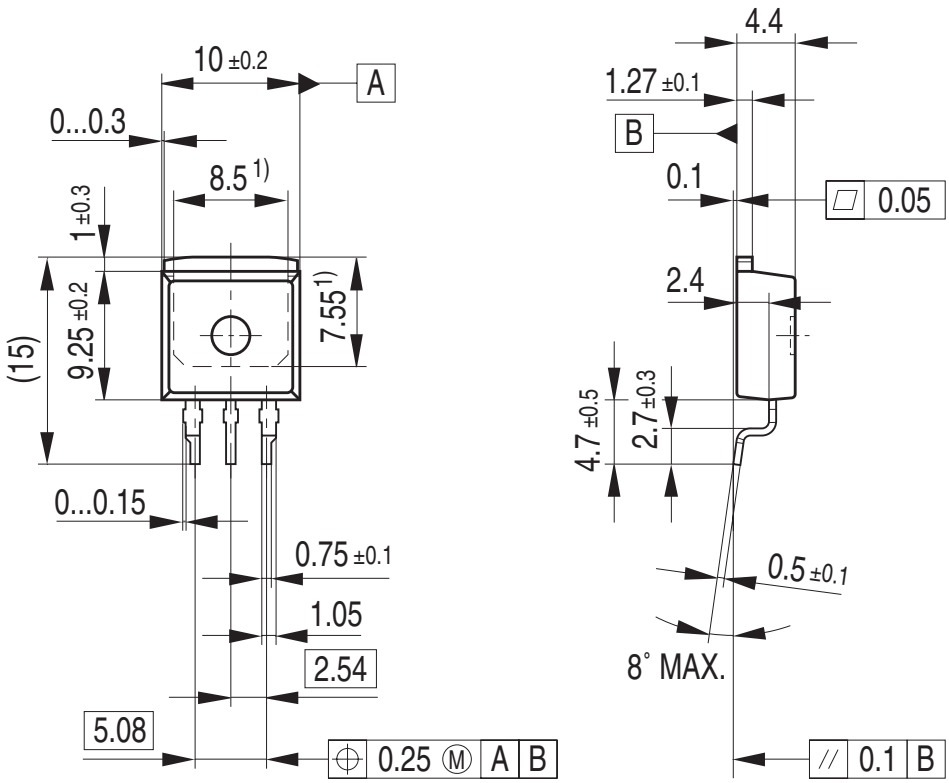


Figure 5 PG-TO263-3

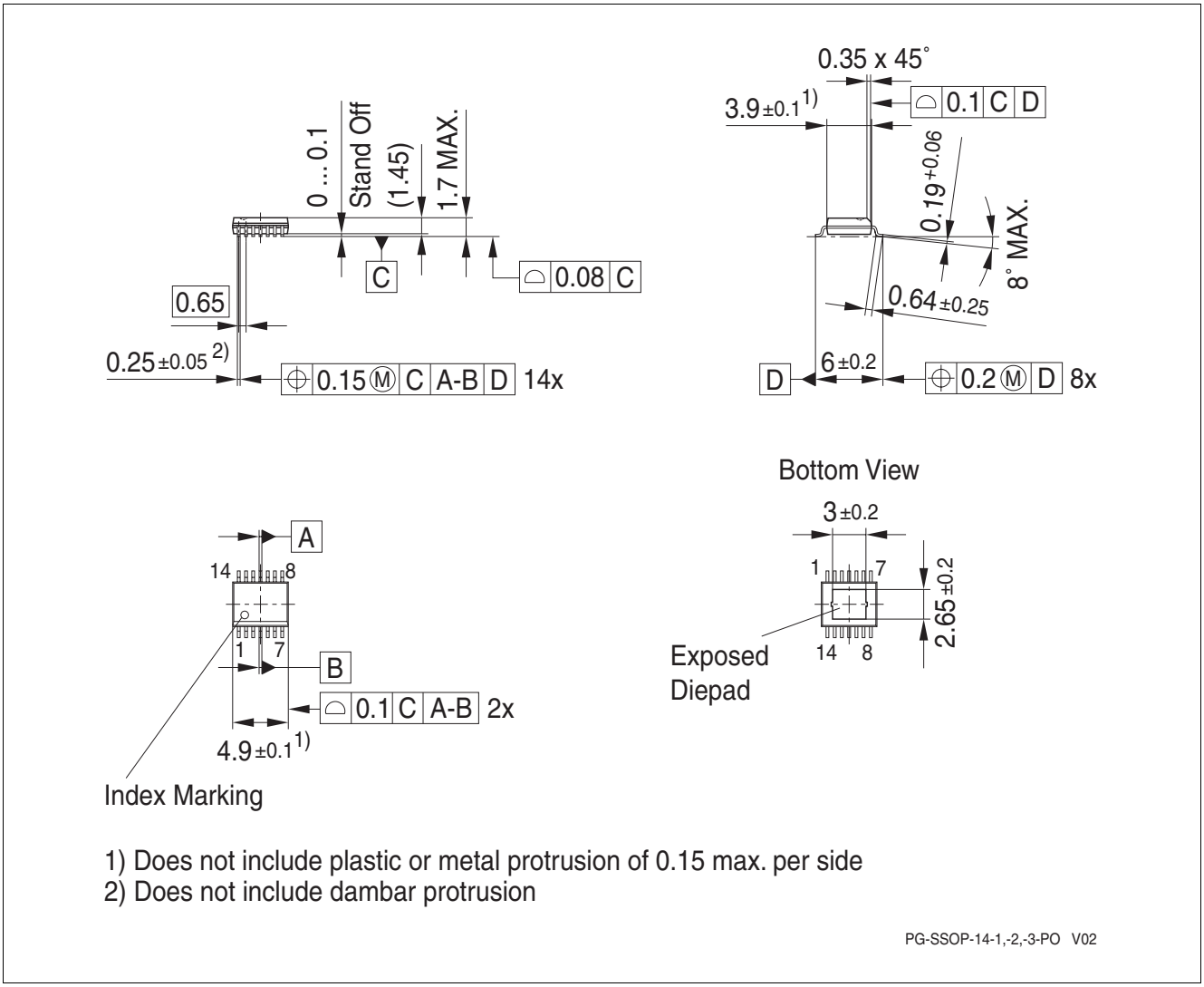


Figure 6 PG-SSOP-14 exposed pad

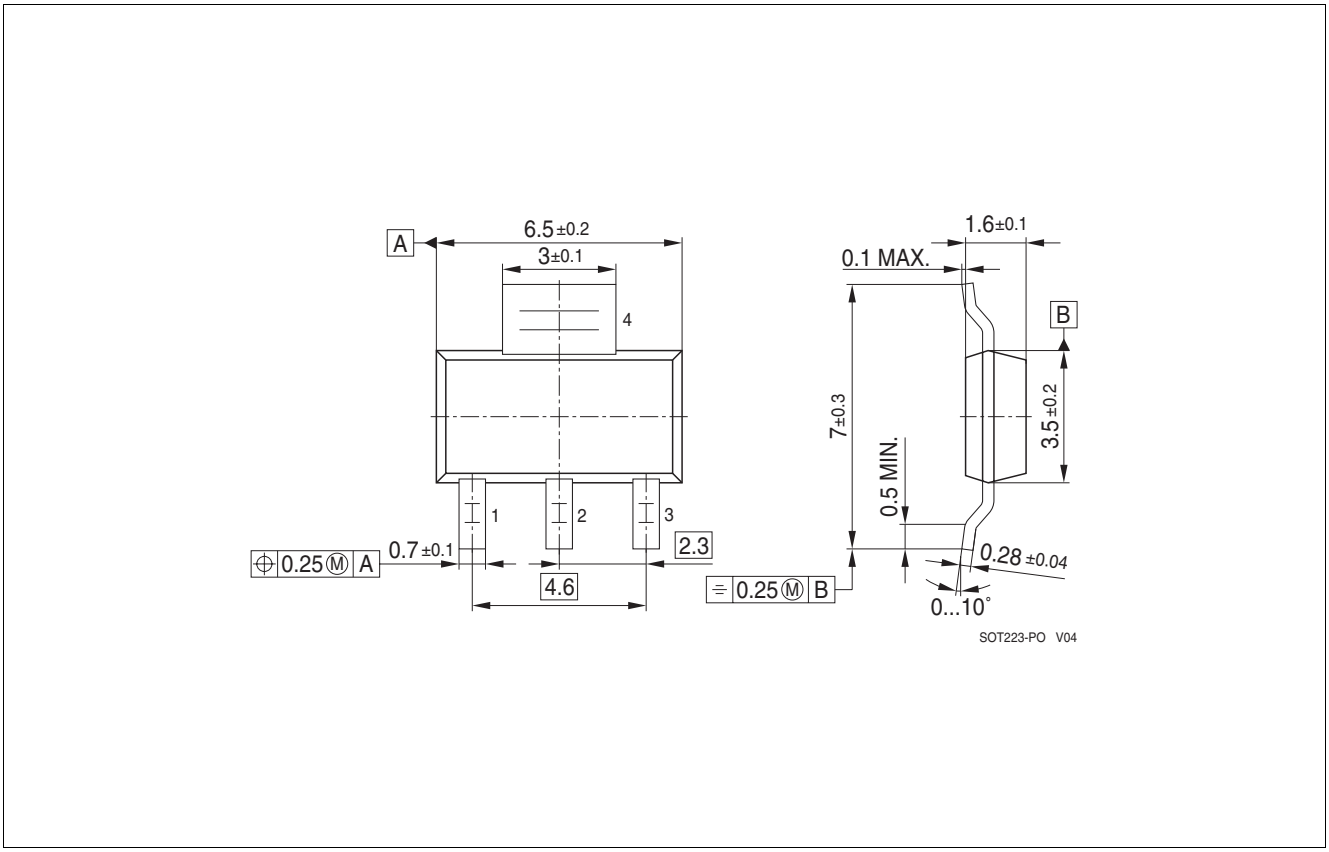


Figure 7 PG-SOT223-4

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

7 Revision History

Revision	Date	Changes
1.1	2010-01-13	Updated Version Data Sheet: version TLE42744EV50 in PG-SSOP-14 exposed pad and all related description added; 3.3V versions TLE42744GV33 in PG-TO263-3, TLE42744DV33 in PG-TO252-3 and TLE42744GSV33 in PG-SOT223-4 and all related description added
1.0	2009-01-14	Initial Version final Data Sheet

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