Factory Device Update

The following are all known device and document errors for the AMCC S5933 PCI Matchmaker revision QE and the 1998 device data book. The workarounds described below are factory suggestions and are not to imply the only or all possible solutions. Contact your local Field Application Engineer for new workaround developements. Also contact your AMCC FAE or local Insight Technical Sales Engineer for the latest design notes and data book corrections or see the AMCC home page at www.amcc.com.

D8: Bus Master Burst Write Operation with an Asynchronous FIFO Interface

Description: When performing a bus master write to the PCI bus, if only one location of the FIFO remains full, the S5933 deasserts FRAME# on the next clock to indicate the last data phase is in progress. If another value is written from the add-on at the right moment, an internal condition may cause IRDY# to remain asserted to sustain the burst, but FRAME# has already been deasserted.

Workaround: Externally synchronizing WRFIFO# or WR# to BPCLK moves the rising edge of the write strobe to prevent this event from occurring. Request separate D8 applications note from your local FAE or Insight TSE for more detail.

Status: No factory plan to re-spin.

D14.1: False Add-On to PCI FIFO Empty Indication

Description: If the last data in the Add-On to PCI FIFO is written by the S5933 to the PCI bus and receives a target retry, the FWE output and Add-On to PCI FIFO status bits will go active, indicating that the FIFO is empty, even though the final data has not yet been transferred. This is only a problem when using Add-On initiated bus mastering when FWE is used as a condition to deassert AMWEN at the end of a bus master write. Using FWE in this way could cause AMWEN to be deasserted before the last bus master write has successfully completed.

Workaround: Instead of using FWE, the Add-On interrupt signal, IRQ#, can be configured to go active when the transfer count reaches zero. The transfer count is only updated when data is successfully written. Request separate D14.1 applications note from your local FAE or Insight TSE for more detail.

NOTE: When FWE and the status bits indicate that the Add-On to PCI FIFO is empty, there are 8 empty locations in the FIFO. The data for the transfer which received the retry is stored in a holding register and is not involved.

Status: No factory plan to re-spin.

D17: PCI to Add-On FIFO Loses Data when Written w/o all PCI Byte Enables Asserted

Description: When writing to the FIFO from the PCI side (as a target), if the byte enable for the specified byte lane is not active, then that data could be lost. The problem is encountered when the S5933 Operation Registers are mapped to I/O space and the FIFO is written to 16 bits at a time, alternating between bytes 0,1 and bytes 2,3. Under certain conditions internal to the S5933, when the byte enable for the FIFO advance byte lane is not active, the data written is not captured by the FIFO.

Workaround 1: Always write the FIFO with the byte enable that corresponds to the FIFO advance byte lane active.

Workaround 2: Always perform 32-bit FIFO writes from the PCI bus.

Status: No factory plan to re-spin.

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PCI Interface Device Summary
S5933QE

B1: PCI Bus Hang when PCI initiated Bus Mastering is Disabled and the S5933 has GNT#

Description: S5933 PCI initiated bus mastering hangs the bus when the S5933 gets GNT# when another master is disabling bus mastering through the MCSR register before the transfer count reaches 0. This only occurs when the PCI bus arbiter offers GNT# to the S5933 while another master is executing a transaction on the PCI bus. If the active transaction disables S5933 bus mastering, then the S5933 will start a bus master transaction, then realize its bus mastering is disabled and hang on the bus with FRAME# active.

Workaround 1: Use the S5933 transfer count register(s) going to 0 in order to get the S5933 to stop bus mastering before it is disabled through the MCSR. The transfer counts should be programmed for the number of bytes that need to be transferred. When that number of bytes has been transferred, the S5933 will get off the bus normally.

Workaround 2: Write the transfer count to 4. This safely aborts the bus master transfer after one more PCI transaction. Then bus mastering can be disabled through the MCSR.

Status: No factory plan to re-spin.

B2: Bus Master Writes to Bus Master Read Address when Bus Master Write has priority over Bus Master Read

Description: When bus master writes are set up to have priority over bus master reads (MCSR register, bit 12=0, bit 8 =1) and both bus master writes and reads are enabled at the same time, then the S5933 could write to the read address.

Workaround: Set the bus master write and read to the same priority.

Status: : No factory plan to re-spin.

1998 Data Book Missing Data

Description: Page 3-176 figure 17 shows time t_{12} for ADR[6:2], BE[3:0] to DQ[31:0] valid. This is missing from table and should be 16 ns maximum for QE silicon. The same figure is missing the PTADR# high time of 12 ns min and PTADR# low to DQ[31:0] driven time of 13 ns.

Status: The 1999 data book will be updated.

1998 Data Book Description Error

Description: Page 3-78 describes FIFO reset functions for bits 25 and 26 of the AGCSTS register. These descriptions are swapped. Bit 25 performs the description for bit 26 and vise versa.

Status: The 1999 data book will be updated.

B3: Asynchronous Reset of PCI Bus Signals

Description: The S5933 does not reset or tri-state it's PCI bus signals on the assertion of motherboard system reset. The deassertion of reset and the first rising PCI clock edge initiate the tri-state of S5933 PCI output signals. The presence of the S5933 signals on the PCI bus while reset is asserted will cause bus contention when implementing the Hot Swap subsection of the *CompactPCI* specification.

Workaround: See the *CompactPCI* Hot Swap design note for a hardware solution when implementing Hot Swap.

Status: : No factory plan to re-spin.

B4: SERR# and INTA# Driven during FLT# Assertion

Description: Driving the FLT# signal low tri-states all S5933 pins with the exception of SDA, SCL, SERR# and INTA#. The SDA and SCL are unaffected by the FLT# signal. The SERR# and INTA# are driven low as long as FLT# is low.

Workaround: See the *CompactPCI* Hot Swap design note for a solution should the FLT# signal be required in a design.

Status: : No factory plan to re-spin.

B5: Bus Master Data Loss Following a Master Abort or Special Cycle

Description: The S5933 PCI Bus Master engine will read or write one DWORD using the wrong address when bus mastering resumes if, after S5933 bus ownership is lost, a special cycle or master abort occurs before the bus mastering resumes and is completed. This applies only to systems using chip sets which drive AD[31::11] to a logic one during master aborts and special cycles.

Workaround: A) Move the S5933 to a slot which does not assert IDSEL from an AD[31::11] logic one condition during special cycles or Master aborts.
B) Block the IDSEL signal to the S5933 from Add-On side before bus mastering.
C) Decode the CB/E signal when FRAME# is asserted and block IDSEL if not a configuration read or write.

Status: : No factory plan to re-spin.

B6: REQ# Fall Time May Cause Arbiter/System Lock-Up

Description: The S5933's PCI Bus REQ# output signal may not have enough drive power to provide a sufficient REQ# fall time for some arbiters. A slow fall time when used in systems containing a Winbond arbiter or Intel 440BX chip set may cause a system lock-up.

Workaround: Connect an external buffer between the S5933's REQ# output pin and the card's PCI Bus edge connector. The propigation delay of the buffer selected should not exceed 4 ns. An example low cost small SOT23 device from Fairchild Semiconductor can be seen at http://www.fairchildsemi.com/pf/NC/NC7SZ126.html.

Status: : No factory plan to re-spin.

NOTE: The 1997 S5933 data book incorporates many updates and clarifications over the Spring 1996 data book. The 1997 and 1998 data books reflect the S5933QB, QC and QE silicon functions and operation with the exception of each device's respective device summary documents.

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