

DESCRIPTION

The RH119 dual comparator features low input offset voltage and offset current, high voltage gain, guaranteed common mode rejection and input protection diodes.

The RH119 is capable of operation over a supply range from 5V to ± 15 V and can drive 25mV loads from each open collector output. A separate GND pin allows the RH119 to isolate system grounds.

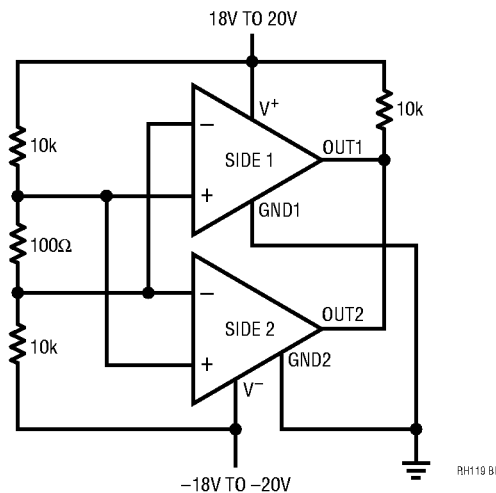
The wafer lots are processed to Linear Technology's in-house Class S flow to yield circuits usable in stringent military applications.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	36V
Output to Negative Supply Voltage	36V
Ground to Negative Supply Voltage	25V
Ground to Positive Supply Voltage	18V
Differential Input Voltage	± 5 V
Differential Input Current	± 5 mA
Input Voltage (See Note 1)	
Output Short-Circuit Duration	10 sec
Operating Temperature Range	-55°C to 125°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

 LTC and LT are registered trademarks of Linear Technology Corporation.

BURN-IN CIRCUIT



PACKAGE INFORMATION

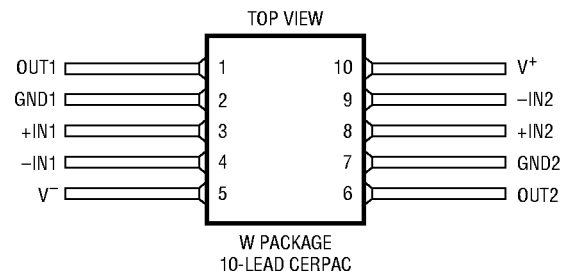
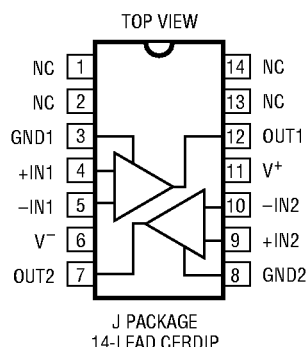
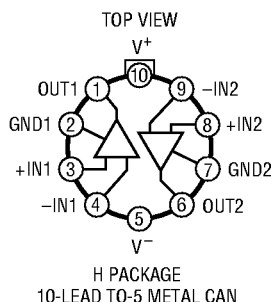


TABLE 1: ELECTRICAL CHARACTERISTICS (Preirradiation) (Note 2)

SYMBOL	PARAMETER	CONDITIONS	NOTES	T _J = 25°C			SUB-GROUP	-55°C T _{AJ}			SUB-GROUP	UNITS
				MIN	TYP	MAX		MIN	TYP	MAX		
V _{OS}	Input Offset Voltage	V _S = ±15V, V _{CM} = 0V	3			4	1			7	2,3	mV mV
CMRR	Common Mode Rejection Ratio			90			1					dB
I _{OS}	Input Offset Current		3			75	1			100	2,3	nA
I _B	Input Bias Current					500	1			1000	2,3	nA
A _V	Voltage Gain			10			4					V/mV
t _R	Response Time		4	80	200		4			200	5,6	ns
V _{SAT}	Saturation Voltage	V _{IN} -5mV, I _O = 25mA				1.5	1					V
		V ⁺ 4.5V, V ⁻ = 0V V _{IN} -6mV, I _{SINK} 3.2mA T _A 0°C T _A 0°C				0.4	1			0.4 0.6	2 3	V V
	Output Leakage Current	V _{IN} 5mV, V _{OUT} = 35V				2	1			10	2,3	μA
	Input Voltage Range	V _S = ±15V V ⁺ = 5V, V ⁻ = 0V		-12 1		12 3	1 1	-12 1		12 3	2,3 2,3	V V
	Differential Input Voltage					±5	1			±5	2,3	V
I _S	Supply Current	V ⁺ = 5V, V ⁻ = 0V			4.3							mA
	Positive Supply Current	V _S = ±15V				11.5	1					mA
	Negative Supply Current	V _S = ±15V				4.5	1					mA

TABLE 1A: ELECTRICAL CHARACTERISTICS (Postirradiation) (Note 5)

SYMBOL	PARAMETER	CONDITIONS	NOTES	10Krad(Si)		20Krad(Si)		50Krad(Si)		100Krad(Si)		200Krad(Si)		UNITS
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V _{OS}	Offset Voltage				4		4		4		4		8	mV
I _{OS}	Input Offset Current		3		75		100		150		300		500	nA
I _B	Input Bias Current		3		500		750		1000		1500		2000	nA
A _{VOL}	Large-Signal Voltage Gain			10		10		10		10		5		V/mV
V _{SAT}	Saturation Voltage	V _{IN} -5mV, I _O = 25mA			1.5		1.5		1.5		1.5		1.5	V
		V ⁺ 4.5V, V ⁻ = 0V V _{IN} -6mV, I _{SINK} 3.2mA			0.4		0.4		0.4		0.4		0.4	V
CMRR	Common Mode Rejection Ratio			90		90		90		90		90		dB
I _S	Positive Supply Current	V _S = ±15V			11.5		11.5		11.5		11.5		11.5	mA
	Negative Supply Current	V _S = ±15V			4.5		4.5		4.5		4.5		4.5	mA
	Output Leakage Current	V _{IN} 5mV, V _{OUT} 35V			2		2		2		2		2	μA

ELECTRICAL CHARACTERISTICS (Continued)

Note 1: For supply voltages less than $\pm 15\text{V}$, the maximum input voltage is equal to the supply voltage.

Note 2: Unless otherwise noted, supply voltage equals $\pm 15\text{V}$ and $T_A = 25^\circ\text{C}$. The GND pin is grounded. Note that the maximum voltage allowed between the GND pin and V^+ is 18V . Do not tie the GND pin to V^- when the power supply voltage exceeds $\pm 9\text{V}$. The offset voltage, offset current and bias current specifications apply for all supply voltages between $\pm 15\text{V}$ and 5V unless otherwise specified.

Note 3: The offset voltages and currents given are the maximum values required to drive the output within 1V of either supply with a 1mA load—thus, these parameters define an error band and take into account the worst-case effects of voltage gain and input impedance.

Note 4: Response time specified for a 100mV input step with 5mV overdrive.

Note 5: $V_S = \pm 15\text{V}$, $V_{CM} = 0\text{V}$, $T_A = 25^\circ\text{C}$ unless otherwise noted.

TABLE 2: ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUP
Final Electrical Test Requirements (Method 5004)	1*,2,3,4
Group A Test Requirements (Method 5005)	1,2,3,4
Group C and D End Point Electrical Parameters (Method 5005)	1

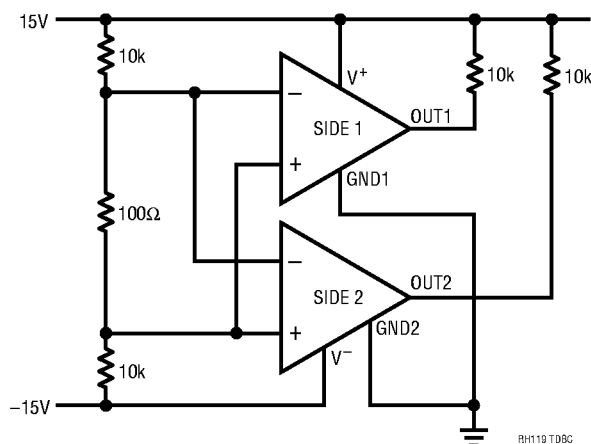
* PDA Applies to subgroup 1. See PDA Test Notes.

PDA Test Notes

The PDA is specified as 5% based on failures from group A, subgroup 1, tests after cooldown as the final electrical test in accordance with method 5004 of MIL-STD-883 Class B. The verified failures (including Delta parameters) of group A, subgroup 1, after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent for the lot.

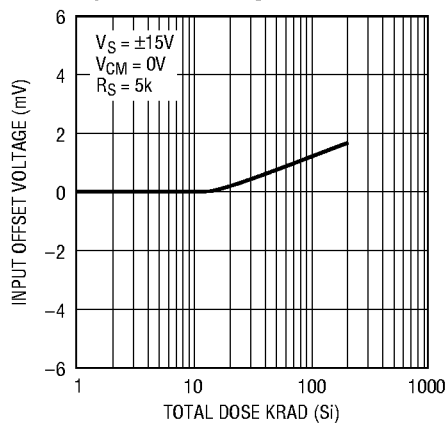
Linear Technology Corporation reserves the right to test to tighter limits than those given.

TOTAL DOSE BIAS CIRCUIT



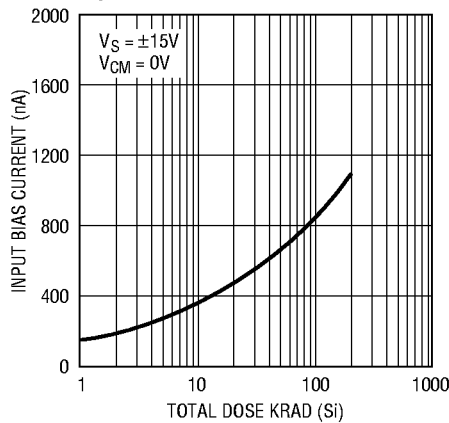
TYPICAL PERFORMANCE CHARACTERISTICS

Input Offset Voltage



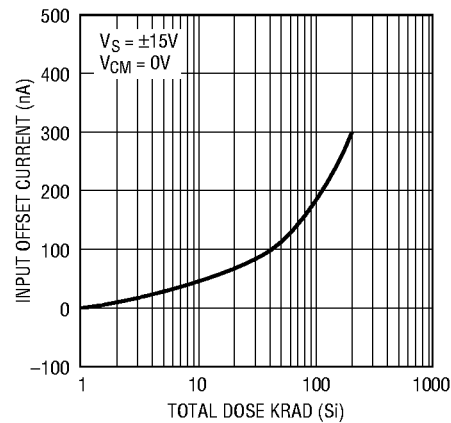
RH119 G01

Input Bias Current



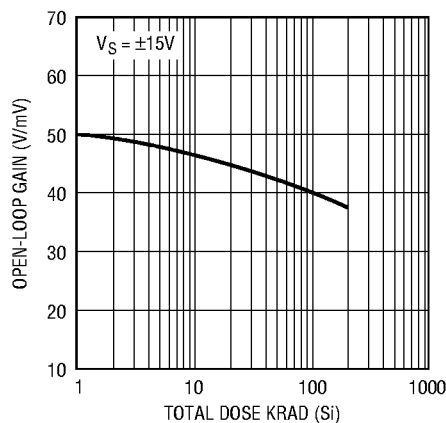
RH119 G02

Input Offset Current



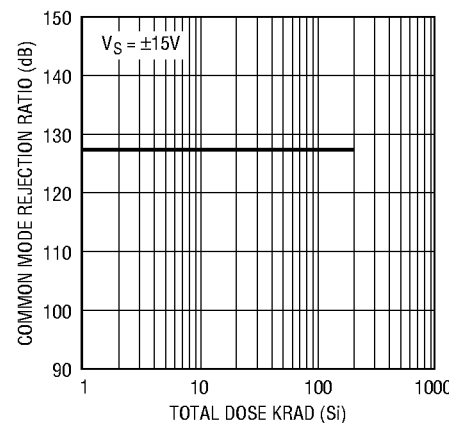
RH119 G03

Open-Loop Gain



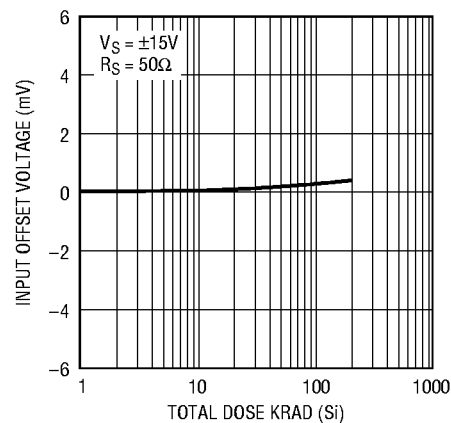
RH119 G04

Common Mode Rejection Ratio



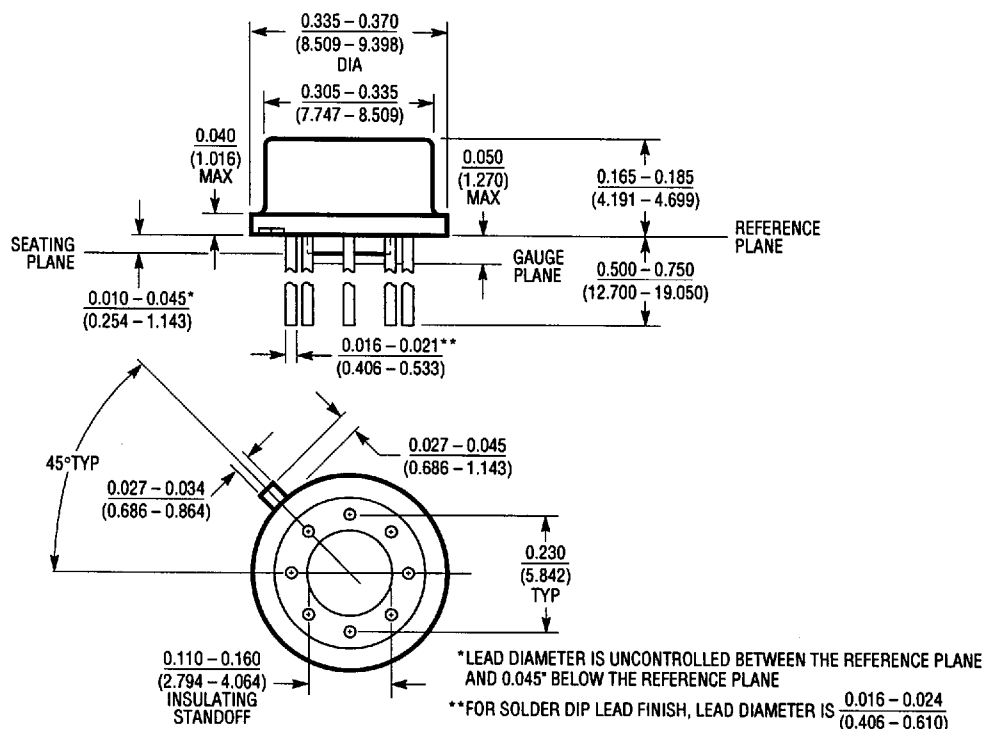
RH119 G05

Input Offset Voltage



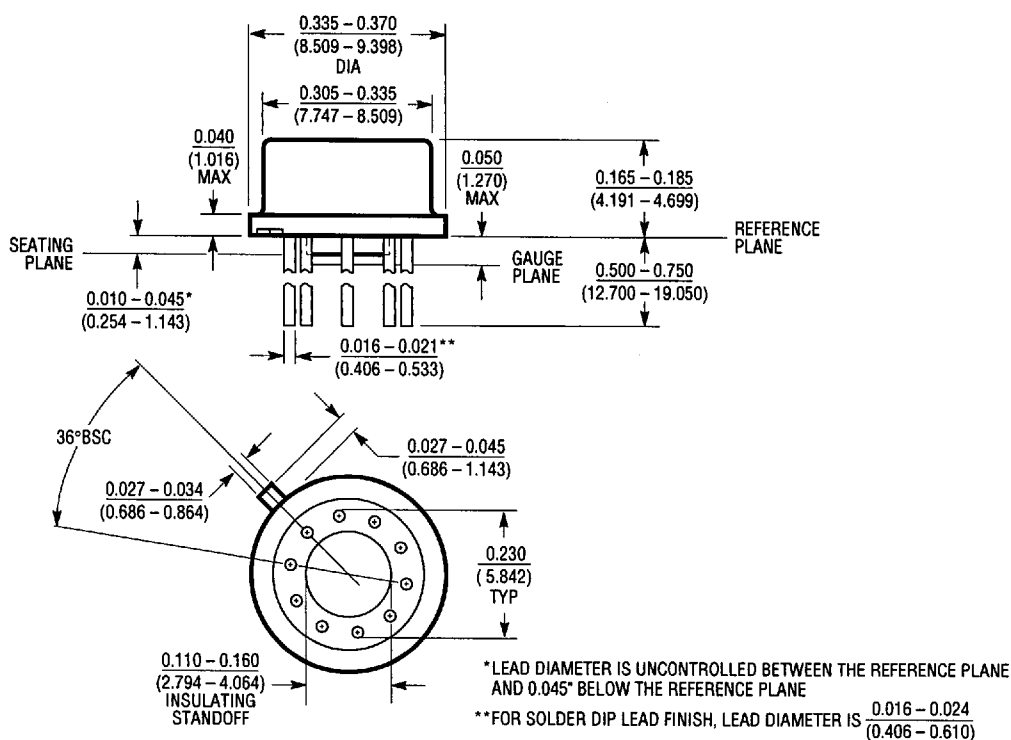
RH119 G06

H Package 8-Lead TO-5 Metal Can (0.230 PCD) (LTC DWG # 05-08-1321)



H8 (TO-5) 0.230 PCD 0595

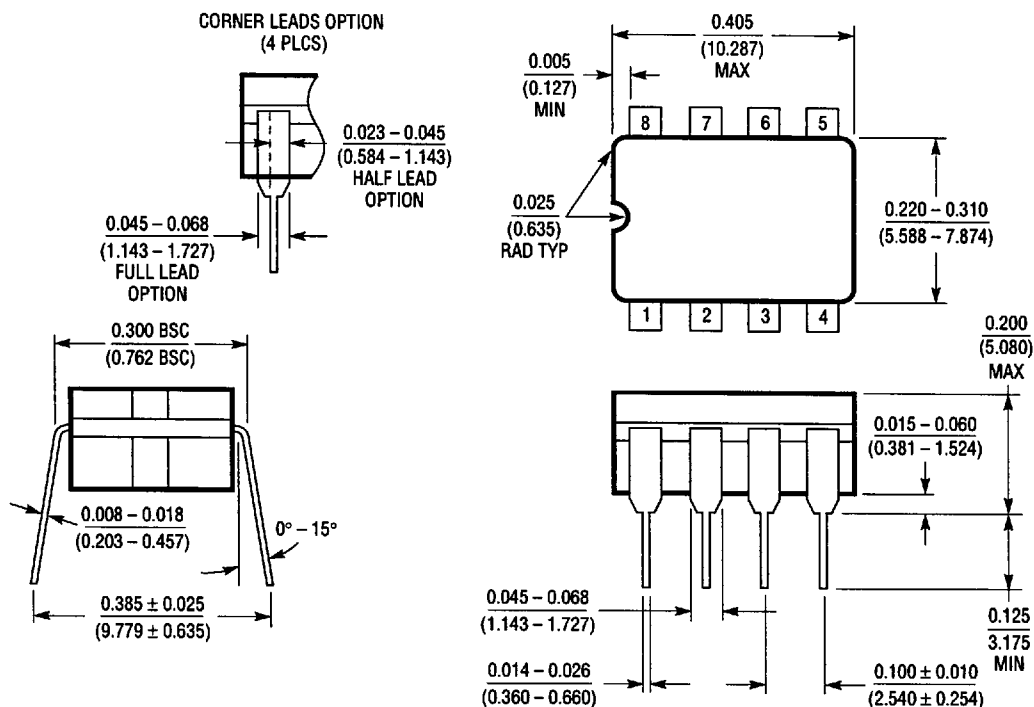
H Package 10-Lead TO-5 Metal Can (LTC DWG # 05-08-1322)



H10(TO-5) 0595

PACKAGE DIMENSIONS

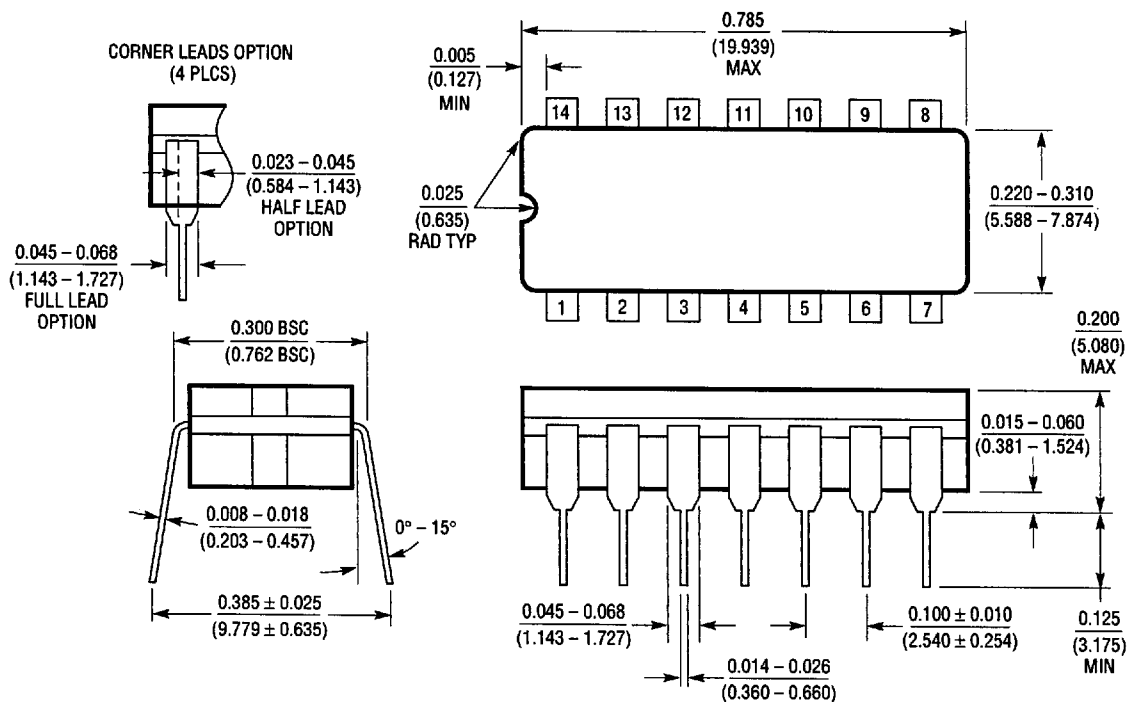
J8 Package 8-Lead CERDIP (Narrow 0.300, Hermetic) (LTC DWG # 05-08-1110)



NOTE: LEAD DIMENSIONS APPLY TO SOLDER DIP/PLATE OR TIN PLATE LEADS.

J8 0694

J Package 14-Lead CERDIP (Narrow 0.300, Hermetic) (LTC DWG # 05-08-1110)

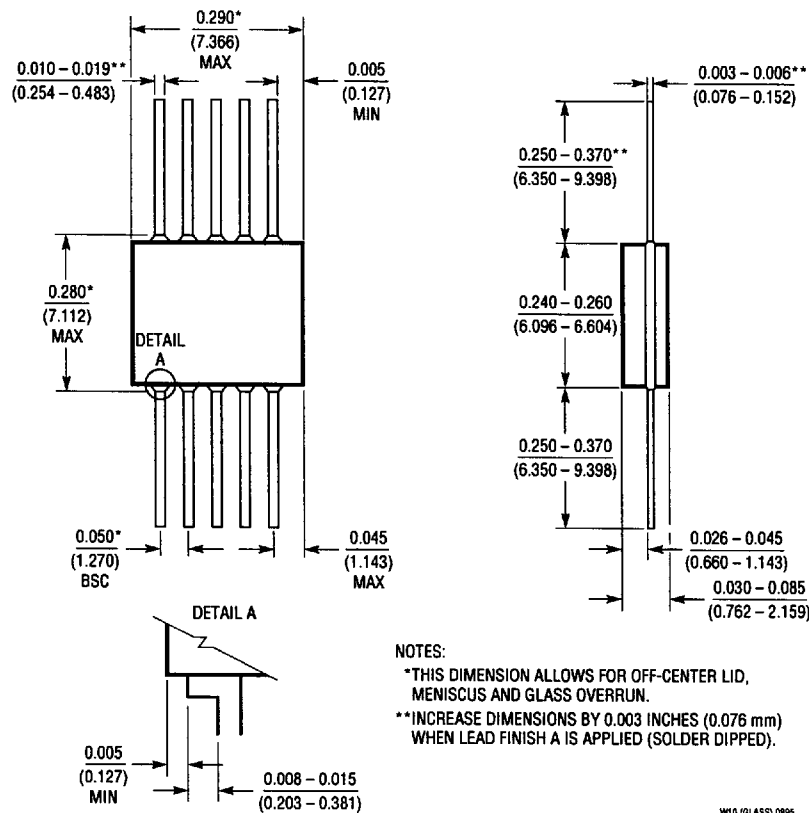


NOTE: LEAD DIMENSIONS APPLY TO SOLDER DIP OR TIN PLATE LEADS.

J14 0694

PACKAGE DIMENSIONS

W Package 10-Lead Flatpak Glass Sealed (Hermetic) (LTC DWG # 05-08-1130)



WB Package 10-Lead Flatpak Metal Sealed Bottom Brazed (Hermetic) (LTC DWG # 05-08-1230)

