QL8x12
pASIC 1 FAMILY
Very-High-Speed 1K (3K) Gate CMOS FPGA

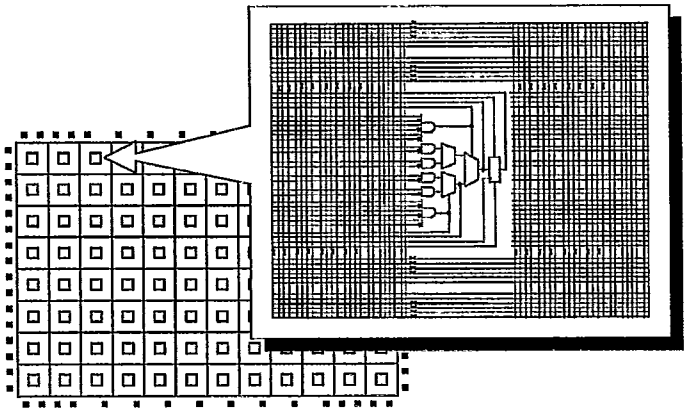
pASIC HIGHLIGHTS

- **Very High Speed** – ViaLink™ metal-to-metal programmable–via antifuse technology, allows counter speeds over 100 MHz, and logic cell delays of under 4 ns.
- **High Usable Density** – An 8-by-12 array of 96 logic cells provides 3000 total available, with 1000 typically usable "gate array" gates in 44- and 68-pin PLCC, and 100-pin Thin PQFP packages.
- **Low-Power, High-Output Drive** – Stand-by current typically 2 mA. A 16-bit counter operating at 100 MHz consumes 50 mA. Minimum IOL and IOH of 8 mA.
- **Flexible FPGA Architecture** – The pASIC™ logic cell supports efficient, high-speed arithmetic, counter, data path, state machine and random logic applications with up to 14-input gates.
- **Low-Cost, Easy-to-Use Design Tools** – Designs entered and simulated using third-party, CAE tools. Fast, fully automatic place and route on PC and workstation platforms.

...3000 total available gates

QL8x12 Block Diagram

96 Logic Cells



■ = Up to 56 I/O cells, 6 Input high-drive cells, 2 Input/CLK (high-drive) cells.

QUICKLOGIC

PRODUCT SUMMARY

The QL8x12 is a member of the pASIC 1 Family of very-high-speed CMOS user-programmable ASIC (pASIC) devices. The 96-logic cell field-programmable gate array (FPGA) offers up to 3000 total available, with 1000 typically usable "gate array" gates (equivalent to 3000 gate claims of EPLD or LCA vendors) of high-performance general-purpose logic in 44- and 68-pin plastic leaded chip carrier packages.

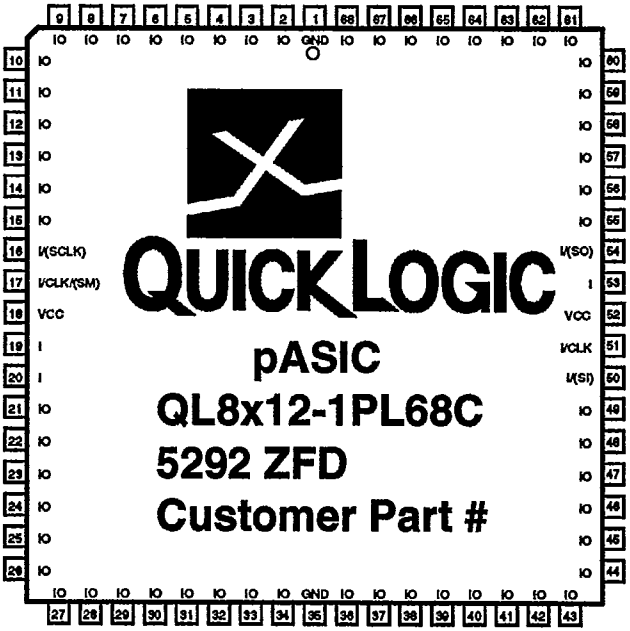
Low-impedance, metal-to-metal, ViaLink interconnect technology provides nonvolatile custom logic capable of operating at counter speeds above 100 MHz. Combined with input delays of 2 ns and output delays under 4 ns, this permits high-density programmable devices to be used with today's fastest CISC and RISC microprocessors.

Designs are entered into the QL8x12 using a pASIC Toolkit combining third-party general-purpose design entry and simulation tools with device-specific place and route and programming software. Ample on-chip routing channels are provided to allow fast, fully automatic place and route of high gate utilization designs.

FEATURES

- 56 Bidirectional Input/Output pins
- 8 Dedicated Input/High-Drive Clock pins
- Input + logic cell + output delays under 9 ns
- Chip-to-chip operating frequencies up to 85 MHz
- Internal state machine frequencies up to 100 MHz
- Clock skew <2 ns
- Input hysteresis provides high noise immunity
- Built-in scan path permits 100% factory testing of logic and I/O cells and functional testing with Automatic Test Vector Generation (ATVG) software after programming
- Ample routing tracks permit fully automatic place and route of designs using up to 100% of internal logic cells
- 68-pin PLCC compatible with EPLD 1800 and LCA 2064 industry-standard pinouts
- 1µ CMOS gate array process with ViaLink programming technology

Pinout Diagram 44-pin PLCC



Pinout Diagram 68-pin PLCC

Pins identified I/SCLK, SM, SO, and SI are used during scan path testing operation.

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... –0.5 to 7.0V
Input Voltage ..... –0.5 to VCC +0.5V
ESD Pad Protection ..... ± 2000V
DC Input Current ..... ± 20 mA
Latch-up Immunity ..... ±100 mA

Storage Temperature
Ceramic ..... –65°C to + 150°C
Plastic ..... –40°C to + 125°C
Lead Temperature ..... 300°C

OPERATING RANGE

Symbol	Parameter		Military		Industrial		Commercial		Unit
			Min	Max	Min	Max	Min	Max	
VCC	Supply Voltage		4.5	5.5	4.5	5.5	4.75	5.25	V
TA	Ambient Temperature		-55		-40	85	0	70	°C
TC	Case Temperature			125					°C
K	Delay Factor	-0 Speed Grade	0.39	2.12	0.4	1.94	0.46	1.80	
		-1 Speed Grade	0.39	1.56	0.4	1.43	0.46	1.33	
		-2 Speed Grade					0.46	1.25	

DC CHARACTERISTICS over operating range

Symbol	Parameter	Conditions	Min	Max	Unit
VIH	Input HIGH Voltage		2.0		V
VIL	Input LOW Voltage			0.8	V
VOH	Output HIGH Voltage	IOH = -4 mA	3.7		V
		IOH = -8 mA	2.4		V
		IOH = -10 µA	VCC-0.1		V
VOL	Output LOW Voltage	IOL = 8 mA		0.4	V
		IOL = 10 µA		0.1	V
II	Input Leakage Current	VI = VCC or GND	-10	10	µA
IOZ	3-State Output Leakage Current	VI = VCC or GND	-10	10	µA
CI	Input Capacitance [1]			10	pF
IOS	Output Short Circuit Current	VO = GND	-10	-80	mA
		VO = VCC	30	140	mA
ICC	Supply Current [2]	VI, VIO = VCC or GND		10	mA

Notes:

[1] CI = 20 pF Max on Pin 50

[2] For AC conditions use the formula described in Section 5 — Power vs Operating Frequency.

[3] Worst case Propagation Delay times over process variation at VCC = 5.0V and TA = 25°C. Multiply by the appropriate Delay Factor, K, for speed grade, voltage and temperature settings as specified in the Operating Range. All inputs are TTL with 3 ns linear transition time between 0 and 3 volts.

AC CHARACTERISTICS at VCC = 5V, TA = 25°C (K = 1.00)

Logic Cell

Symbol	Parameter	Propagation Delays (ns) [3] Fanout				
		1	2	3	4	8
tPD	Combinatorial Delay [4]	3.6	4.0	4.4	5.0	8.3
tSU	Setup Time [4]	3.9	3.9	3.9	3.9	3.9
tH	Hold Time	0.0	0.0	0.0	0.0	0.0
tCLK	Clock to Q Delay	3.0	3.3	3.8	4.3	4.9
tSET	Set Delay	2.7	3.1	3.5	4.1	7.4
tRESET	Reset Delay	2.9	3.2	3.6	4.2	7.5
tCWHI	Clock High Time	2.0	2.0	2.0	2.0	2.0
tCWLO	Clock Low Time	3.6	3.6	3.6	3.6	3.6
tSW	Set Width	2.1	2.1	2.1	2.1	2.1
tRW	Reset Width	1.9	1.9	1.9	1.9	1.9

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Input Cells

Symbol	Parameter	Propagation Delays (ns) [3] Fanout				
		1	2	3	4	8
tIN	Input Delay (high drive)	3.7	3.8	4.2	4.6	6.4
tINI	Input, Inverting Delay (high drive)	3.5	3.6	4.0	4.4	6.2
tIO	Input Delay (bidirectional pad)	2.3	2.6	3.2	4.1	5.5

Output Cell

Symbol	Parameter	Propagation Delays (ns) [3] Output Load Capacitance (pF)				
		30	50	75	100	150
tOUTLH	Output Delay Low to High	3.1	3.8	4.6	5.5	7.2
tOUTHL	Output Delay High to Low	3.1	3.9	5.0	6.1	8.3
tPZH	Output Delay Tri-state to High	4.4	5.3	6.5	7.7	10.1
tPZL	Output Delay Tri-state to Low	4.0	4.6	5.4	6.2	7.7
tPHZ	Output Delay High to Tri-state [5]	3.3				
tPLZ	Output Delay Low to Tri-state [5]	3.7				

Notes:

[4] These limits are derived from worst case values for a representative selection of the slowest paths through the pASIC logic cell including net delays. Guaranteed delay values for specific paths should be determined from simulation results.

[5] The following loads are used for tPXZ:

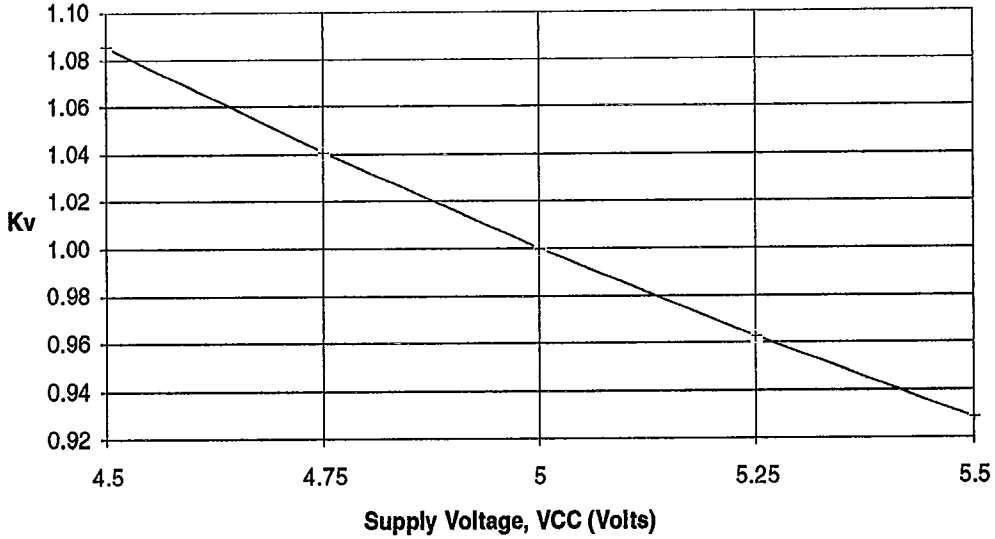
Clock Driver

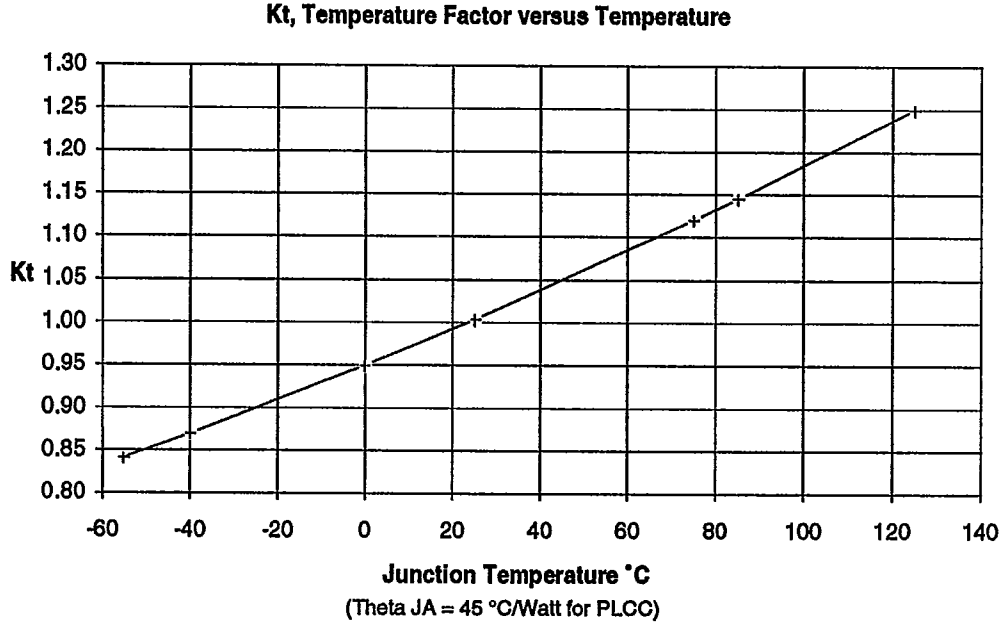
Symbol	Parameter	Clock Drivers Wired Together	Propagation Delays (ns) [3] Fanout				
			12	24	48	72	96
tCKD	Clock Driver Delay	1	4.8	6.8			
		2		4.8	6.1		
		3			5.4	6.4	7.5
		4				5.8	6.2
tCKDI	Clock Driver, Inverting Delay	1	5.2	7.2			
		2		5.1	6.4		
		3			5.7	6.7	7.3
		4				6.2	6.5

AC Performance

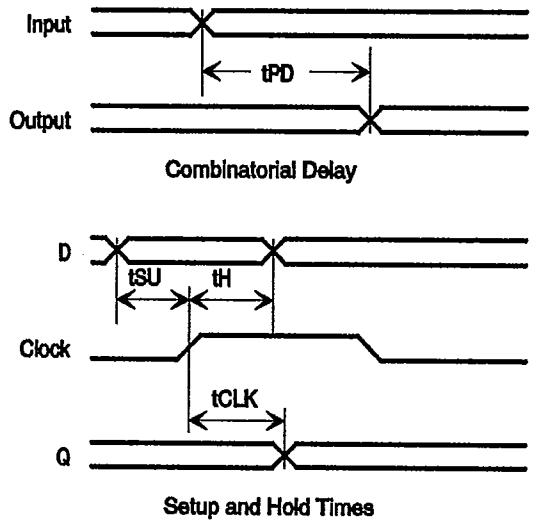
Propagation delays depend on routing, fanout, load capacitance, supply voltage, junction temperature, and process variation. The AC Characteristics are a design guide to provide initial timing estimates at nominal conditions. Worst case estimates are obtained when nominal propagation delays are multiplied by the appropriate Delay Factor, K, as specified in the Operating Range. The effects of voltage and temperature variation are illustrated in the following graphs. The SpDE Toolkit incorporates data sheet AC Characteristics into the QDIF database for pre-place-and-route simulations. The SpDE Delay Modeler extracts specific timing parameters for precise simulation results following place and route.

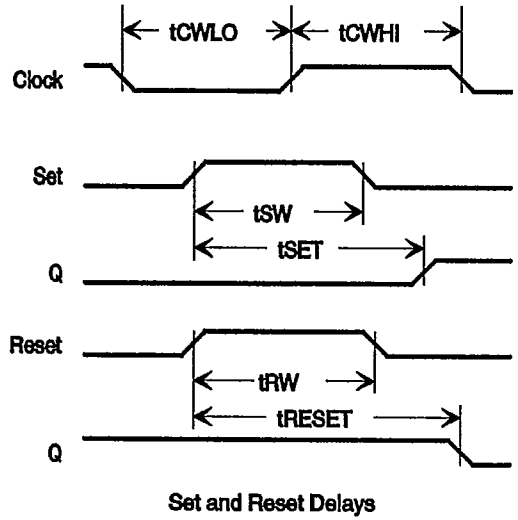
Kv, Voltage Factor versus Vcc, Supply Voltage





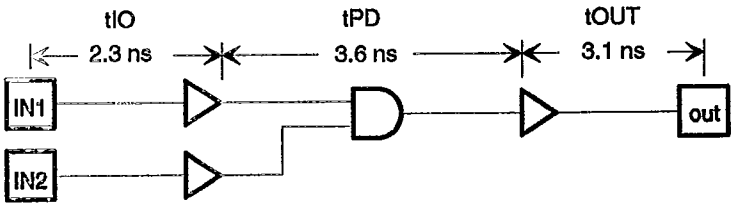
Timing Waveforms





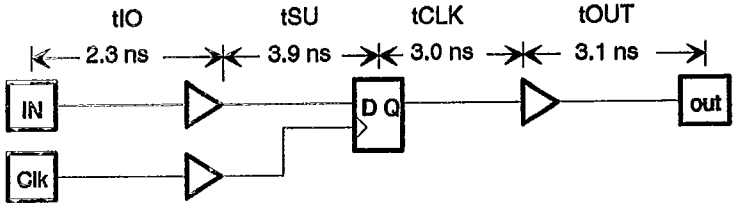
Combinatorial Delay Example

Nominal I/O Delays Load = 30 pF



Input Delay + Combinatorial Delay + Output Delay = 9.0 ns

Sequential Delay Example



Input Delay + Reg Setup + Clock to Output + Output Delay = 12.3 ns

ORDERING INFORMATION

QL 8x12 -1 PL68 C

- QL — QuickLogic pASIC device prefix
- 8x12 — pASIC device part number for 8 by 12 array of 96 logic cells
- -1 — Speed Grade (see data sheet)
- PL68 — Package Code
  - First Letter
    - P = Plastic
    - C = Ceramic
  - Second Letter
    - L = LCC
    - F = QFP
    - G = PGA
  - Number of Leads
    - 68 = 68 Leads
- C — Operating Range
  - C = Commercial
  - I = Industrial
  - M = Military