

# HM50256 Series

262144-word × 1-bit Dynamic Random Access Memory

## FEATURES

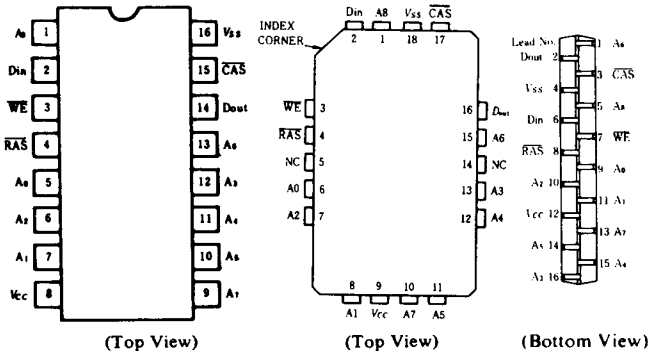
- Industry Standard 16-Pin DIP, 18-Pin PLCC, 16-Pin ZIP
- Single 5V (±10%)
- On chip substrate bias generator
- Low Power: 350mW active, 20mW standby
- High speed: Access Time 120ns/150ns/200ns(max.)
- Common I/O capability using early write operation
- Page mode capability
- TTL compatible
- 256 refresh cycles . . . (4ms)
- 3 variations of refresh . . . RAS only refresh, CAS before RAS refresh, Hidden refresh

## ORDERING INFORMATION

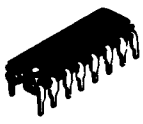
Type No.	Access Time	Package
HM50256P-12 HM50256P-15 HM50256P-20	120ns 150ns 200ns	300 mil 16 pin Plastic DIP
HM50256ZP-12 HM50256ZP-15 HM50256ZP-20	120ns 150ns 200ns	16 pin Plastic ZIP
HM50256CP-12 HM50256CP-15 HM50256CP-20	120ns 150ns 200ns	18 pin PLCC

## PIN ARRANGEMENT

- HM50256P Series
- HM50256CP Series
- HM50256ZP Series




HM50256P Series



(DP-16B)

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HM50256CP Series



(CP-18)

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HM50256ZP Series



(ZP-16)

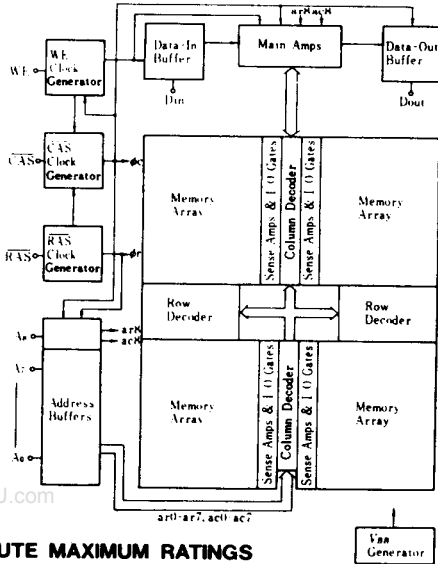
## PIN DESCRIPTION

A <sub>0</sub> - A <sub>7</sub>	Address Inputs
CAS	Column Address Strobe
Din	Data In
Dout	Data Out
RAS	Row Address Strobe
WE	Read/Write Input
V <sub>cc</sub>	Power (+5V)
V <sub>ss</sub>	Ground
A <sub>8</sub> - A <sub>17</sub>	Refresh Address Inputs

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**■ BLOCK DIAGRAM**



**■ ABSOLUTE MAXIMUM RATINGS**

- Voltage on any pin relative to  $V_{SS}$  . . . . . -1V to +7V
- Operating temperature,  $T_a$  (Ambient) . . . . . 0°C to +70°C
- Storage temperature . . . . . -55°C to +125°C
- Short circuit output current . . . . . 50mA
- Power dissipation . . . . . 1W

**■ RECOMMENDED DC OPERATING CONDITIONS ( $T_a=0$  to +70°C)**

Parameter	Symbol	min	typ	max	Unit	Note
Supply Voltage	$V_{CC}$	4.5	5.0	5.5	V	1
Input High Voltage	$V_{IH}$	2.4	—	6.5	V	1
Input Low Voltage	$V_{IL}$	-1.0	—	0.8	V	1

Note) 1. All voltages referenced to  $V_{SS}$

**■ DC ELECTRICAL CHARACTERISTICS ( $T_a=0$  to +70°C,  $V_{CC}=5V \pm 10\%$ ,  $V_{SS}=0V$ )**

Parameter	Symbol	HM50256-12		HM50256-15		HM50256-20		Unit	Notes
		min	max	min	max	min	max		
Operating Current (RAS, CAS = Cycling; $t_{RC} = \min$ )	$I_{CC1}$	—	83	—	70	—	55	mA	1
Standby Current (RAS = $V_{IH}$ , Dout = High Impedance)	$I_{CC2}$	—	4.5	—	4.5	—	4.5	mA	
Refresh Current (RAS only Refresh, $t_{RC} = \min$ )	$I_{CC3}$	—	62	—	53	—	42	mA	
Standby Current (RAS = $V_{IH}$ , Dout = Enable)	$I_{CC5}$	—	10	—	10	—	10	mA	1
Refresh Current (CAS before RAS Refresh, $t_{RC} = \min$ )	$I_{CC6}$	—	69	—	58	—	45	mA	
Page Mode Supply Current (RAS = $V_{IL}$ , CAS = Cycling, $t_{PC} = \min$ )	$I_{CC7}$	—	57	—	48	—	37	mA	
Input leakage ( $0 < V_{in} < 7V$ )	$I_{LI}$	-10	10	-10	10	-10	10	$\mu A$	
Output leakage ( $0 < V_{out} < 7V$ , Dout = Disable)	$I_{LO}$	-10	10	-10	10	-10	10	$\mu A$	
Output levels High ( $I_{out} = -5mA$ )	$V_{OH}$	2.4	$V_{CC}$	2.4	$V_{CC}$	2.4	$V_{CC}$	V	
Output levels Low ( $I_{out} = 4.2mA$ )	$V_{OL}$	0	0.4	0	0.4	0	0.4	V	

Note) 1.  $I_{CC}$  depends on output loading condition when the device is selected.  $I_{CC \max}$  is specified at the output open condition.



■ CAPACITANCE ( $V_{CC} = 5V \pm 10\%$ ,  $T_a = 25^\circ C$ )

Parameter		Symbol	typ	max	Unit	Notes
Input Capacitance	Address, Data-in	$C_{I1}$	—	5	pF	1
	Clocks	$C_a$	—	7		1, 2
Output Capacitance	Data-out	$C_o$		7		1, 2

Notes) 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.  
 2. CAS =  $V_{in}$  to disable Dout.

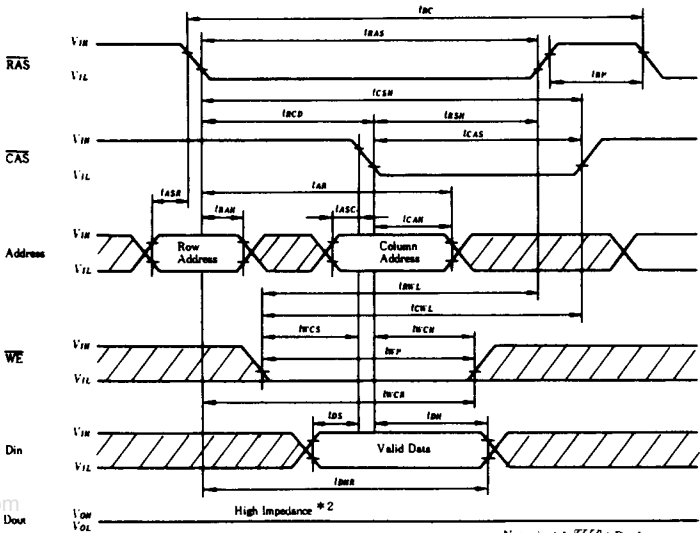
■ ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

( $T_a = 0$  to  $+70^\circ C$ ,  $V_{CC} = 5V \pm 10\%$ ,  $V_{SS} = 0V$ )<sup>1), 10), 11)</sup>

Parameter	Symbol	HM50256-12		HM50256-15		HM50256-20		Unit	Notes
		min	max	min	max	min	max		
Random Read or Write Cycle Time	$t_{RC}$	220	—	260	—	330	—	ns	
Read/Write Cycle Time	$t_{RWC}$	265	—	310	—	390	—	ns	
RAS to CAS Delay Time	$t_{RCD}$	25	60	25	75	30	100	ns	7
Access Time from RAS	$t_{RAC}$	—	120	—	150	—	200	ns	2, 3
Access Time from CAS	$t_{CAC}$	—	60	—	75	—	100	ns	3, 4
Output Buffer Turn-off Delay	$t_{OFF}$	—	30	—	40	—	50	ns	5
Transition Time (Rise and Fall)	$t_r$	3	50	3	50	3	50	ns	6
RAS Precharge Time	$t_{RP}$	90	—	100	—	120	—	ns	
RAS Pulse Width	$t_{RAS}$	120	10000	150	10000	200	10000	ns	
RAS Hold Time	$t_{RSH}$	60	—	75	—	100	—	ns	
CAS Hold Time	$t_{CSH}$	120	—	150	—	200	—	ns	
CAS Pulse Width	$t_{CAS}$	60	10000	75	10000	100	10000	ns	
CAS to RAS Precharge Time	$t_{CRP}$	10	—	10	—	10	—	ns	
Row Address Set-up Time	$t_{ASR}$	0	—	0	—	0	—	ns	
Row Address Hold Time	$t_{RAH}$	15	—	15	—	20	—	ns	
Column Address Set-up Time	$t_{ASC}$	0	—	0	—	0	—	ns	
Column Address Hold Time	$t_{CAH}$	20	—	25	—	30	—	ns	
Column Address Hold Time referenced to RAS	$t_{AR}$	80	—	100	—	130	—	ns	
Read Command Set-up Time	$t_{RCS}$	0	—	0	—	0	—	ns	
Read Command Hold Time referenced to CAS	$t_{RCH}$	0	—	0	—	0	—	ns	
Write Command Set-up Time	$t_{WCS}$	0	—	0	—	0	—	ns	8
Write Command Hold Time	$t_{WCH}$	40	—	45	—	55	—	ns	
Write Command Hold Time referenced to RAS	$t_{WCR}$	100	—	120	—	155	—	ns	
Write Command Pulse Width	$t_{WP}$	40	—	45	—	55	—	ns	
Write Command to RAS Lead Time	$t_{RWL}$	40	—	45	—	55	—	ns	
Write Command to CAS Lead Time	$t_{CWL}$	40	—	45	—	55	—	ns	
Data-in Set-up Time	$t_{DS}$	0	—	0	—	0	—	ns	9
Data-in Hold Time	$t_{DH}$	40	—	45	—	55	—	ns	8, 9
Data-in Hold Time referenced to RAS	$t_{DHR}$	100	—	120	—	155	—	ns	
RAS to WE Delay	$t_{RWD}$	120	—	150	—	200	—	ns	
CAS to WE Delay	$t_{CWD}$	60	—	75	—	100	—	ns	8
Page Mode Read or Write Cycle	$t_{PC}$	120	—	145	—	190	—	ns	
Page Mode Read Modify Write Cycle	$t_{PCM}$	165	—	195	—	250	—	ns	
CAS Precharge Time, Page Cycle	$t_{CP}$	50	—	60	—	80	—	ns	
Read Command Hold Time referenced to RAS	$t_{RRH}$	10	—	10	—	10	—	ns	
Refresh Period	$t_{REF}$	—	4	—	4	—	4	ms	
CAS Set-up Time	$t_{CSR}$	10	—	10	—	10	—	ns	
CAS Hold Time (CAS before RAS Refresh)	$t_{CHR}$	120	—	150	—	200	—	ns	
RAS Precharge to CAS Hold Time	$t_{RPC}$	0	—	0	—	0	—	ns	



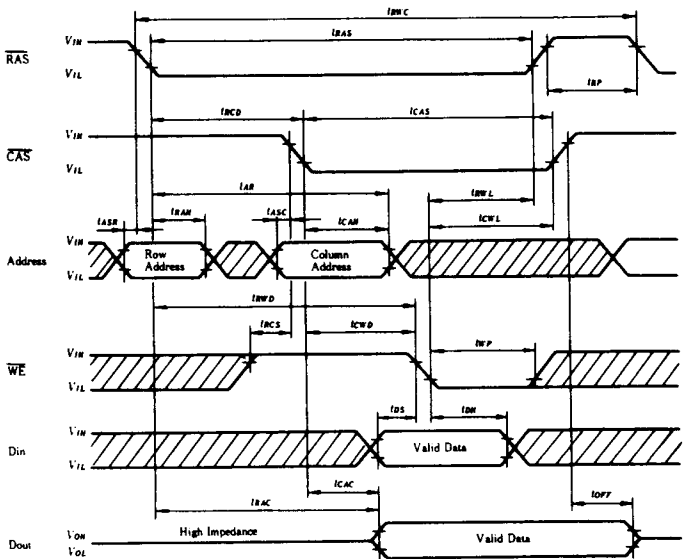
● WRITE CYCLE



Notes) \*1. [ZZ]: Don't care  
 \*2.  $t_{WCS} \geq t_{WCS}(\text{min})$

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● READ MODIFY WRITE CYCLE

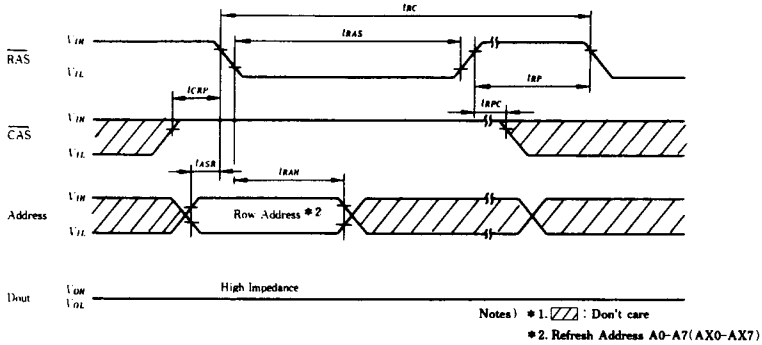


Notes) \*1. [ZZ]: Don't care  
 \*2.  $t_{AWO} \geq t_{AWP}(\text{min})$   
 $t_{CWP} \geq t_{CWP}(\text{min})$

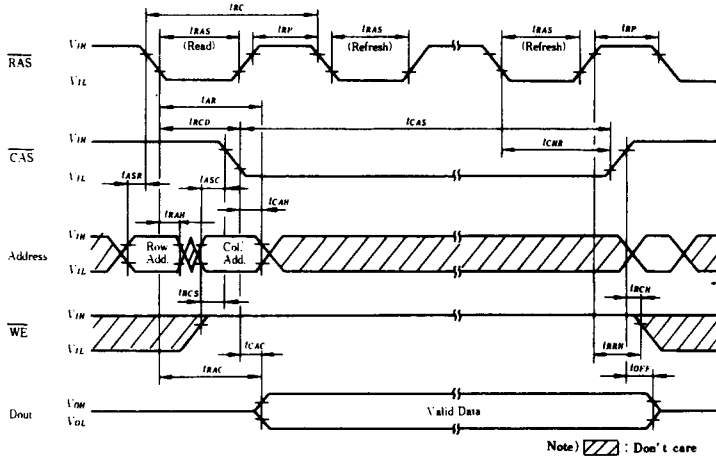
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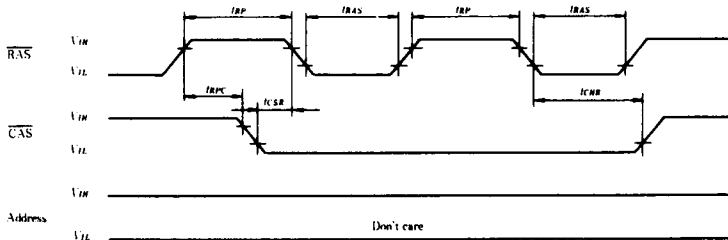
● **RAS ONLY REFRESH CYCLE**



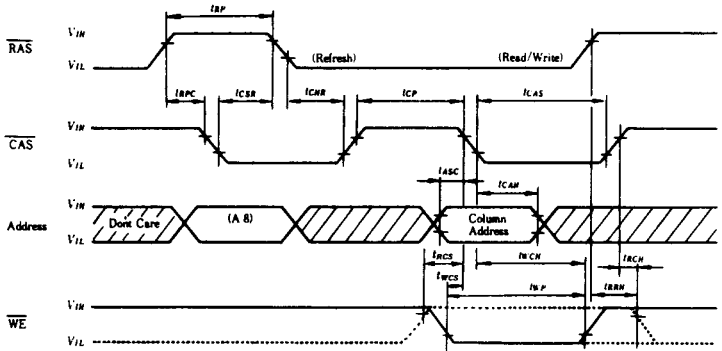
● **HIDDEN REFRESH CYCLE**



● **CAS BEFORE RAS REFRESH CYCLE**

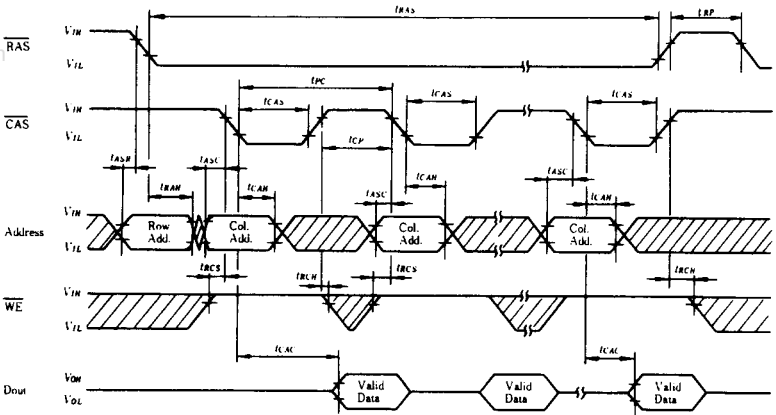


● COUNTER TEST



Notes) \*1. : Don't care  
\*2. Dotted Line Means Read Cycle.

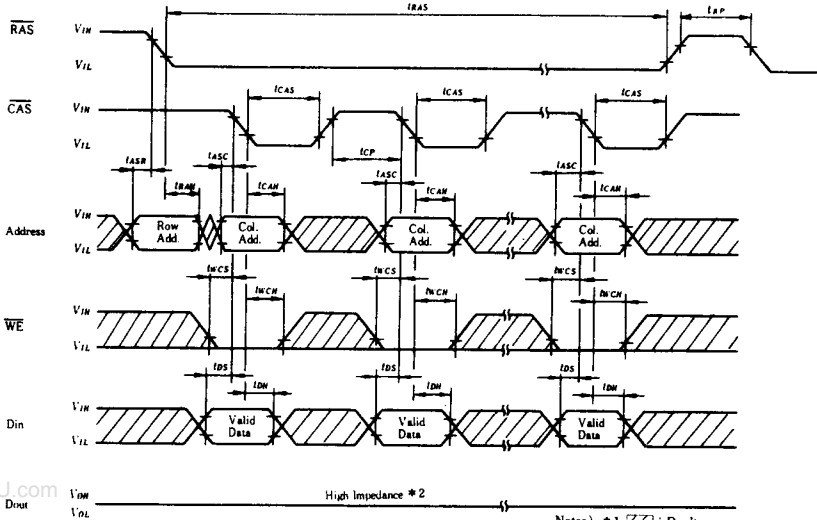
● PAGE MODE READ CYCLE



Note) : Don't care

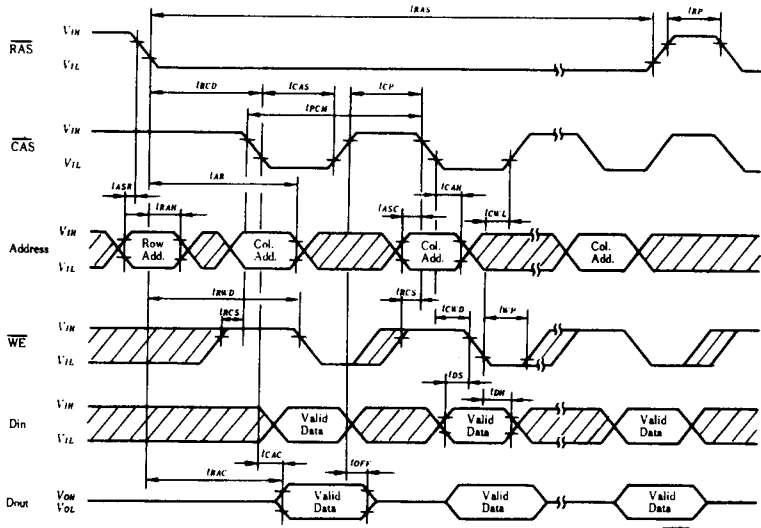
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● PAGE MODE WRITE CYCLE



Notes) \* 1.  $\text{Z}$ : Don't care  
 \* 2.  $t_{wcs} \approx t_{wcs}(\min)$

● PAGE MODE READ MODIFY WRITE CYCLE



Notes) \* 1.  $\text{Z}$ : Don't care  
 \* 2.  $t_{rwd} \approx t_{rwd}(\min)$   
 $t_{cwo} \approx t_{cwo}(\min)$

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