NEW PRODUCT

GTM415

FAX VOdem Controller with Built-in High Speed UART

1995.2

Overview

The Yamaha FAX VOdem Controller, GTM415, combines an 8031-software-compatible CPU core with a 16550 UART and autobaud circuitry in a single IC designed to operate in 5V, 3.3V, and mixed 3.3V/5V systems. The integration of the CPU, UART, glue logic, and the 3.3V operation in GTM415 provides a compact solution for low voltage and space sensitive applications such as palmtops and PCMCIA. GTM415 is an upgrade to the previous FAX VOdem Controller from Yamaha, GTM407, and is available in a standard 80-pin Quad Flat Pack (QFP) and an 80-pin, 1.4mm Thin Quad Flat Pack (TQFP).

Features and Benefits

The GTM415 IC is a companion controller chip for the Yamaha YTM403 Fax/Data VOdem. GTM415 runs the accompanying firmware and offers the following features:

- Internal Microcontroller runs all of the VOdemWare (8031 compatible firmware) that accompanies the chip. The VOdemWare runs out of an external EPROM and includes the following:
  - Hayes AT command set autodialer
  - V.42bis and MNP5 data compression
  - V.42 and MNP2-4 error correction.
  - TR29.2 Class 1, 2, and 2.0 AT command set extensions for FAX.
  - T.30 FAX handshake protocol
  - Voice record and playback
  - Voice, FAX, and DATA auto-switch.
  - Binary Final Transfer (BFT) TR29.1.
  - Group 3 FAX Error Correction Mode (ECM).
  - V.22bis handshake with fallback.
  - Embedded operating system and hooks for firmware customization. according to customers' specifications (i.e. Non-Standard Facilities, etc.)
  - DAA (NCU) control of the data pump (on/off-hook, ring status)

- Provides a complete 16-byte FIFO UART interface to the data pump.
- Saves on the required glue logic for the PC Bus.
- Provides 3 interface options for the user to save on the required glue logic for PC-Bus:
  - COM1, COM2, COM3, or COM4 interface from the PC Bus.
  - An RS232 type serial interface (TTL levels) for stand alone applications.
  - A parallel interface with 'chip select' (user selectable address)..
- Has built-in power down circuitry which saves the user the external power management hardware. If the power down mode is enabled on the chip, the chip will power down after it has not been accessed for 30 seconds. When the chip is powered down, it will not only power down the YTM403 , but any other external chips that need to be powered down as well. The modem is powered back up whenever it is either accessed by the host, DTR is asserted, or a ring signal is detected.
- Is capable of addressing external EPROM of 16K, 32k, 64K or 128K.
- Is capable of addressing external SRAM up to 124K bytes.
- Has an auxiliary on/off-hook and an on line detect bit (for European approval as well as certain Fax switch applications.)
- Stores user configuration through an external NVRAM serial interface.
- 2-bit speaker volume control and speaker enable/disable is compatible with the AT commands.
- Controls external peripherals through optional chip select logic.
- Contains autobaud detection hardware to enable autobauding at baud rates up to 38.4 Kbps with minimal software overhead.
- Enables flow control at high baud rates through fully programmable character detection/flow control hardware.

Upgrades to GTM407

- *3.3V operation* - GTM415 can run in 5.0V, 3.3V, and mixed 3.3V and 5.0V systems. In a mixed system, the GTM415 is powered by 3.3V. The following chart shows how other parts of the system may be powered in 5.0V, 3.3V and mixed operation.

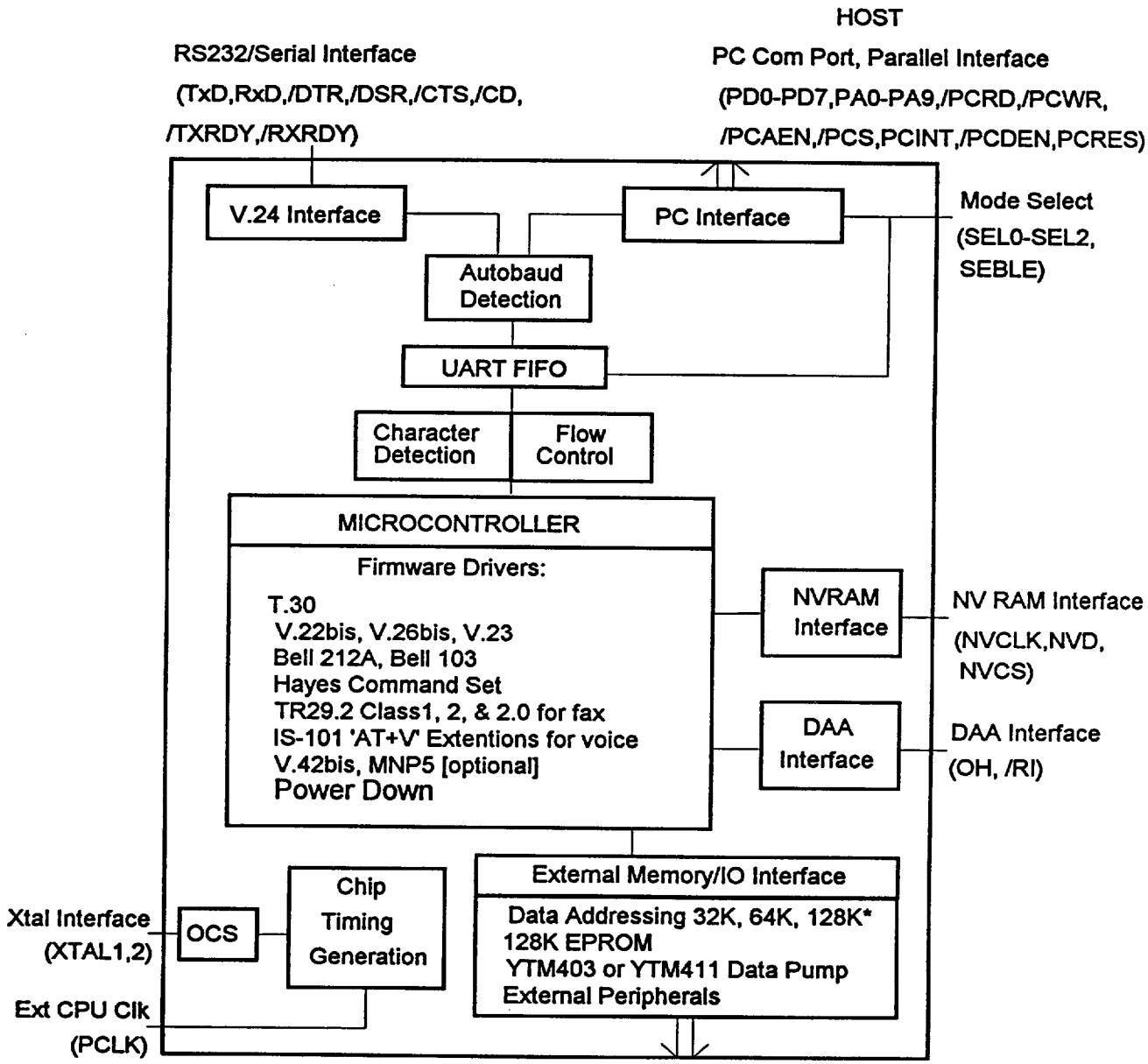
Function	+5V	+3.3V	Mixed
External Memory/IO	5V	3.3V	3.3V
DAA	5V	3.3V	3.3V
NVRAM	5V	3.3V	3.3V or 5.0V
Host	5V	3.3V	3.3V or 5.0V
RS232	5V	3.3V	3.3V or 5.0V

Typical power consumption for the GTM415 is 125 mW at 5V and 90 mW at 3.3V in active mode, and less than 3 mW in standby.

- *Higher speed operation for the CPU* - Pin 3 of the GTM415 has been assigned as PCLK, a clock for the 8051. If PCLK is left open, the 8051 clock generation will be the same as the previous GTM407. If PCLK is driven with a clock, it will be used to generate the 8051 clock. The GTM415 CPU can run at speeds as high as 20 MHz and 35 MHz.

- *Enhanced BAUD rate generator* - The BAUD rate generator in the GTM415 allows new BAUD rates compatible with the NEC standard. These rates will be selected by the BAUD Select Register which may be written to by the 8051. The register will be cleared when the chip is reset. When cleared, the GTM415 will generate BAUD rates that are compatible with the previous GTM407.

Internal Block Diagram



* 124K usable external RAM, 4K memory mapped IO space

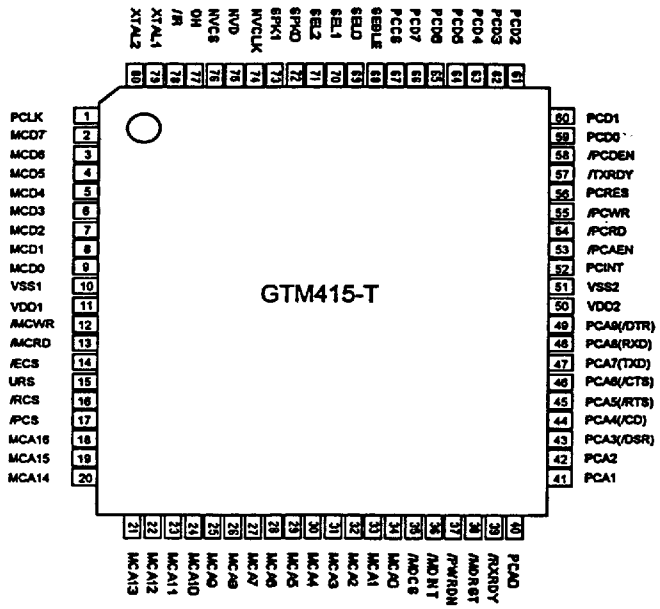
GTM415 Architecture

The basic high level building blocks of the chip consist of the following:

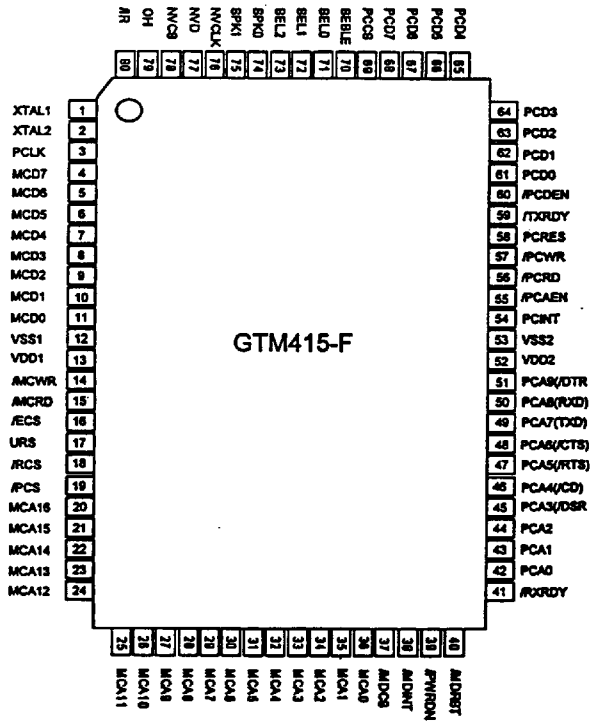
- **Microcontroller**. The chip runs at 14.7458 MHz. Address, data, and control lines on the chips IO so an external EPROM (8031 compatible firmware) and external RAM can be used with the chip.
- **16450 UART**. The 16450 is an industry standard UART used in PC type communication packages. This is a Mega Function part, and is 100% register compatible with a 16450 chip.
- **16 byte UART FIFO**. The 16550 is a FIFO version of the 16450. FIFOs are added to the data buffer area of the 16450. The FIFO circuitry works so that the chip is register compatible with the 16550 chip.
- The chip has 192 bytes of **Internal RAM** that can be accessed through the 8031 compatible microcontroller. Therefore the GTM415 has an extra 64 bytes but does not need the timer 2 of the 8031.
- **Microcontroller Glue Logic**. This includes the internal memory and external memory addressing capability. It also includes interfacing to the external YTM403 FAX VOdem data pump, the external NVRAM, and the internal 16450.
- **Clock Circuitry**. This includes the circuitry for an on-chip oscillator. This is accomplished through the addition of one external crystal. The clock circuitry provides the necessary clocks for the microcontroller, the UART, and the autobaud circuitry. In addition, an independent clock source can be supplied for the microcontroller via the PCLK pin.
- **Power Down Circuitry**. This circuitry detects a "power down", or 30 seconds of no activity and turns off the chip's clock. A "power on" condition is also detected and the chip is switched back on.
- **RS232 Interface**. This circuit consists of the RS232 interface to the 16550.
- **PC Interface**. This circuit has a full address decode of the PC bus going to either COM1, COM2, COM3, or COM4 register. This also includes a data interface and an interrupt line. In addition, the user can choose to have the address decode external to the chip.

Pin Configuration

(1) 80-pin Thin Quad Flat Pack



(2) 80-pin Quad Flat Pack



Function Assignment to Pins

Pin Name	Pin No. QFP	Pin No. TQFP	Type	Function
XTAL1	1	79	XI	Crystal In
XTAL2	2	80	XO	Crystal Out
PCLK	3	1	DIP	Processor Clock Input
MCD7	4	2	DIO2	Microcontroller Data Bus
MCD6	5	3	DIO2	Microcontroller Data Bus
MCD5	6	4	DIO2	Microcontroller Data Bus
MCD4	7	5	DIO2	Microcontroller Data Bus
MCD3	8	6	DIO2	Microcontroller Data Bus
MCD2	9	7	DIO2	Microcontroller Data Bus
MCD1	10	8	DIO2	Microcontroller Data Bus
MCD0	11	9	DIO2	Microcontroller Data Bus
VSS1	12	10	GND	Digital Ground
VDD1	13	11	PWR	Digital +5V or +3.3V source
/MCWR	14	12	DO	Microcontroller Write
/MCRD	15	13	DO	Microcontroller Read
/ECS	16	14	DO	EPROM Chip Select
URS	17	15	DO	Upper RAM Select
/RCS	18	16	DO	SRAM Chip Select
/PCS	19	17	DO	Peripheral Chip Select
MCA16	20	18	DO	Microcontroller Address Bus
MCA15	21	19	DO	Microcontroller Address Bus
MCA14	22	20	DO	Microcontroller Address Bus
MCA13	23	21	DO	Microcontroller Address Bus
MCA12	24	22	DO	Microcontroller Address Bus
MCA11	25	23	DO	Microcontroller Address Bus
MCA10	26	24	DO	Microcontroller Address Bus
MCA9	27	25	DO	Microcontroller Address Bus
MCA8	28	26	DO	Microcontroller Address Bus
MCA7	29	27	DO	Microcontroller Address Bus
MCA6	30	28	DO	Microcontroller Address Bus
MCA5	31	29	DO	Microcontroller Address Bus
MCA4	32	30	DO	Microcontroller Address Bus
MCA3	33	31	DO	Microcontroller Address Bus
MCA2	34	32	DO	Microcontroller Address Bus
MCA1	35	33	DO	Microcontroller Address Bus
MCA0	36	34	DO	Microcontroller Address Bus
/MDCS	37	35	DO	Modem Chip Select
/MDINT	38	36	DIP	Modem Interrupt
/PWRDN	39	37	DO	Power Down
/MDRST	40	38	DO	Modem (Data Pump) Reset
/RXRDY	41	39	D0	Receive Ready (16550)
PCA0	42	40	DIP	Parallel Interface Address
PCA1	43	41	DIP	Parallel Interface Address
PCA2	44	42	DIP	Parallel Interface Address
PCA3	45	43	DIO1	Parallel Interface Address (DI)
/DSR				Data Set Ready (DO)
PCA4	46	44	DI01	Parallel Interface Address (DI)

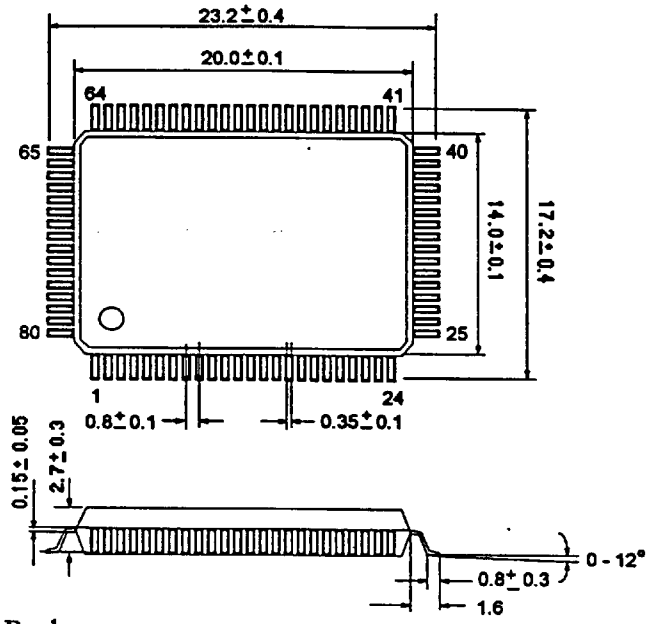
/CD				Data Carrier Detected (DO)
PCA5	47	45	DI	Parallel Interface Address
/RTS				Request To Send
PCA6	48	46	DIO1	Parallel Interface Address (DI)
/CTS				Clear To Send (DO)
PCA7	49	47	DI	Parallel Interface Address
TXD				Transmit Data
PCA8	50	48	DIO1	Parallel Interface Address (DI)
RXD				Receive Data (DO)
PCA9	51	49	DI	Parallel Interface Address
/DTR				Data Terminal Ready
VDD2	52	50	PWR	Digital +5V or +3.3V source
VSS2	53	51	GND	Digital Ground
PCINT	54	52	DO	Parallel Interrupt
/PCAEN	55	53	DIP	PC Access Enable
/PCRD	56	54	DIP	Parallel Read
/PCWR	57	55	DIP	Parallel Write
PCRES	58	56	DIS	PC Reset
/TXRDY	59	57	DO	Transmit Ready (16550)
/PCDEN	60	58	DO	PC data enable
PCD0	61	59	DIO2	Parallel Interface Data
PCD1	62	60	DIO2	Parallel Interface Data
PCD2	63	61	DIO2	Parallel Interface Data
PCD3	64	62	DIO2	Parallel Interface Data
PCD4	65	63	DIO2	Parallel Interface Data
PCD5	66	64	DIO2	Parallel Interface Data
PCD6	67	65	DIO2	Parallel Interface Data
PCD7	68	66	DIO2	Parallel Interface Data
/PCCS	69	67	DIP	Parallel Chip Select
SEBLE	70	68	DI	Serial Mode Select
SEL0	71	69	DI	Interface Mode Selection
SEL1	72	70	DI	Interface Mode Selection
SEL2	73	71	DI	Interface Mode Selection
SPK0	74	72	DO	Speaker Control, general purpose output
SPK1	75	73	DO	Speaker Control, general purpose output
NVCLK	76	74	DO	NVRAM Clock
NVD	77	75	DIO2	NVRAM Data
NVCS	78	76	DO	NVRAM Chip Select
OH	79	77	DO	Off-hook control, general purpose IO
/RI	80	78	DI	Ring Detect, general purpose IO

Type symbols:

DI	Digital input (TTL)
DIS	Digital input (Schmitt)
DO	Digital output
DIP	Pull-up resistor Incorporated digital input
DIO1	Digital input/output
DIO2	Digital input/output
PWR	Power supply
GND	Ground
XI, XO	Crystal oscillator connection

Package Drawing

(1) 80-pin Thin Quad Flat Pack



(2) 80-pin Quad Flat Pack

1=1mm