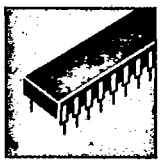


GS81 MPA PRELIMINARY

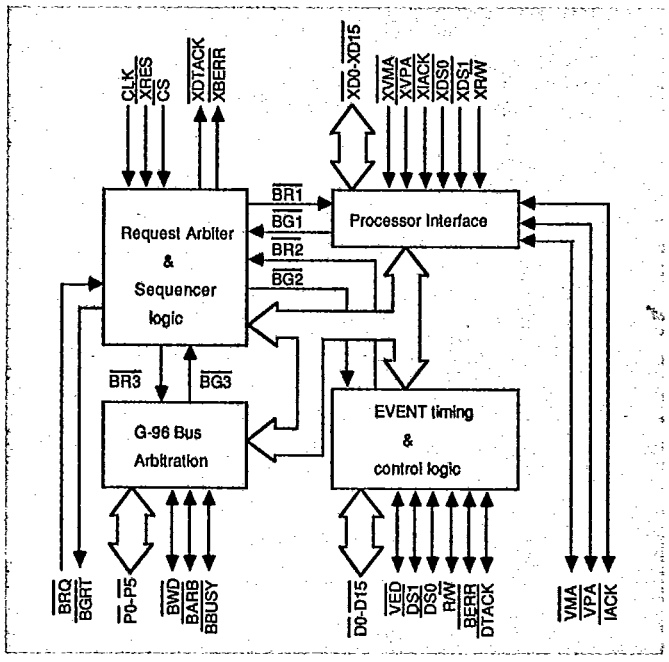
GESPAC MULTIPROCESSOR ARBITRATOR

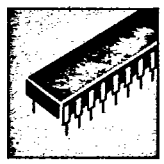
For multiprocessor support, the G-96 bus implements a fully asynchronous, decentralized parallel arbitration scheme. This simple but powerful architecture uses 9 lines for controlling the access to the bus by up to 31 masters. Each board contains the GS81 MPA arbitration circuit, thus making a G-96 system much more fault tolerant than an equivalent system based on a centralized architecture.

The multiprocessing specification of the G-64 bus supports a very efficient message passing mechanism. These messages, called «events», allow fast communication between masters as well as interrupts between peripherals and masters on the bus. All the protocol of message passing are handled by the GS81 MPA.

The priority level is directly selected by jumpers on each processor module, and the priority is independant of the position in the backplane. The priority level can be set also by software, thus allowing a master to dynamically change its priority level to gain control of the bus. These priority levels are managed through 6 priority bus lines on the GS81 MPA chips.

The bus arbitration cycle is totally transparent to the microprocessor on the master module.





GS64 SMC 1

T-52-33-55

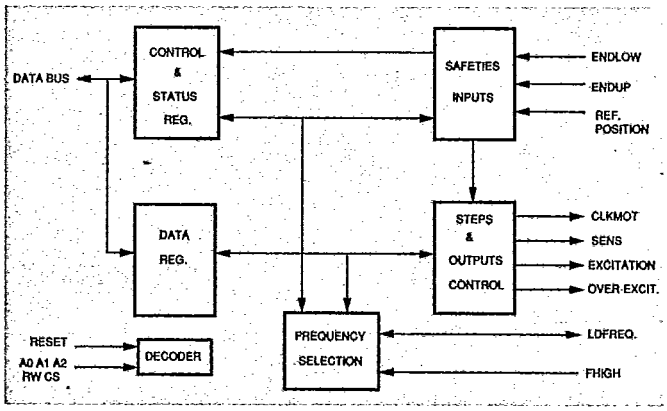
8-BIT STEPPER MOTOR CONTROLLER INTERFACE

The GS64 SMC 1 interface is a complete device capable of generating clock, direction, excitation and over-excitation to drive a power translator for stepper motor. In addition, this component can manage end-high/end-low limit switches and a home position reference to allow homing sequence and safety control.

T-52-13-25

Technical features

- High frequency input: Up to 4 Mhz
- Base frequency Input/Output: Programmable Frequency
- Five programmable Control Registers and one Status Register
- 8-Bit Internal Data Bus for steps generation
- Two limit switch inputs for safety control
- One reference position input for home sequence
- Step rate up to 2 Mhz (micro-step application)
- Excitation and over excitation outputs
- TTL-Compatible



Reference
GS81 MPA: Gespac Multiprocessor Arbitrator

Reference
GS64 SMC 1: Stepper motor controller interface
PLCC package