2.2W Stereo Audio Amplifier

Features

- **Depop Circuitry Integrated**
- **Output Power at 10% THD+N, VDD=5V**
  --2.2W/CH (typical) into a 4Ω Load
- **Output Power at 1% THD+N, VDD=5V**
  --2W/CH (typical) into a 4Ω Load
  --1.2W/CH (typical) into a 8Ω Load
- **Bridge-Tied Load (BTL)**
- **Shutdown Control Available**
- **Thermal protection**
- **Surface-Mount Power Package**
  20-Pin TSSOP-P

General Description

The G1426 is a stereo audio power amplifier in 20pin TSSOP package. It can deliver 2W continuous RMS power into 4Ω load per channel in Bridge-Tied Load (BTL) mode at 5V supply voltage under 1% THD. To simplify the audio system design in the notebook application, The G1426 supports the Bridge-Tied Load (BTL) mode for driving the speakers. For the low current consumption applications, the SHDN mode is supported to disable the G1426 when it is idle. The current consumption can be further reduced to below 2μA.

Applications

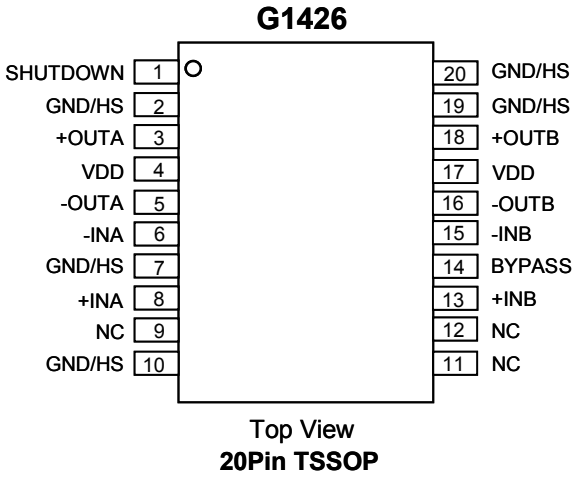
- **Stereo Power Amplifiers for Notebooks or Desktop Computers**
- **Multimedia Monitors**
- **Stereo Power Amplifiers for Portable Audio Systems**

Ordering Information

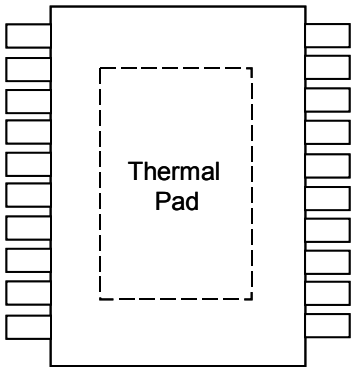
ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE
G1426D5X	G1426	-40°C to +85°C	TSSOP-20L
G1426F2X	G1426	-40°C to +85°C	TSSOP-20L (FD)

Note: X Specify the packing type
U: Tape & Reel T: Tube
* TSSOP-20L (FD): Thermal Pad

Pin Configuration



Top View
20Pin TSSOP



Bottom View

Absolute Maximum Ratings

Supply Voltage, V_{CC}.....6V
Operating Ambient Temperature Range
T_A.....-40°C to +85°C
Maximum Junction Temperature, T_J.....150°C
Storage Temperature Range, T_{STG}.....-65°C to+150°C
Soldering Temperature, 10seconds, T_S.....260°C

Power Dissipation [1]
$T_A \le 25°C$.....2.7W
$T_A \le 70°C$.....1.7W
$T_A \le 85°C$.....1.4W
Electrostatic Discharge, V_{ESD}
Human body mode.....-3000 to 3000[2]

Note:
[1]: Recommended PCB Layout
[2]: Human body model : C = 100pF, R = 1500Ω, 3 positive pulses plus 3 negative pulses

Electrical Characteristics

DC Electrical Characteristics, V_{DD} = 5.0V, T_A=+25°C, unless otherwise noted

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Supply Current	I_{DD}	V_{DD} = 5V	-	8.5	15	mA
DC Differential Output Voltage	$V_{O(DIFF)}$	V_{DD} = 5V,Gain = 2	-	5	50	mV
I_{DD} in Shutdown	I_{SD}	V_{DD} = 5V	-	0.1	2	μA

(AC Operation Characteristics, V_{DD} = 5.0V, T_A=+25°C, R_L = 4Ω, unless otherwise noted)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Output power (each channel) see Note	$P_{(OUT)}$	THD = 1%, BTL, R_L = 4Ω	-	2	-	W
		THD = 1%, BTL, R_L = 8Ω	-	1.25	-	
		THD = 10%, BTL, R_L = 4Ω	-	2.5	-	
		THD = 10%, BTL, R_L = 8Ω	-	1.6	-	
Total harmonic distortion plus noise	THD+N	P_O = 1.6W, BTL, R_L = 4Ω	-	300	-	m%
		P_O = 1W, BTL, R_L = 8Ω	-	100	-	
		V_I = 1V, RL = 10KΩ, G = 1	-	10	-	
Maximum output power bandwidth	B_{OM}	G = 10, THD = 1%	-	20	-	kHz
Phase margin		R_L = 4Ω, Open Load	-	65	-	°
Power supply ripple rejection	PSRR	f = 120Hz	-	75	-	dB
Channel-to-channel output separation		f = 1kHz	-	80	-	dB
Input impedance	ZI		-	2	-	MΩ
Signal-to-noise ratio		P_O = 500mW, BTL	-	90	-	dB
Output noise voltage	V_n	Output noise voltage	-	55	-	μV (rms)

Note :Output power is measured at the output terminals of the IC at 1kHz.

Pin Description

PIN	NAME	I/O	FUNCTION
1	SHUTDOWN	I	Shutdown mode control signal input, places entire IC in shutdown mode when held high, I_{DD} is below 2μA.
2,7,10,19,20	GND/HS		Ground connection for circuitry, directly connected to thermal pad.
3	+OUTA	O	A channel + output
4,17	VDD		Supply voltage for circuitry.
5	-OUTA	O	A channel - output
6	-INA	I	A channel input signal
8	+INA	I	A channel positive input of OPAMP, biasing DC operation of OPAMP
9	NC	I	NC
11	NC	I	NC
12	NC		NC
13	+INB	I	B channel positive input of OPAMP, biasing DC operation of OPAMP
14	BYPASS		Connect to voltage divider for internal mid-supply bias.
15	-INB	I	B channel input signal
16	-OUTB	O	B channel - output
18	+OUTB	O	B channel + output

Typical Characteristics

Table of Graphs

		FIGURE
THD +N Total harmonic distortion plus noise	vs Frequency	2,4,6,9,11
	vs Output power	1,3,5,7,8,10
V_n Output noise voltage	vs Frequency	13
Supply ripple rejection ratio	vs Frequency	12
Crosstalk	vs Frequency	14
Closed loop response	vs Frequency	17
I_{DD} Supply current	vs supply voltage	15
P_O Output power	vs supply voltage	16
	vs Load resistance	18
P_D Power dissipation	vs Output power	19,20

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

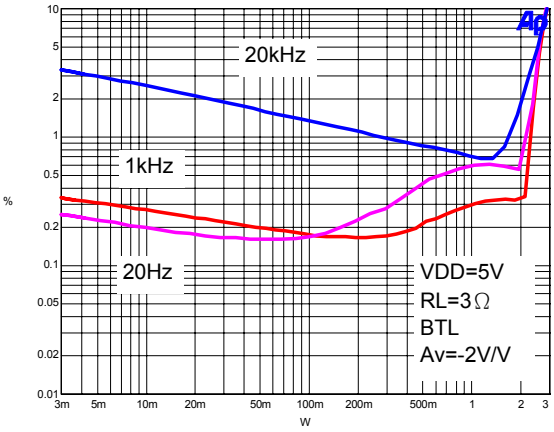


Figure 1

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

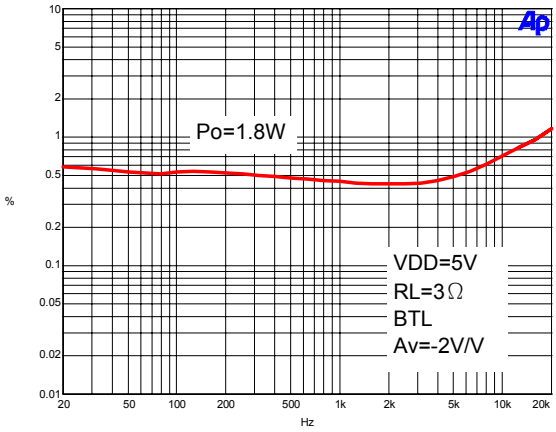


Figure 2

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

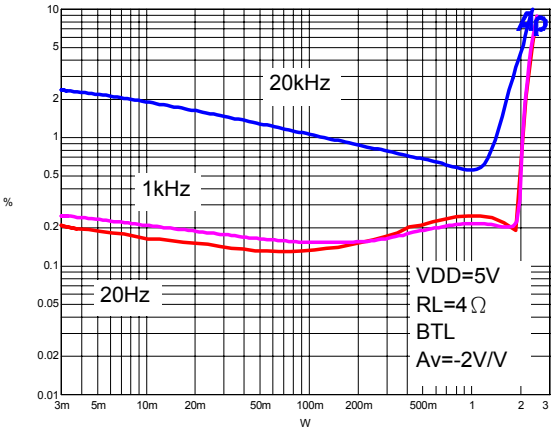


Figure 3

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

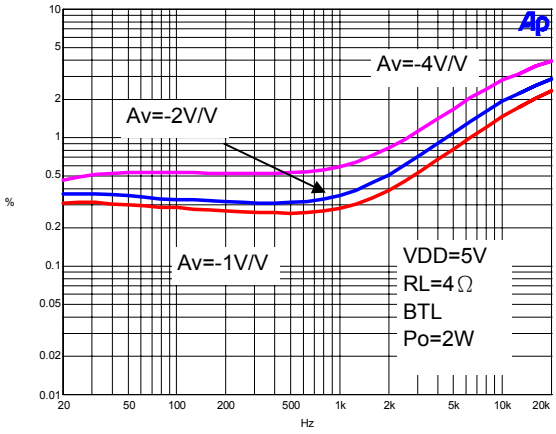


Figure 4

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

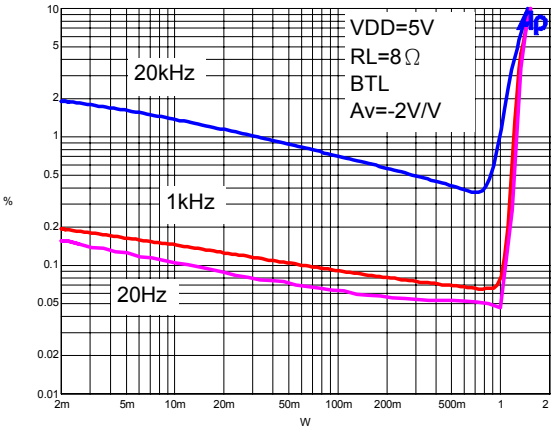


Figure 5

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

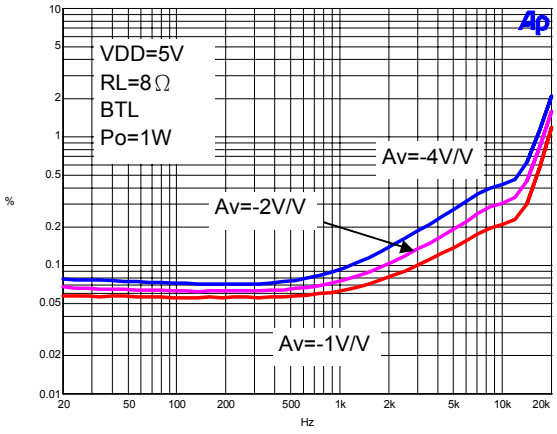


Figure 6

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

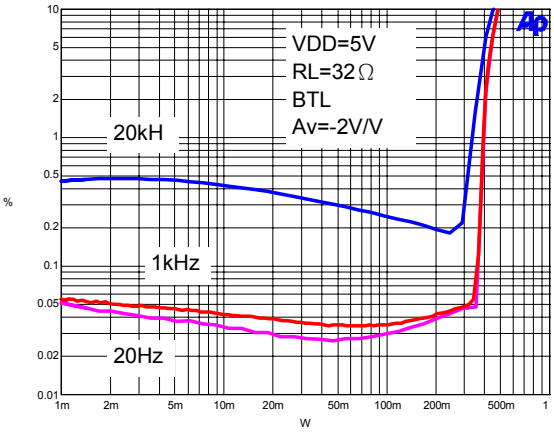


Figure 7

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

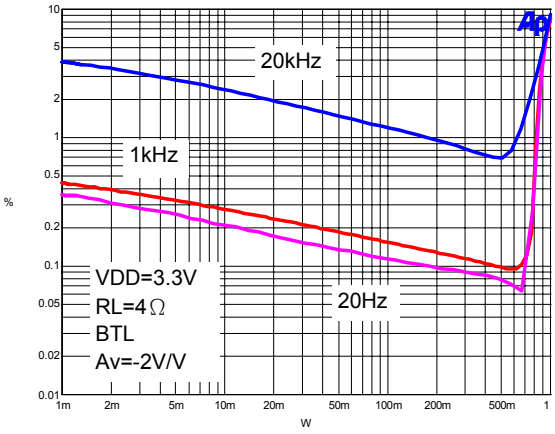


Figure 8

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

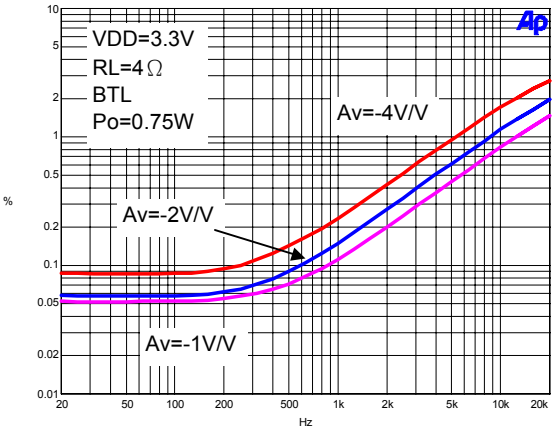


Figure 9

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

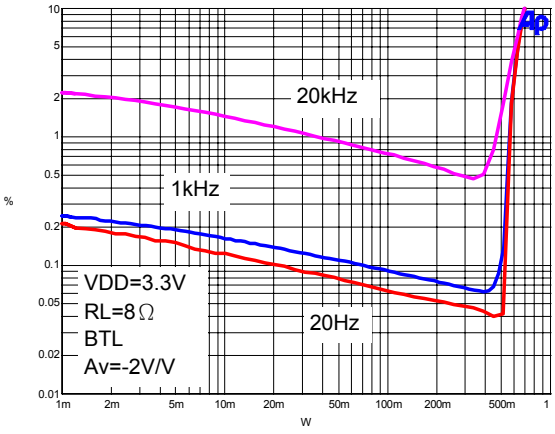


Figure 10

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

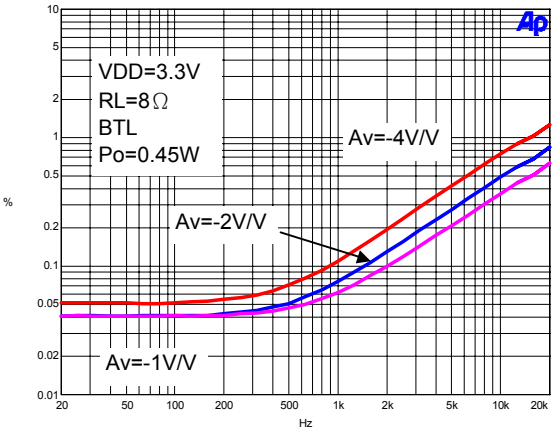


Figure 11

SUPPLY RIPPLE REJECTION RATIO vs FREQUENCY

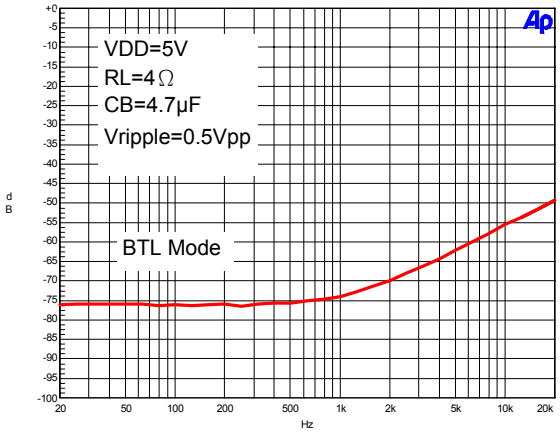


Figure 12

OUTPUT NOISE VOLTAGE vs FREQUENCY

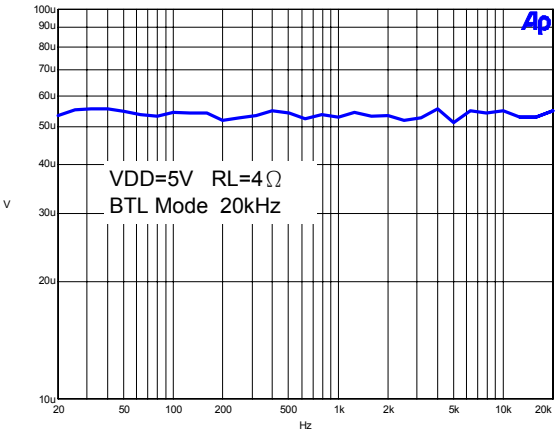


Figure 13

CHANNEL SEPARATION

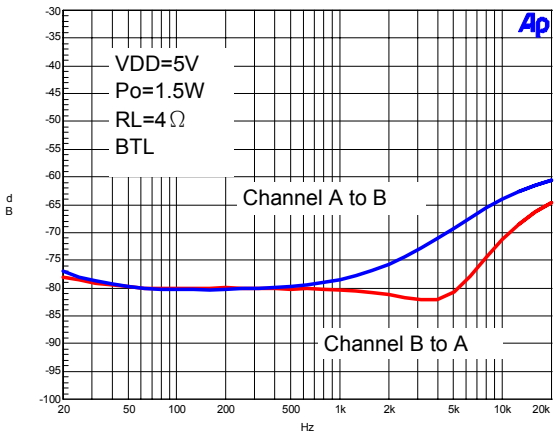


Figure 14

SUPPLY CURRENT vs SUPPLY VOLTAGE

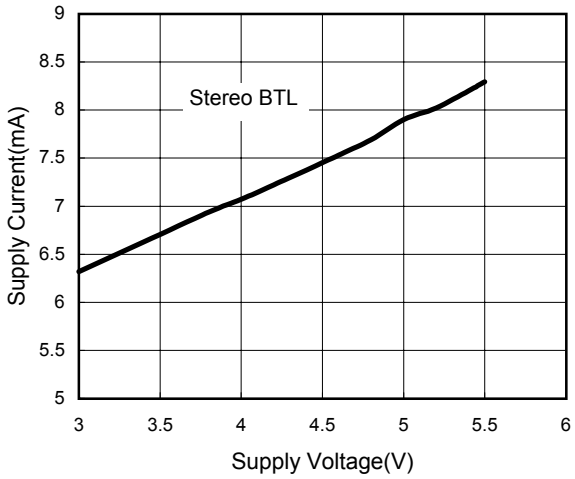


Figure 15

OUTPUT POWER vs SUPPLY VOLTAGE

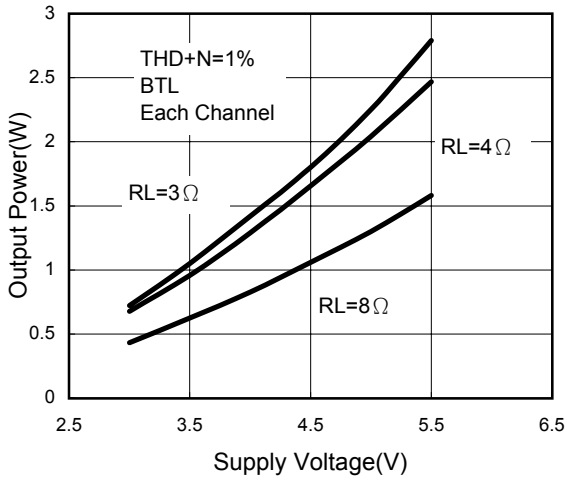


Figure 16

OPEN LOOP RESPONSE

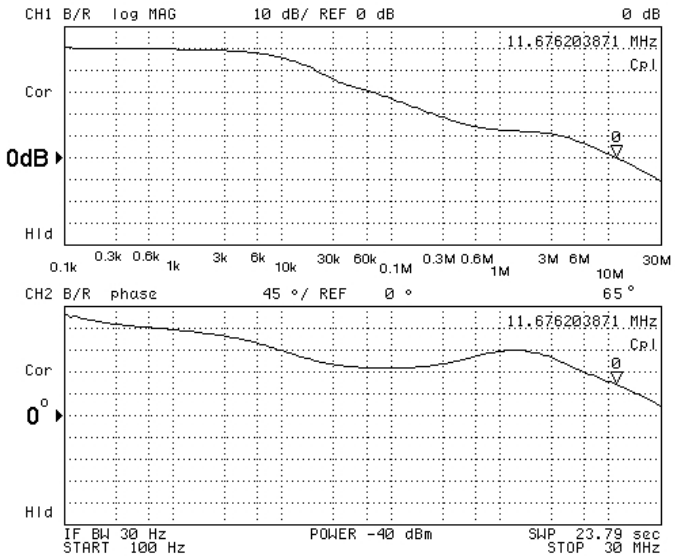


Figure 17

OUTPUT POWER vs LOAD RESISTANCE

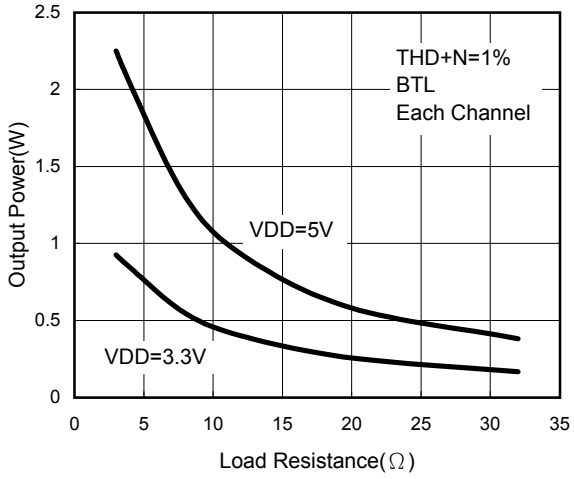


Figure 18

POWER DISSIPATION vs OUTPUT POWER

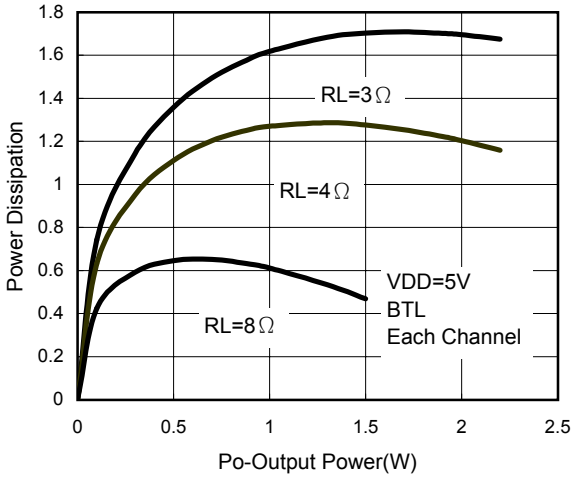


Figure 19

POWER DISSIPATION vs OUTPUT POWER

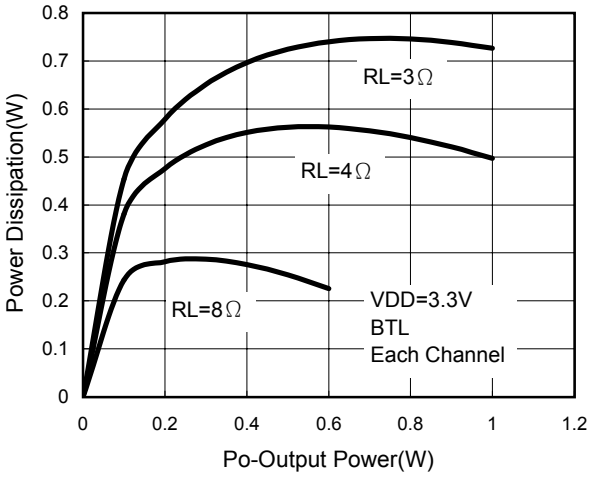
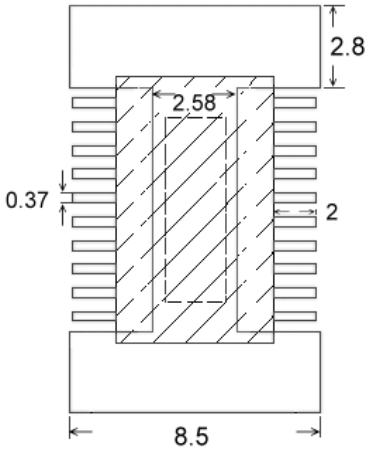
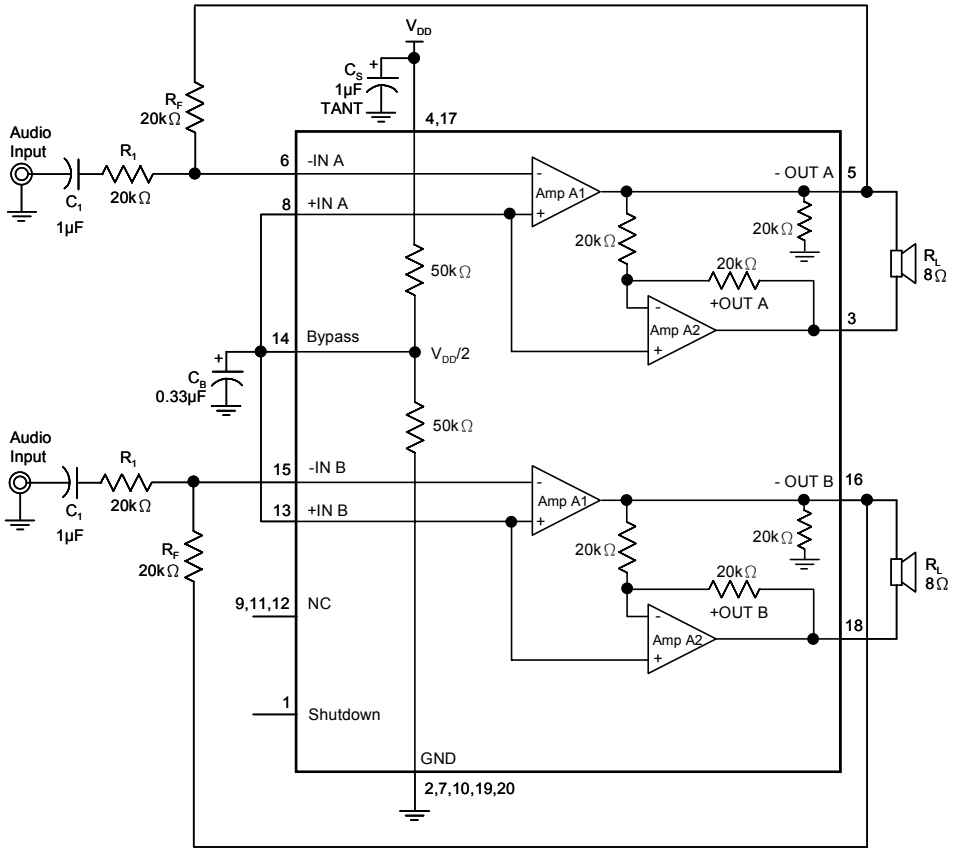


Figure 20

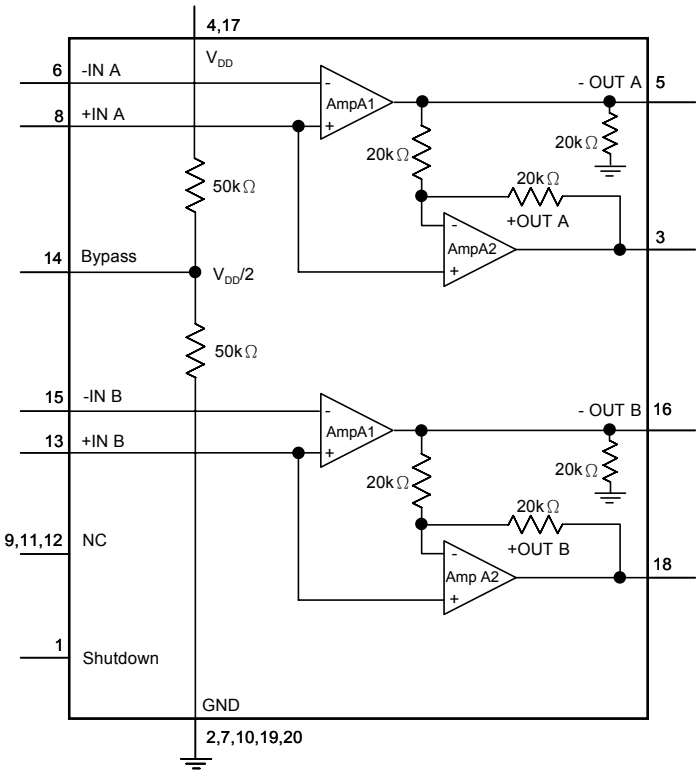
Recommended PCB Layout
Unit:mm



Block Diagram



Application Circuits



Application Information

Bridged-Tied Load Mode Operation

G1426 has two linear amplifiers to drive both ends of the speaker load in Bridged-Tied Load (BTL) mode operation. Figure 1 shows the BTL configuration. The differential driving to the speaker load means that when one side is slewing up, the other side is slewing down, and vice versa. This configuration in effect will double the voltage swing on the load as compared to a ground reference load. In BTL mode, the peak-to-peak voltage V_O(PP) on the load will be two times than a ground reference configuration. The voltage on the load is doubled, this will also yield 4 times output power on the load at the same power supply rail and loading. Another benefit of using differential driving configuration is that BTL operation cancels the dc offsets, which eliminates the dc coupling capacitor that is needed to cancelled dc offsets in the ground reference configuration. Low-frequency performance is then limited only by the input network and speaker responses. Cost and PCB space can be minimized by eliminating the dc coupling capacitors.

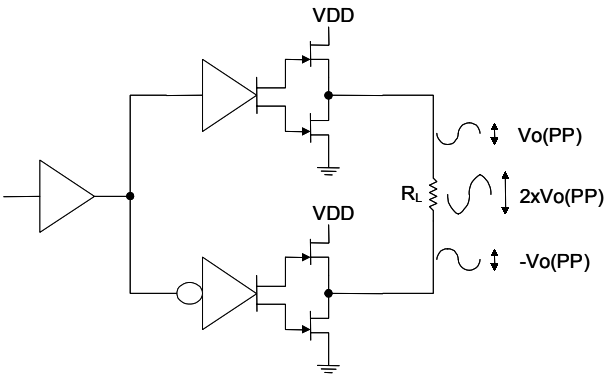


Figure 1

SHUTDOWN Mode Operations

G1426 implements the shutdown mode operations to reduce supply current, $I_{DD,}$ to the absolute minimum level during nonuse periods for battery-power conservation. When the shutdown pin (pin 1) is pulled high, all linear amplifiers will be deactivated to mute the amplifier outputs. And G1426 enters an extra low current consumption state, I_{DD} is smaller than 2μA. Shutdown pin should never be left unconnected, this floating condition will cause the amplifier operations unpredictable.

Optimizing DEPOP Operation

Circuitry has been implemented in G1426 to minimize the amount of popping heard at power-up and when coming out of shutdown mode. Popping occurs whenever a voltage step is applied to the speaker and making the differential voltage generated at the two ends of the speaker. To avoid the popping heard, the bypass capacitor should be chosen promptly, $1/(C_B x 100k\Omega) \leqq 1/(C_I*(R_I+R_F))$. Where 100kΩ is the output impedance of the mid-rail generator, C_B is the mid-rail bypass capacitor, C_I is the input coupling capacitor, R_I is the input impedance, R_F is the gain setting impedance which is on the feedback path. C_B is the most important capacitor. Besides it is used to reduce the popping, C_B can also determine the rate at which the amplifier starts up during startup or recovery from shutdown mode.

De-popping circuitry of G1426 is shown on Figure 2. The PNP transistor limits the voltage drop across the 225kΩ by slewing the internal node slowly when power is applied. At start-up, the voltage at BYPASS capacitor is 0. The PNP is ON to pull the mid-point of the bias circuit down. So the capacitor sees a lower effective voltage, and thus the charging is slower. This appears as a linear ramp (while the PNP transistor is conducting), followed by the expected exponential ramp of an R-C circuit.

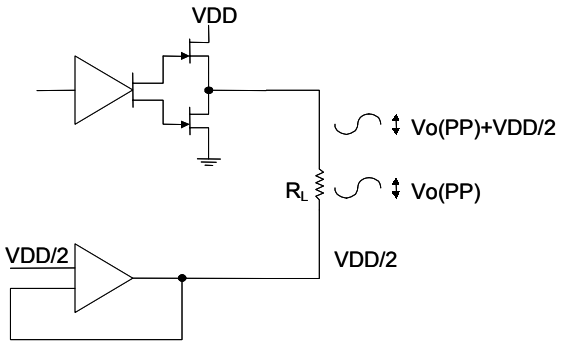
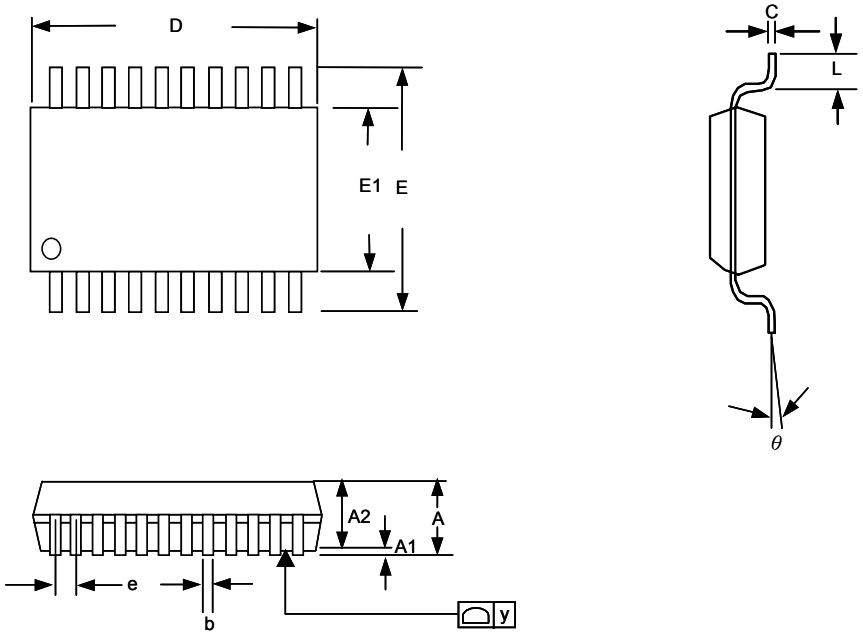


Figure 2

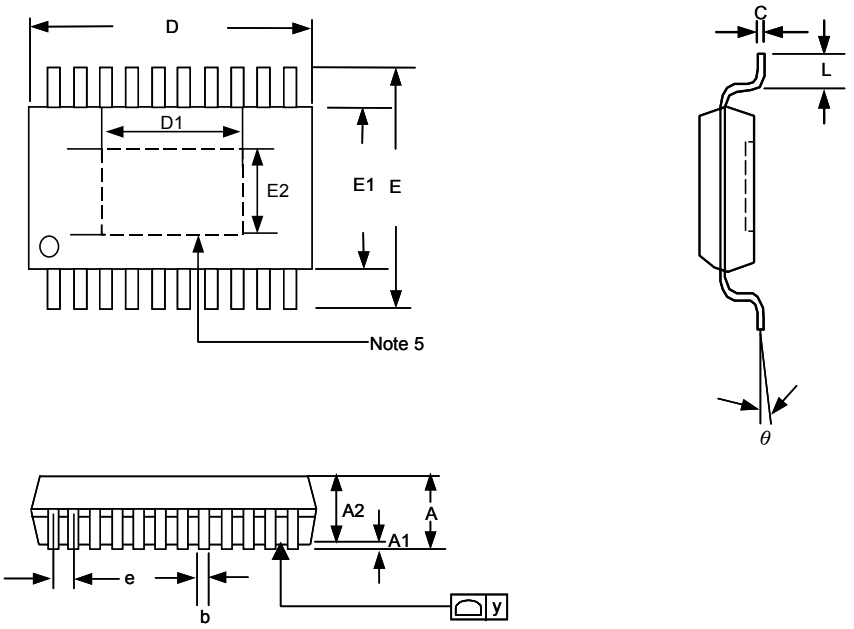
Package Information



TSSOP-20L Package

NOTE:
1. Package body sizes exclude mold flash protrusions or gate burrs
2. Tolerance ±0.1mm unless otherwise specified
3. Coplanarity : 0.1mm
4. Controlling dimension is millimeter. Converted inch dimensions are not necessarily exact.
5. Follow JEDEC MO-153

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	-----	-----	1.20	-----	-----	0.048
A1	0.05	-----	0.15	0.002	-----	0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19	-----	0.30	0.007	-----	0.012
C	0.09	-----	0.20	0.004	-----	0.008
D	6.40	6.50	6.60	0.252	0.256	0.260
E	-----	6.40	-----	-----	0.252	-----
E1	4.30	4.40	4.50	0.169	0.173	0.177
e	-----	0.65	-----	-----	0.026	-----
L	0.45	0.60	0.75	0.018	0.024	0.030
y	-----	-----	0.10	-----	-----	0.004
θ	0°	-----	8°	0°	-----	8°



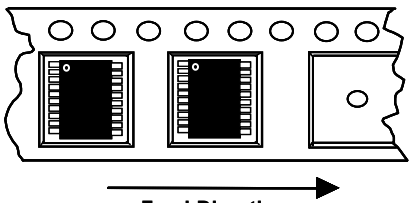
TSSOP-20L (FD) Package

NOTE:

1. Package body sizes exclude mold flash protrusions or gate burrs
2. Tolerance ±0.1mm unless otherwise specified
3. Coplanarity : 0.1mm
4. Controlling dimension is millimeter. Converted inch dimensions are not necessarily exact.
5. Die pad exposure size is according to lead frame design.
6. Follow JEDEC MO-153

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	-----	1.15	0.031	-----	0.045
A1	0.00	-----	0.10	0.000	-----	0.004
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19	-----	0.30	0.007	-----	0.012
C	0.09	-----	0.20	0.004	-----	0.008
D	6.40	6.50	6.60	0.252	0.256	0.260
E	-----	6.40	-----	-----	0.252	-----
E1	4.30	4.40	4.50	0.169	0.173	0.177
e	-----	0.65	-----	-----	0.026	-----
L	0.45	0.60	0.75	0.018	0.024	0.030
y	-----	-----	0.10	-----	-----	0.004
θ	0°	-----	8°	0°	-----	8°
D1	3.90	-----	4.28	0.153	-----	0.168
E2	2.30	-----	2.78	0.091	-----	0.109

Taping Specification



Feed Direction

Typical TSSOP Package Orientation