Edge211
Dual Pin
Electronics Driver

HIGH-PERFORMANCE PRODUCTS – ATE

Description

The Edge211 is a dual trinary driver manufactured in a wide voltage CMOS process. It is designed for automatic test equipment and instrumentation where cost, functional density, and power are all at a premium.

Each tristatable driver is capable of generating 3 levels - one for a logic high, one for a logic low, and one for either a termination voltage or a special programming voltage.

The Edge211 is intended to offer an extremely low leakage, low cost, low power, small footprint, driver solution for 100 MHz and below pin electronics applications.

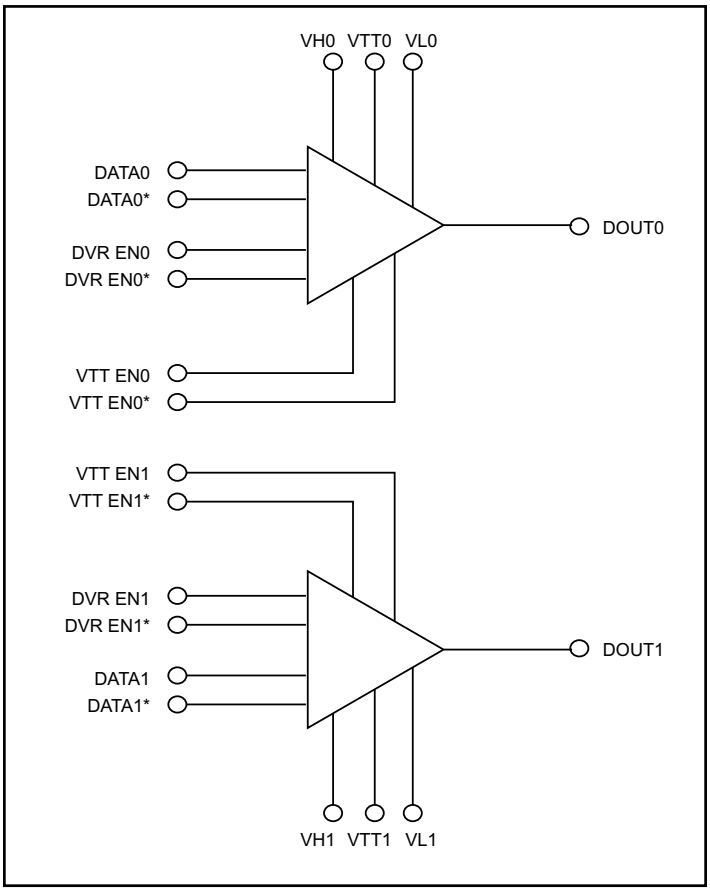
Features

- 100 MHz Operation
- 12V I/O Range
- Programmable Output Levels
- Flex In digital Inputs (Technology Independent)
- Three Level Driver
- Extremely Low Leakage Currents (~0 nA)
- Small Footprint (32 Pin, 7 mm X 7 mm, TQFP Package)

Applications

- Low Cost Automatic Test Equipment

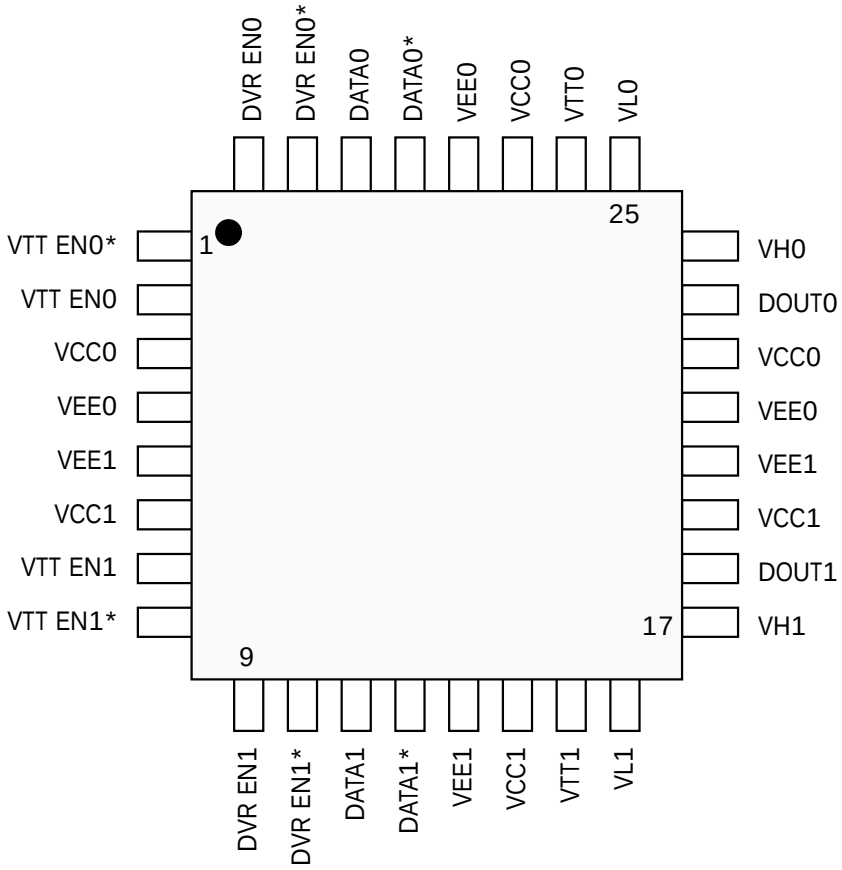
Functional Block Diagram



PIN Description

Pin Name	Pin *	Description
DATA0 / DATA0* DATA1 / DATA1*	30, 29 11, 12	Digital input that determines the high/low status of the driver when it is enabled.
DVR EN0 / DVR EN0* DVR EN1 / DVR EN1*	32, 31 9, 10	Digital input that enables and disables the driver, or places the driver in the VTT state.
VTT EN0 / VTT EN0* VTT EN1 / VTT EN1*	2, 1 7, 8	Digital input that determines whether DVR EN* places the driver in a high impedance state or actively drives to the VTT level.
DOUT0 DOUT1	23 18	Driver output.
VH0, VH1 VL0, VL1 VTT0, VTT1	24, 17 25, 16 26, 15	Unbuffered analog inputs that set the voltage level of a logical 1, 0, or VTT at the driver output.
Power Supplies		
VCC0 VCC1	3, 22, 27 6, 14, 19	Positive analog power supply.
VEE0 VEE1	4, 21, 28 5, 13, 20	Negative analog power supply.

PIN Description *(continued)*



32 Pin, 7 mm X 7 mm,
TQFP Package

Circuit Description

Driver Description

The Edge211 supports three distinct programmable driver levels – high, low, and termination, along with high impedance. There are no restrictions between any of these three levels in that all three may vary independently over the entire operating voltage range between VCC and VEE.

Digital Inputs

All digital inputs are wide voltage comparator inputs, and are therefore technology independent. The Edge211 may be driven by TTL, ECL, CMOS, or any custom level circuitry.

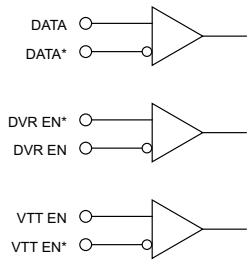


Figure 1. Driver Digital Inputs

Do NOT leave any driver digital inputs floating.

The DVR EN*, DATA, and VTT EN are digital input pins that can be used to control the driver output level displayed at the DOUT pin.

DVR EN, DATA*, and VTT EN* can be connected to a reference voltage which defines the logic triggering level. The relationship between the driver control pins and their corresponding logic levels can be seen in Table 1.

Input Voltage	Corresponding Logic Level
$V_{DATA} > V_{DATA*}$	DATA = 1
$V_{DATA} < V_{DATA*}$	DATA = 0
$V_{DVR\ EN} > V_{DVR\ EN*}$	DVR EN* = 0
$V_{DVR\ EN} < V_{DVR\ EN*}$	DVR EN* = 1
$V_{VTT\ EN} > V_{VTT\ EN*}$	VTT EN = 1
$V_{VTT\ EN} < V_{VTT\ EN*}$	VTT EN = 0

Table 1.

Using the logic levels defined in Table 1, driver functionality is described in Table 2.

DVR EN*	VTT EN	DATA	DOUT
1	0	X	HiZ
1	1	X	VTT
0	X	0	VL
0	X	1	VH

Table 2.

Note that DVR EN* determines whether the driver output state will be controlled by the VTT EN or the DATA pin. With DVR EN high (Logic 1), the driver output pin, DOUT, is controlled by the VTT EN pin and can be toggled between the voltage value applied at VTT, and a high impedance state. With DVR En* low (Logic 0), DOUT can be toggled between the voltage values applied to the VL and VH pins by using the DATA input pin.

VH, VL, and VTT

VH, VL, and VTT define the logical “1”, “0”, and “termination” levels of the driver and can be adjusted anywhere over the range spanned by VCC to VEE. There is no restriction between VH, VL, and VTT, in that they can all vary independently over the entire voltage range determined by the power supply levels.

The VH, VL, and VTT inputs are unbuffered in that they also provide the driver output current, so the sources of these voltages must have ample current drive capability.

While VTT is referred to as the termination voltage, it may also be used as a very high “programming” level on many memory devices.

Circuit Description *(continued)*

Driver Output Protection

The Edge211 is designed to operate in a functional testing environment where a controlled impedance (typically 50 Ohms) is maintained between the pin electronics and the DUT. In general, there will be an external resistor at the driver output which series terminates the transmission line to the DUT. In this environment, the driver can withstand a short to any legal DUT voltage for an indefinite amount of time.

In a low impedance application with no additional output series resistance, care must be exercised and systems should be designed to check for this condition and tristate the driver if a short is detected.

The driver does NOT have on-chip short circuit protection or limitation circuitry.

Power Supplies Decoupling

A .1 µF capacitor is recommended between VCC and VEE.

In addition, solid VCC and VEE planes are recommended to provide a low inductance path for the power supply currents. These planes will reduce any inductive supply drops associated with swtiching currents on the power supply pins. If solid planes are not possible, then wide power busses are preferable.

VH, VL, and VTT Decoupling

As the VH, VL, and VTT inputs are unbuffered and must supply the driver output current, decoupling capacitors for these inputs are recommended in proportion to the amount of output current the application requires. In general, a surge current of 50 mA (5V swings series terminated with 50 Ω into a 50 Ω transmission line) are the maximum dynamic output currents the driver should see. The decoupling capacitors should be able to provide this current for the duration of the round trip time between the pin electronics and the DUT, and then recharge themselves before the next such transition would occur. Once this condition is satisfied, the VH, VL, and VTT supply voltages are more responsible for establishing the DC levels associated with each function and recharging the capacitors, rather than providing the actual dynamic currents required to drive the DUT transmission line.

Ideally, VH, VL, and VTT would each have a dedicated power layer on the PC board for the lowest possible inductance power supply distribution.

Power Supply Sequencing

The following sequence should be used when powering up the Edge211.

1. VCC
2. VEE
3. Analog inputs (VH, VL , VTT)
4. Digital inputs (VTTEN, DVREN, DATA)

Latchup Protection

The Edge211 has several power supply requirements to protect the part in power supply fault situations, as well as during power up and power down sequences. VCC must remain greater than or equal to VDD (external supply for the digital logic) at all times. Both VCC and VDD must always be positive (above ground), and VEE must always be negative (at or below ground).

The three diode configuration shown in Figure 2 should be used on a once-per-board basis.

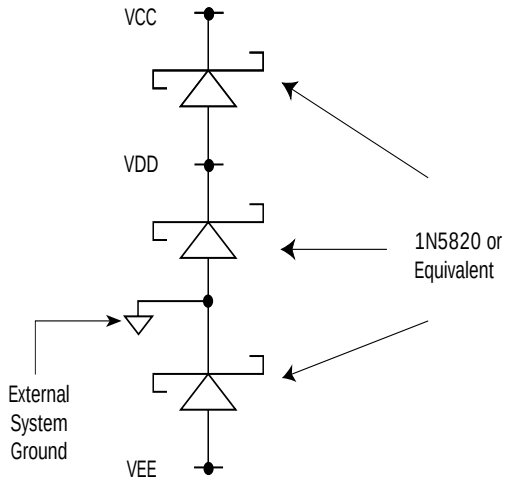
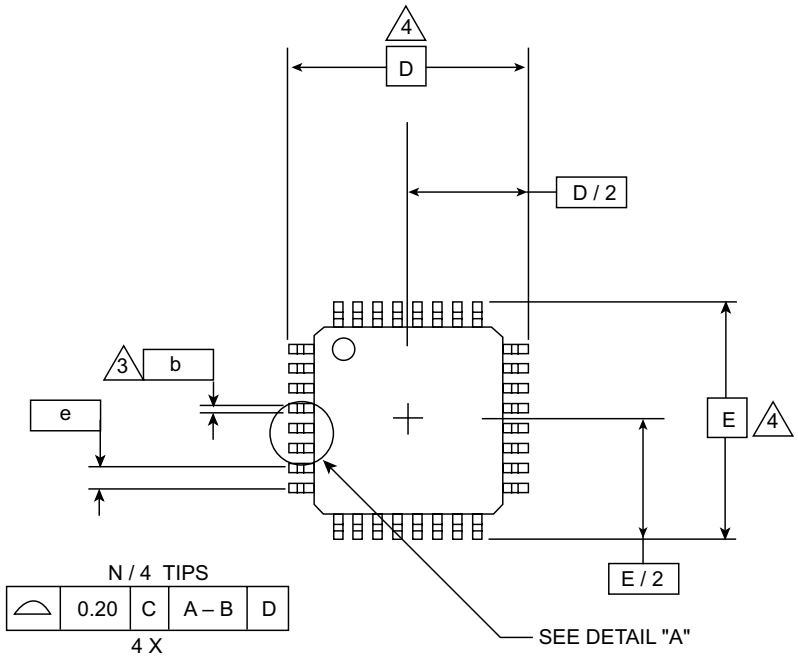


Figure 2.
Power Supply Protection Scheme

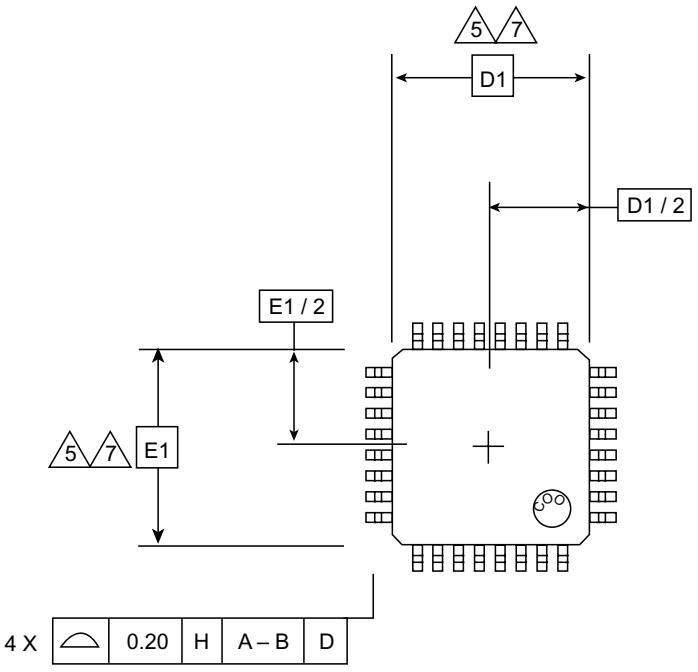
Warning: It is extremely important that the voltage on any device pin does not exceed the range of VEE –0.5V to VCC +0.5V at any time, either during power up, normal operation, or during power down. Failure to adhere to this requirement could result in latchup of the device, which could be destructive if the system power supplies are capable of supplying large amounts of current. Even if the device is not immediately destroyed, the cumulative damage caused by the stress of repeated latchup may affect device reliability.

Package Information

TOP VIEW

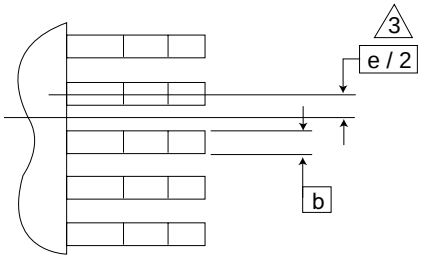


BOTTOM VIEW

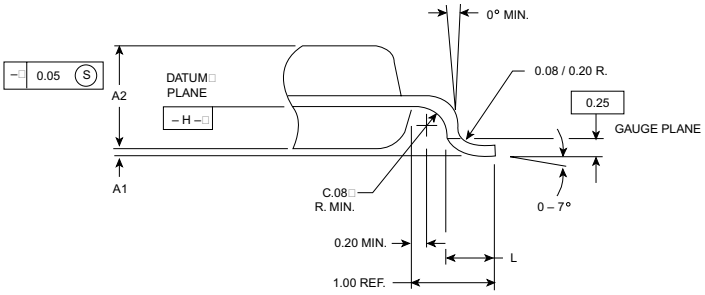


Package Information *(continued)*

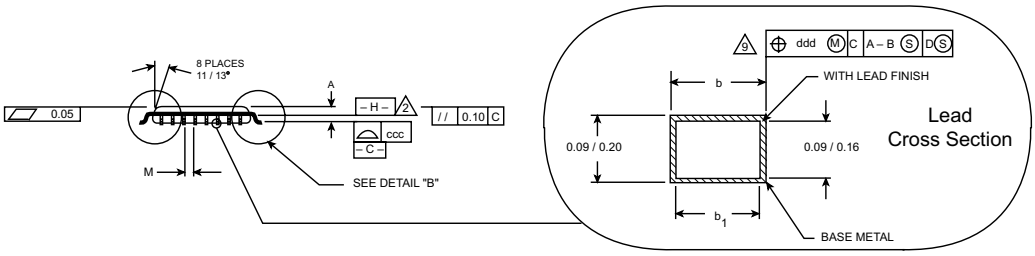
DETAIL "A"



DETAIL "B"



SECTION C–C



Notes:

1. All dimensions and tolerances conform to ANSI Y14.5-1982.
2. Datum plane -H- located at mold parting line and coincident with lead, where lead exits plastic body at bottom of parting line.
3. Datums A-B and -D- to be determined at centerline between leads where leads exit plastic body at datum plane -H-.
4. To be determined at seating plane -C-.
5. Dimensions D1 and E1 do not include mold protrusion.
6. “N” is the total # of terminals.
7. These dimensions to be determined at the datum plane -H-.
8. Package top dimensions are smaller than bottom dimensions and top of package will not overhang bottom of package.
9. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall be 0.08 mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius or the foot.
10. Controlling dimension: millimeter.
11. Maximum allowable die thickness to be assembled in this package family is 0.30 millimeters.
12. This outline conforms to JEDEC publication 95, registration MO-136, variations AC, AE, and AF.

	JEDEC VARIATION All Dimensions in Millimeters			
	AC			
	Min.	Nom.	Max.	Note
A			1.60	
A1	0.05	0.10	0.15	
A2	1.35	1.40	1.45	
D		9.00 BSC.		4
D1		7.00 BSC.		7,8
E		9.00 BSC.		4
E1		7.00 BSC.		7,8
L	0.45	0.60	0.75	
M	0.15			
N		32		
e		0.80 BSC.		
b	0.30	0.37	0.45	9
b1	0.30	0.35	0.40	
ccc			0.10	
ddd			0.20	

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Positive Analog Power Supply	VCC	6		12	V
Negative Analog Power Supply	VEE	-5		-3	V
Total Analog Power Supply	VCC - VEE	9		12	V
Junction	Tj			+125	^{o} C

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
Total Analog Power Supply	VCC - VEE	0		13	V
Positive Analog Power Supply	VCC	0		13	V
Negative Analog Power Supply	VEE	-6		0	V
Analog Input Voltages		VEE - .5		VCC + .5	V
Digital Inputs		VEE - .5		VCC + .5	V
Ambient Operating Temperature	TA	-55		+125	^{o}C
Storage Temperature		-65		+150	^{o}C
Junction Temperature	TJ			+150	^{o}C
Soldering Temperature				260	^{o}C

Stresses above listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

Driver Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Programmable Driver Output Voltages	VH, VL, VTT	VEE		VCC	V
Driver Output Swing	VH – VL	VEE – VCC		VCC – VEE	V
	VH – VTT	VEE – VCC		VCC – VEE	V
	VTT – VLL	VEE – VCC		VCC – VEE	V
DC Driver Output Current	Iout DC	–50		+50	mA
AC Driver Output Current	Iout AC	–220		+220	mA
Output Impedance					
VH (@ +3.0V) (Note 3)	Rout – HI	21.6	23.6	25.6	Ω
VTT (@ +1.5V) (Note 3)	Rout – VTT	22.3	24.3	26.3	Ω
VL (@ 0.0V) (Note 3)	Rout – LOW	22.3	24.3	26.3	Ω
DUT Pin Capacitance (Driver Off)	Cout		13		pF
High Impedance Leakage Current (Note 1)	Ileak		0	4	nA
VH / VL / VTT Offset Voltage (Note 2)	VOS	–100		+100	mV
VH / VL / VTT Gain and Linearity Error (Note 2)		–(.5% + 5)		+(.5% + 5)	mV
Power Supply					
Positive Supply Current	ICC		23	32	mA
Negative Supply Current	IEE		23	32	mA
Total RMS Supply Current @ 80 MHz					
AC + DC Positive Supply Current			70		mA
AC + DC Negative Supply Current (Note 1)			70		mA

Note 1: This parameter is guaranteed by design and characterization. Production testing is performed against a ± 250 nA limit.
Note 2: No load conditions.
Note 3: Tester min / max limits set to Typ ± 2.0Ω. Tester repeatability = .8Ω.

Digital Inputs
DATA, DVR EN*, VTT EN

Parameter	Symbol	Min	Typ	Max	Units
Input High Voltage	INPUT - INPUT*	800			mV
Input Low Voltage	INPUT* - INPUT	800			mV
Input Current	IIN		0	1.0	µA
Digital Input Voltage Range	INPUT, INPUT*	-2.0*		+5.0	V

* -2V or (VEE + 2.0V), whichever is more positive.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Propagation Delay					
DATA IN to DOUT		7	11	14	ns
DVR EN* to DOUT (Active to HiZ) (Note 2)		7	11	14	ns
DVR EN* to DOUT (HiZ to Active) (Note 4)		7	11	15	ns
Minimum Pulse Width (3V Swing)			4	5	ns
Toggle Rate	Fmax	100			MHz
DOUT Output Rise/Fall Times (Note 1)					
1V Swing (20% - 80%)			1.0	1.6	ns
3V Swing (10% - 90%)			1.3	3.0	ns
5V Swing (10% - 905)			1.4	4.0	ns
Driver Temperature Coefficient	$\Delta Tpd/\Delta T$		<25		ps / ^{O}C
Driver Edge to Edge Matching			<500		ps
Tpd vs. Pulse Width (Note 3)			<100		ps
I/O Voltage Spike		-500		500	mV
Overshoot / Undershoot		- (3% + 50)		+ (3% + 50)	%Swing + mV

Note 1: Into 18 cm of 50 Ω transmission line terminated with 1KΩ and 5 pF with the proper series termination resistor.
Note 2: Measured at a voltage change of 500 mV with a 30 mA load. (VH = +5V, VL = 0V)
Note 3: Tested with an input pulse of 20 ns, 30 ns, and 80 ns. T = 100 ns.
Note 4: 4 mA load current.

Ordering Information

Model Number	Package
E211ATF	32-Pin TQFP
EVM211ATF	Edge211 Evaluation Module

Contact Information

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Revision History

Current Revision Date: October 23, 2001
Previous Revision Date: June 27, 2001

Page #	Section Name	Previous Revision	Current Revision
4	Circuit Description		Move "Digital Inputs" section after "Driver Output Protection" section, add new paragraph and table

Current Revision Date: June 27, 2001
Previous Revision Date: October 27, 2000

Page #	Section Name	Previous Revision	Current Revision
5	Application Information		*Add:* Power Supply Sequencing Section *Add:* "External System Ground" to Figure 2