AQ120

LDO Regulator Controller
SOT23-5 Package

Preliminary Specification | **Revision 1.2** | **April 1, 2006**

General Description

The AQ120 is a low cost LDO controller. The AQ120 flexibility allows the setting of the output voltage and controls up to 2 Amps of output current with a minimum number of external components.

The open collector output is capable of driving an external PNP transistor. A temperature stable bandgap reference (1.25 V) controls the output voltage and is programmable through two external resistors. The AQ120 if offered in the very small SOT23-5 package.

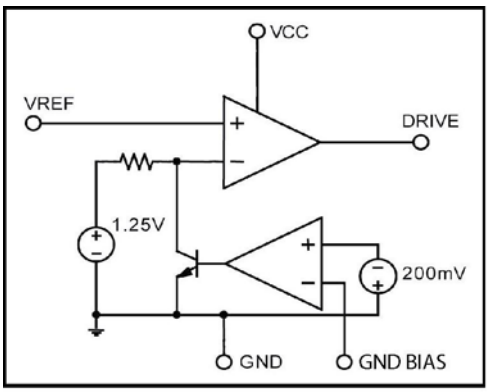
Applications

- Graphic cards
- PC motherboards
- Switching power supply post-regulation
- Telecom equipment
- DVD video player

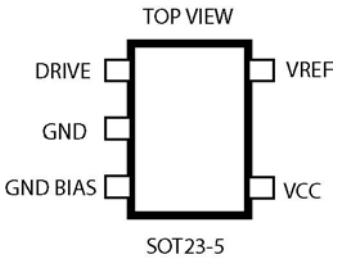
Features

- 1.25V reference with 1.5% accuracy
- Low current consumption
- Offered in small SOT23-5 package
- Wide Vin range: 2.5V to 18V
- 20mA drive current sink
- **RoHS compliant** available

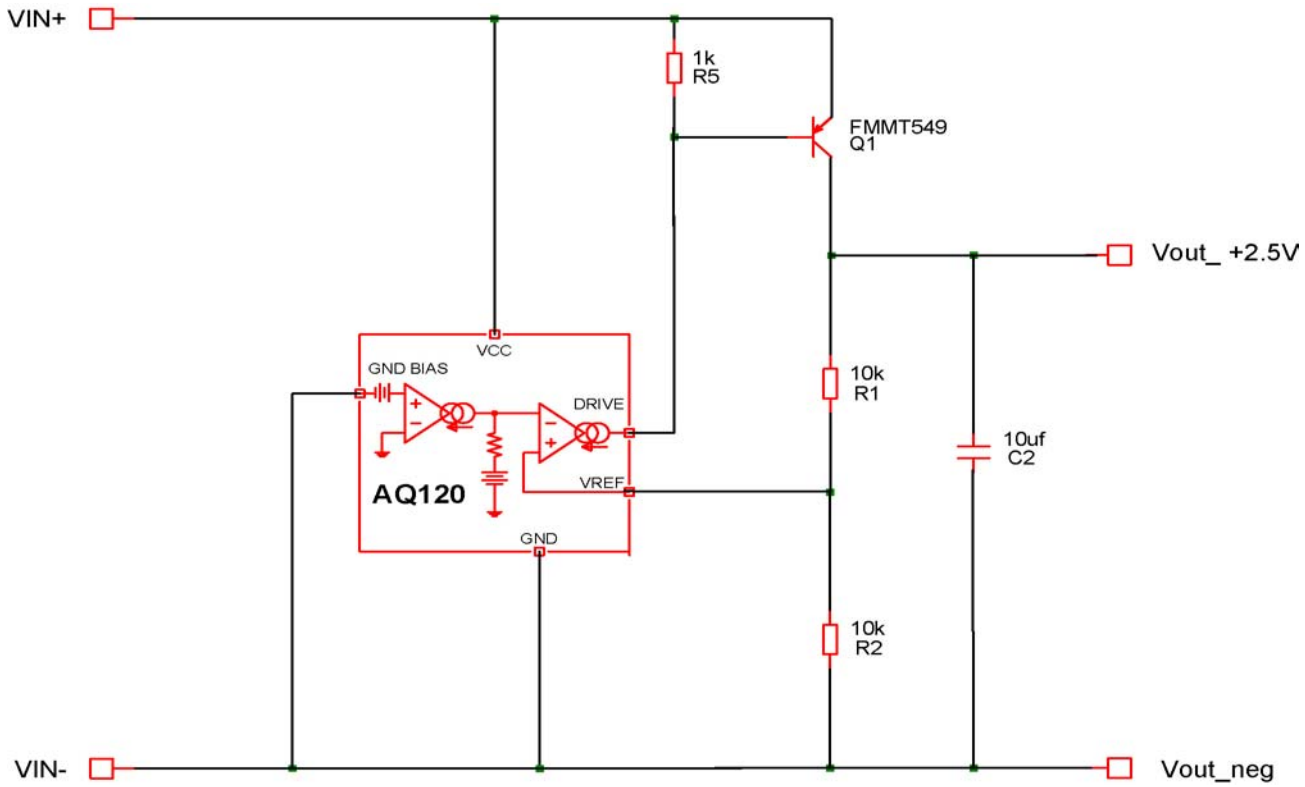
Block Diagram



Pin Configuration



Typical Application



Note: The values of R1and R2 set the output voltage. The typical Vref is 1.25V

Pin Descriptions

Pin	Pin Name	Function
1	DRIVE	Output of error amplifier. 20 mA sink capability to drive PNP pass element
2	GND	Ground
3	GND BIAS	Must connect to GND for proper operation as an LDO Controller
4	VCC	Positive supply
5	VREF	Voltage programming pin; has a threshold of 1.25V.

Ordering Information

Device	Operating Tj	%Tol	Pkg Type	VOUT	Wrap	Order Number
AQ120	-40C˚ ≤ 85C˚	1.5	SOT-23-5	1.25V	T&R	AQ120EX-M5-AJ-TR
AQ120	-40C˚ ≤ 85C˚	1.5	SOT-23-5	1.25V	T&R	AQ120EX-M5-AJ-TRL

Note: The TRL parts are Lead Free and RoHS compliant.

Absolute Maximum Ratings

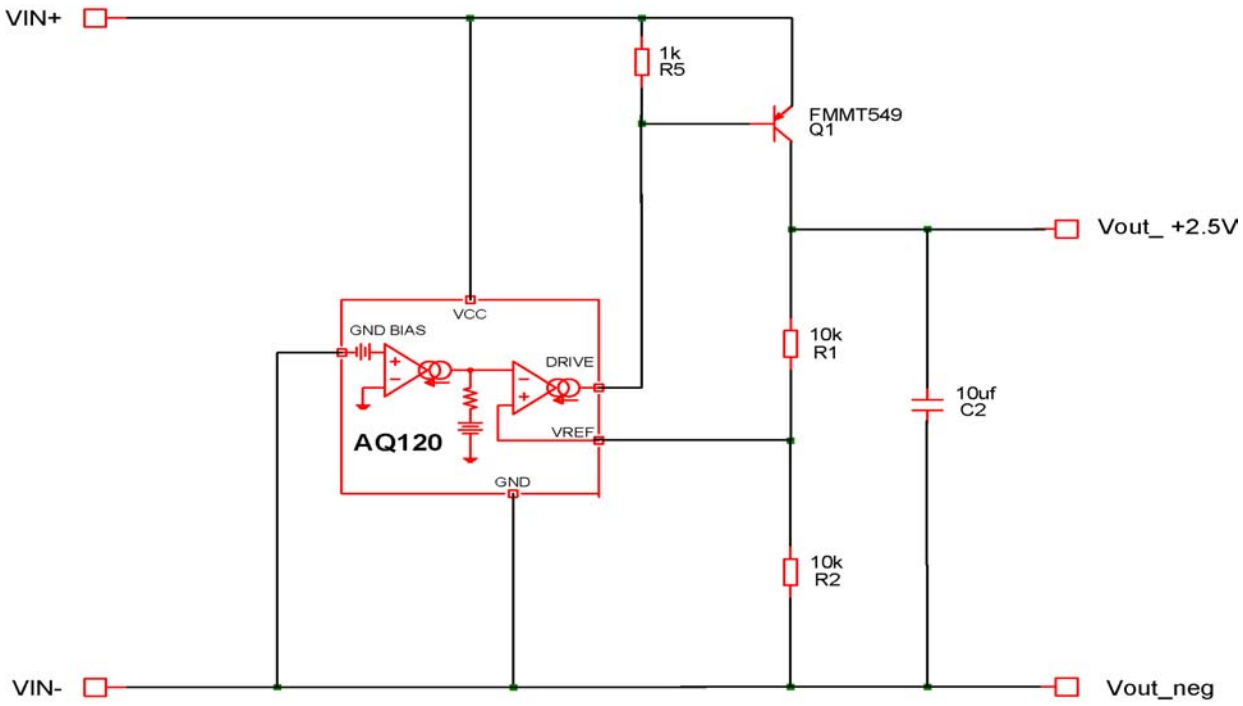
Parameter	Value	Units
V_{CC} Voltage	18	V
DRIVE Voltage	18	V
REF Voltage	18	V
VCC, DRIVE, REF Current	50	mA
Operating Junction Temperature	150	ºC
Lead Temperature (soldering 10 seconds)	300	ºC
Storage Temperature Range	-80 to +150	ºC

Electrical Specifications

Electrical characteristics are guaranteed over the full temperature range –40ºC <Tj< 85ºC. Ambient temperature must be de-rated based upon power dissipation and package thermal characteristics. Unless otherwise stated, test conditions are V_{CC} = 5V, V_{DRIVE} = 4.3V, $V_{GND\ BIAS}$ = GND.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Vcc	Supply Voltage Range		2.5	5	18	V
Icc	Vcc Quiescent Supply Current	V_{REF}= V_{CC}= V_{DRIVE}= 5V		150	300	µA
V_{REF}	Reference Voltage	Ta=25ºC	1.231	1.250	1.268	V
TC REF	Reference Temperature Deviation	-40ºC <Tj<85ºC		0.5	1	%
LnREG	Output variation with Supply Voltage	VCC=2.5V to 18V I_{DRIVE} = 500 µA		0.3	1.0	mV/V
LdREG	Vref variation with Drive Current	I_{DRIVE} = 0.1mA to 10 mA		0.15	0.20	%/mA
I REF	Reference input current	V_{REF} = 0V	-50	-20		nA
V_{DRV}low	Output Saturation Voltage	I_{DRIVE} = 10 mA, V_{REF} = 0V		1.8	2.2	V
I DRIVE	Drive Current	V DRIVE = 5V, V_{REF} = $V_{GND\ BIAS}$ = GND	20	25		mA
I LEAK	Output Leakage Current	V_{DRIVE} = V_{REF} = V_{CC} = 18V		200	400	nA

APPLICATION



(Figure 1)

GENERAL DESCRIPTION

The AQ120 is a linear LDO voltage regulator controller. It drives a discrete PNP transistor while comparing the output to a 1.25V reference. The output voltage is programmable through an external resistor divider. VOUT can be set to any value above 1.25 Volts. The collector of the external PNP transistor provides the output current to the load. Vin range is 2.5V to 18V. The Maximum Load current is Beta of the PNP times IDRIVE. IDRIVE range is 0.1 mA to 20 mA (max).

SETTING THE OUTPUT VOLTAGE

The AQ120 VREF pin is the input to an amplifier comparing to a precision 1.25V reference. With VREF tied back to the output, it will drive the base of the external PNP to maintain output voltage with changing load current and VCC. The regulated output voltage can be set by selecting the proper ratio of R1 and R2.

The Output Voltage is set by:

$$Vout = V_{REF} * \frac{R1 + R2}{R2} = 1.25V * \left(1 + R1/R2\right)$$

SELECTION OF PNP PASS DEVICE

In the application of (figure 1) above, an FMMT549 SOT223 package was used.
However, selection of the PNP pass device is based on Vin max, Iout max, and Power dissipation for your particular application.

VIN max
BVCEO and BVCBO minimum rating of the PNP transistor must exceed the maximum Vin of the application. The AQ120 will stand off 18V max. Therefore the maximum voltage the PNP will experience is 18V.

Iout max
Beta of the PNP transistor will dictate the maximum output current as per the equation:

$$Iout\max = Idrive\max(20mA) * BetaExt.PNP$$

Higher beta of the PNP will improve the Vout variation due to change in load (load reg.) Minimizing the Idrive required will also minimize the Load reg. as Vout will decrease by .15% per mA of Idrive. Therefore, delta 10mA of Idrive will cause a delta 1.5% of Vout.

Power dissipation
Selection of the external PNP package is based on size requirements and power dissipation. Consult the transistor data sheet for power considerations.

Contact Information

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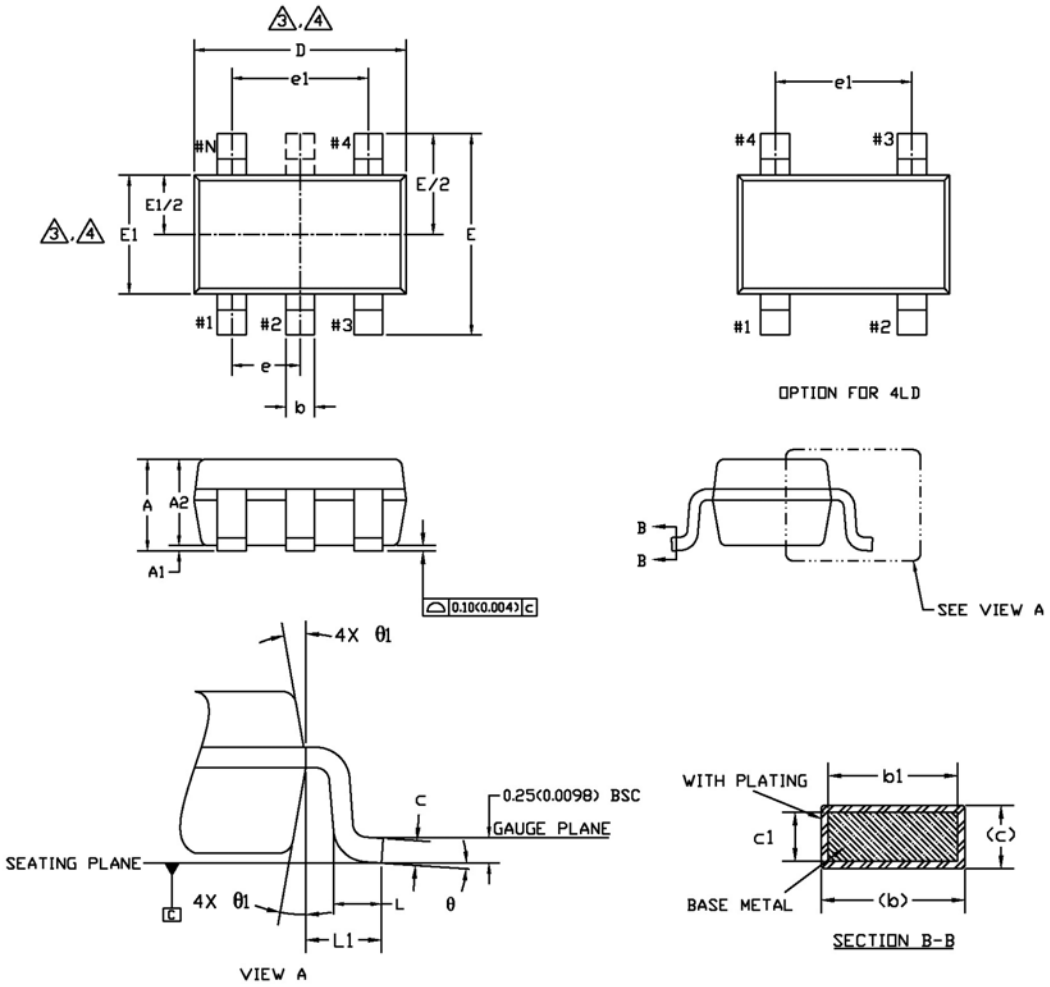
Package Dimensions

SOT23-3, SOT23-4, SOT23-5, SOT23-6



SYMBOL	COMMON					
	DIMENSIONS MILLIMETER			DIMENSIONS INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.20	1.30	1.40	0.047	0.051	0.055
A1	0.05	-	0.15	0.002	-	0.006
A2	0.90	1.15	1.30	0.035	0.045	0.051
b	0.35	-	0.50	0.013	-	0.020
b1	0.35	0.40	0.45	0.013	0.015	0.017
c	0.08	-	0.22	0.003	-	0.008
c1	0.08	0.13	0.20	0.003	0.005	0.007
D	2.90 BSC			0.114 BSC		
E	2.80 BSC			0.110 BSC		
E1	1.60 BSC			0.062 BSC		
e	0.95 BSC			0.037 BSC		
e1	1.90 BSC			0.074 BSC		
L	0.35	0.45	0.55	0.013	0.017	0.021
L1	0.60 REF.			0.023 REF.		
θ	0°	4°	8°	0°	4°	8°
θ1	10° TYP			10° TYP		

NOTE :

1. Dimensioning and tolerancing per ASME Y 14.5 M - 1994.
2. Dimensions are in millimeters.Converted inch dimension are not necessarily exact.
3. Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 0.15 mm per side. Dimension E1 does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.15 mm per side.
4. Top package may be smaller than the bottom package Dimension D and E1 are determine at the outermost extremes of the plastic body exclusive of mold flash gate burrs and interlead flash.
5. Terminal numbers are shown for reference only. Die is facing up for molding. Die is facing down for trim/form.