MULTIMODE DMA CONTROLLER

TMP82C37AP-5/TMP82C37AM-5/TMP82C37AT-5

1. GENERAL DESCRIPTION

The TMP82C37AP-5/AM-5/AT-5 (hereinafter referred to as TMP82C37A) is a multimode direct memory access (DMA) controller. The TMP82C37A improves the system function by directly transferring information between the system memory and external devices. Memory-to-Memory data transfer capability is also provided.

The TMP82C37A is provided with versatile programmable control functions in order to improve data throughput.

The TMP82C37A is used with an 8-bit address register connected externally. The TMP82C37A has four built-in independent channels and it is possible to expand channels through cascade connection.

There are three basic data transfer modes which are programmable by the user. Each channel is programmable individually and autoinitialization is possible by End of Process ($\overline{EOP}$) signal.

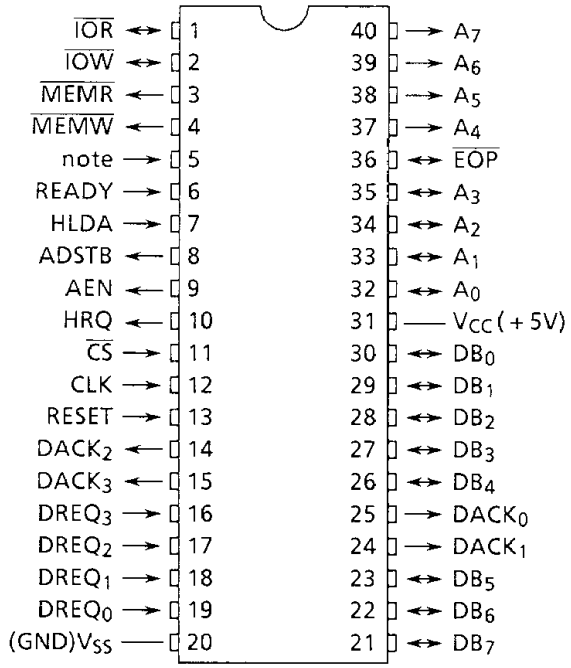
Each channel has the maximum 64K capability for both address and word count. $\overline{EOP}$ signal is capable of terminating data transfer between DMA and memories. $\overline{EOP}$ signal is useful for block search or verify or for terminating erroneous service.

2. FEATURES

- Four independent DMA channels available
- Three transfer modes available; block, demand, and single transfer modes
- Independent auto initialize function provided to each of all channels
- Memory-to-Memory transfer
- Address increment or decrement
- All DMA request disabled by disabling the master system
- Individual DMA request enable/disable control
- Unrestricted channel expansion by cascade connection
- End of Process ($\overline{EOP}$) input for terminating transfer
- Software DMA Request
- Polarity control provided for DREQ signal and DACK signal
- Option for increasing transfer speed up to 2.5M word/sec (@5MHz)
- Single +5V power supply
- Low power consumption 5mA TYP. @5MHz
- Extend operating temperature −40°C to +85°C

3. PIN CONNECTION (TOP VIEW)

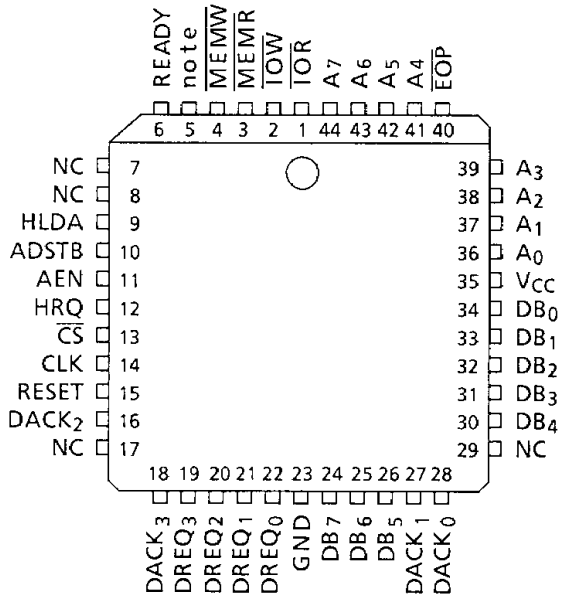
3.1 TMP82C37AP-5 (DIP), TMP82C37AM-5 (SOP)



050489

Note : PIN 5 must be connected to V_{CC} or opened.

3.2 TMP82C37AT-5 (PLCC)



050489

Note : PIN 5 must be connected to Vcc or must be opened.
NC : No Connection

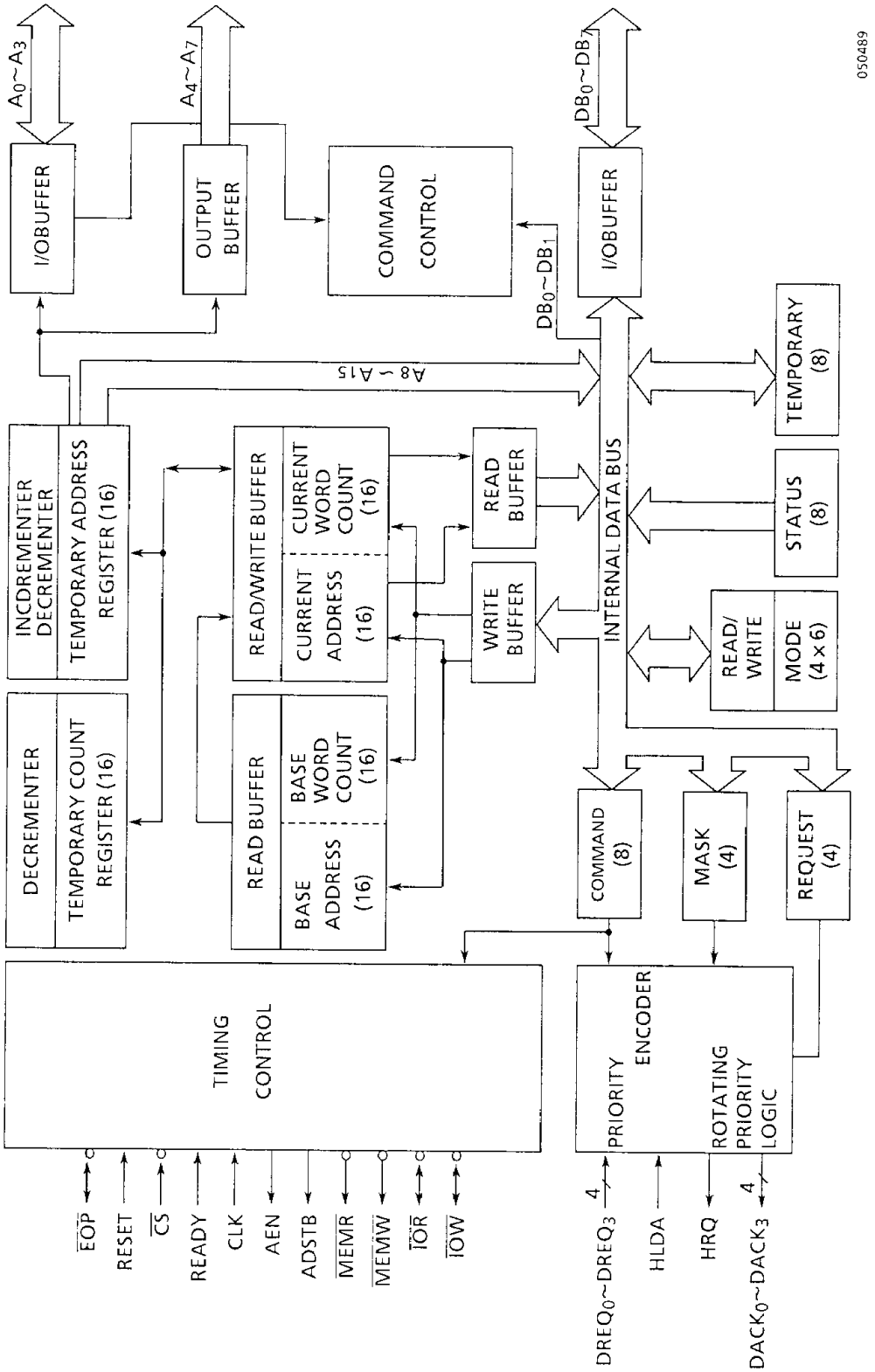


Figure 3.1 Block Diagram of TMP82C37A

4. PIN NAME & FUNCTION

- V_{CC}

  +5V power supply

- V_{SS}

  Ground

- CLK (Clock, Input)

  This input controls the internal operation and data transfer rate of the TMP82C37A.

- $\overline{CS}$ (Chip Select, Input)

  This input is low active and used to select the TMP82C37A as an I/O device during an I/O read or I/O write by the host MPU. If $\overline{IOR}$ or $\overline{IOW}$ is toggled following each transfer when a host MPU and the TMP82C37A are transferring data mutually, $\overline{CS}$ may be kept at LOW.

- RESET (Reset, Input)

  This input is asynchronous input to clear the command, status, request and temporary registers. In addition, this input is used to clear First/Last flip-flops and set the mask register. Following the reset, the TMP82C37A is placed in the idle cycle.

- READY (Ready, Input)

  This input is used to extend the memory or I/O read and write pulses in DMA cycle in order to adapt to low speed memories or I/O peripheral devices.

- HLDA (Hold Acknowledge, Input)

  By this signal, the TMP82C37A knows that the system bus control is turned over from MPU.

- $DREQ_0$-$DREQ_3$ (DMA Request, Input)

  DMA request signals are input from peripheral circuits. If priority is fixed, the highest priority is given to $DREQ_0$ and the lowest priority to $DREQ_3$. Polarity of DREQ is programmable. DREQ becomes high active by RESET.

- DB_0-DB_7 (Data Bus, Input/Output)

  The Data Bus are bidirectional 3-state lines connecnted to the system data bus. During MPU is in I/O read state, output is enabled and contents of the registers (address, status, temporary and word count) are output to MPU. During MPU is in I/O write state, the data bus serves as input and it becomes possible to program the control register of the TMP82C37A.

  During the DMA cycle, the most significant 8 bits of address are output on the data bus and latched by ADSTB signal externally. During the Memory-to-Memory transfer, the data of the source memory location are loaded into the temporary register of the TMP82C37A by the read operation and the contents of the temporary register are output to the destination memory location by the write operation.

- $\overline{IOR}$ (I/O Read, Input/Output)

  I/O read is a bidirectional, low active and 3-state signal. During the idle cycle, this signal serves as an input control signal used by MPU to read the control registers of the TMP82C37A. During the active cycle, this signal serves as an output control signal used by the TMP82C37A to access data from the peripheral circuit during the DMA read and transfer.

- $\overline{IOW}$ (I/O Write, Input/Output)

  I/O write is a bidirectional, low active, 3-state signal. During the idle cycle, this signal serves as an input control signal used by MPU to load the information to the TMP82C37A. During the active cycle, this signal served as an output control signal used by TMP82C37A to load the data to the peripheral. For write to the TMP82C37A by MPU, the leading edge of the write signal ($\overline{IOW}$) is required for every data transfer. It is not possible to write more than two data by toggling $\overline{CS}$ while holding the $\overline{IOW}$ pin at low level.

- $\overline{EOP}$ (End of Process, Input/Output)

  $\overline{EOP}$ (End of Process) is a signal relative to the end of DMA service, and is a low active, bidirectional and open drain signal. When the channel word count reaches from 0000H to FFFFH, the TMP82C37A outputs low pulse of $\overline{EOP}$ to peripheral devices as the end signal.

  In addition, it is also possible to pull $\overline{EOP}$ to the low level by peripheral device in order to cause the end of process.

  When $\overline{EOP}$ is received (internally or externally), the channel which is presently active terminates the service, sets that TC bit of the status register and resets that request bit.

  If that channel is programmed for auto initialization, that current register is updated from the base register. In all other cases, mask bit is set and the content of that register remains unchanged.

  During the Memory-to-Memory transfer, $\overline{EOP}$ is output when TC of channel 1 is produced. $\overline{EOP}$ is always used for channels with active DACK and external $\overline{EOP}$ has no connection when $DACK_0$-$DACK_3$ are all inactive.

  $\overline{EOP}$ is an open drain signal and therefore, requires an external pull-up resistor.

- A_0-A_3 (Address, Input/Output)

  The four least significant address lines are the bidirectional 3-state signals. In the idle cycle, these lines serve as the input signals and used by MPU for write/read of the control register. In the active cycle, they serve as the output signals and become low order 4 bits of output address.

- A_4-A_7 (Address, Output)

  The four most significant address lines are 3-state output signals. These lines are enabled for the period of DMA service only.

- HRQ (Hold Request, Output)

  This is the hold request signal to MPU, and is used to request the system bus control. HRQ is output by the TMP82C37A according to a software request or unmasked DREQ.

- $DACK_0$-$DACK_3$ (DMA Acknowledge, Output)

  The DMA acknowledge lines indicate that channels are active. Normally, these are used for selecting peripheral devices. Only one DACK becomes active but it does not become active unless DMA is controlling the system bus. Polarity of these lines are programmable. After reset, they initialize low active.

- AEN (Address Enable, Output)

  Address Eanble is a high active signal and used to enable output of the external latch which holds high order byte of address and to disable the system bus during the DMA cycle.

  During the DMA transfer, HLDA and AEN are used to disable all I/O except programmed I/O. The TMP82C37A disables $\overline{CS}$ input for DMA transfer to prevent itself from being selected automatically.

- ADSTB (Address Strobe, Output)

  This signal is a strobe output to an external latch circuit and is used to latch high order 8-bit address from DB_0-DB_7.

- $\overline{MEMR}$ (Memory Read, Outputd)

  This is a low active 3-state output used for transferring data from a memory to a peripheral device or for data accessing from a selected memory during the Memory-to-Memory transfer.

- $\overline{MEMW}$ (Memory Write, Output)

  This is a low active 3-state output used for transferring data from a peripheral device to a memory or for writing data into a selected memory during the Memory-to-Memory transfer.

5. OPERATIONAL DESCRIPTION

5.1 DMA OPERARTION

The TMP82C37A has two operations; idle cycle and active cycle. Each of these cycles consists of several states.

On the TMP82C37A, it is possible to consider 7 states each of which consists of one clock cycle. State I (SI) is an idle state. This is such a state as there is no valid DMA request pending. SI is a program condition state which is programmable by MPU.

State 0 (S0) is the first DMA service state. This is a state that the TMP82C37A made a hold request to MPU but not yet received the acknowledge signal from MPU. When the acknowledge signal is recieved from MPU, the transfer is started.

S1, S2, S3 and S4 are the DMA service states. If more time is required by the transfer, it is possible to insert the wait state (SW) before S4 by READY input to the TMP82C37A.

In the Memory-to-Memory transfer, in order to assure complete transfer, read from the memory and write to the memory are required. 8 states are necessary for one transfer. The first four states (S11, S12, S13 and S14) are read from the memory and the latter four state (S21, S22, S23 and S24) are write to the memory.

The temporary data register is used as an intermediate storage area of memory bytes.

5.2 IDLE CYCLE

When DMA service is not requested by channels, the TMP82C37A enters into the idle cycle and is placed in SI state. In order to check if the channels request DMA service, the TMP82C37A samples DREQ for every clock.

The TMP82C37A also samples $\overline{CS}$ to check if MPU is requesting read or write of internal registers. When $\overline{CS}$ is low and HLDA is also low, the TMP82C37A is placed in the program condition.

At this time, MPU is able to change or check the content of any internal register through read or write from that register.

Address lines A_0-A_3 are input signals and used for selecting a register being read or written. $\overline{IOR}$ and $\overline{IOW}$ are used for selecting read or write and decide read/write timing.

The internal flip-flop is used for generating address extension bits according to number and size of internal registers. (First/Last flip-flop) This bit is used for deciding high or low order byte of 16-bit address and word count register.

The flip-flop is reset by the master clear or reset. In addition, this flip-flop also can be reset by an independent software command. On a special software command, the execution in the TMP82C37A program conditon is possible. These commands are decoded as in the address setting when both $\overline{CS}$ and $\overline{IOW}$ are active.

The data bus is not used for this command. This command is available in three types; clear First/Last flip-flop, master clear and clear mask register.

5.3 ACTIVE CYCLE

When the TMP82C37A is in idel cycle and the channels are requesting DMA service, the TMP82C37A outputs HRQ to MPU and goes into the active cycle. In this cycle, the DMA service for any one of 4 modes is executed.

5.3.1 Single Transfer Mode:

In this mode, the TMP82C37A performs a single byte transfer during each HRQ/HLDA handshake. When DREQ becomes active, HRQ becomes active. After MPU responds by driving HLDA active, a single byte transfer will take place. After the transfer HRQ becomes inactive, its word count is decreased, and address is increased or decreased. When word count changes from 0000H to FFFFH, a terminal signal is generated and if the channels are programmed, the auto initialization is made.

To execute the single byte transfer, it is necessary to hold DREQ until DACK corresponding each DREQ becomes active. If DREQ is continuously active, HRQ becomes inactive following each transfer and then, becomes active again, and the new single byte is executed following the leading edge of HLDA.

On the 8085A system, one machine cycle can be executed during the DMA transfer.

5.3.2 Block Transfer Mode:

In this mode the TMP82C37A continues the transfer until terminal count (TC) is generated or an external End of Process signal ($\overline{EOP}$) is encountered. Here, TC is produced when the word count changes from 0000H to FFFFH.

What is required for DREQ is to hold it in active state until DACK becomes active. Auto initialization (if so programmed) is taken place at the end of DMA service.

5.3.3 Demand Transfer Mode:

In this mode the TMP82C37A continues the transfer until TC is produced or $\overline{EOP}$ is or DREQ becomes inactive. Thus, it is possible for a device, which is requesting the DMA service, to suspend the transfer by making DREQ inactive. The service is resumed when DREQ is made active again. It is possible to read an intermediate value of address and word count from the current address and current word count register of the TMP82C37A while the system bus is returned to MPU during execution of the DMA service.

The auto initialization is taken place following TC or $\overline{EOP}$ at the end of DMA service. In order to perform a new DMA service following the auto intialization, the active edge of DREQ is necessary.

5.3.4 Cascade Mode:

This mode is used when the TMP82C37A is cascade connected for a simple system expansion. HRQ and HLDA of the additional TMP82C37A are connected to DREQ and DACK of the first TMP82C37A. DMA request to the TMP82C37A which is added for the purpose of system expansion is authorized by the priority circuit of the first TMP82C37A.

If the priority is already decided, the additional device must wait till the acknowledge request. The cascade channel of the first TMP82C37A is used only for deciding priority of the additional TMP82C37A and therefore, the channel itself does not output address nor control signal. This is to prevent the added device from colliding with output of the cascade channel. On the TMP82C37A, DACK respond to DREQ. However all other outputs except HRQ are disabled.

The state of cascade connection is shown in Figure 5.1. In Figure 5.1, two levels of DMA are formed. To further expand the TMP82C37A, it is possible to add it to the second level using the TMP82C37A, it is possible to add it to the second level using the remaining channel of the first TMP82C37A. To further add another TMP82C37A, the third level can be formed by cascade connecting it to the second level.

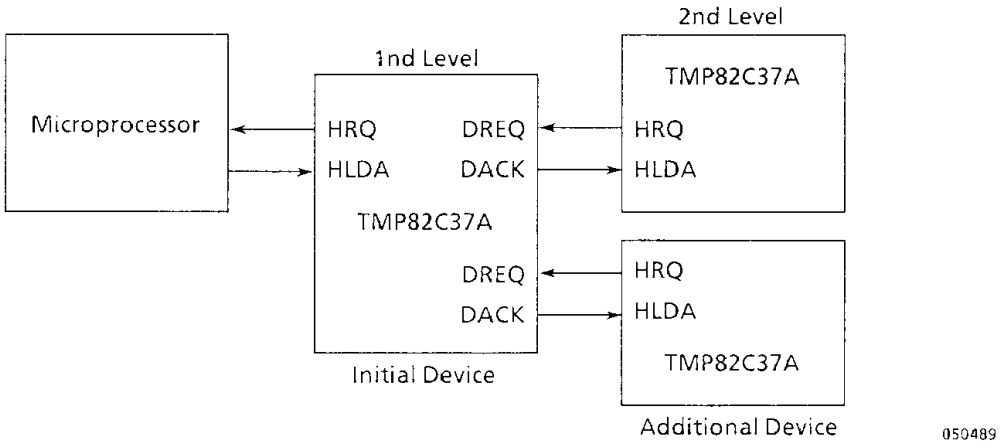


Figure 5.1 Example of Cascade Connection of TMP82C37A

5.4 TRANSFER FORMAT

3 different transfer format are available for 3 active transfer modes.

They are read, write and verify. In the write transfer, data is transferred from I/O device to memory by $\overline{\text{MEMW}}$ and $\overline{\text{IOR}}$. In the read transfer, data is transferred from memory to I/O device by $\overline{\text{MEMR}}$ and $\overline{\text{IOW}}$.

The verify transfer is a pseudo transfer. The TMP82C37A perform such operations as address generation for read or write transfer, answer to $\overline{\text{EOP}}$, etc. However, memory or I/O control line does not become active.

5.5 MEMORY-TO-MEMORY TRANSFER:

The TMP82C37A has the ability of block movement and is capable of transferring data block from one memory address location to another location. When Bit 0 of the command register is programmed at Logic 1, Channel 0 and 1 operate as the Memory-to-Memory transfer channels. Channel 0 serves as source address and Channel 1 as a destination address, and the word count of Channel 1 is used. The Memory-to-Memory transfer is executed when software DMA request is set for Channel 0.

The Memory-to-Memory transfer must use the block transfer mode.

When Channel 0 is programmed as a fixed source address, it is possible to write single source words into a memory block.

When the TMP82C37A is programmed for the Memory-to-Memory transfer, Channel 0 and Channel 1 must be masked. The same value as that is set for Channel 1 must be set for the word count of Channel 0. During the Memory-to-Memory transfer, AEN became active but DACK does not become active.

During the Memory-to-Memory transfer, the TMP82C37A respond to external $\overline{EOP}$ signal. In the block search, the data comparator uses this ($\overline{EOP}$) input to terminate the DMA service when match is found. The Memory-to-Memory transfer timing is shown in Timing Diagram 4.

5.6 AUTO INITIALIZATION:

When Bit 4 of the mode register is set to 1, the channels are set up for the auto initialization. During the auto initialization, data are loaded into the current address and current word count registers from the base address and base word count registers, respectively, following $\overline{EOP}$. The base registers are loaded by MPU simultaneously with the current registers and remain unchanged during the DMA service.

When the channels are under the auto initialization, mask bit is not set by $\overline{EOP}$.

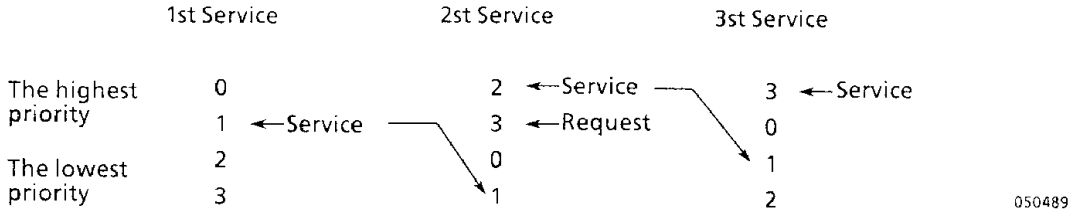
Following the auto initialization, that channel is prepared to execute the service without interposition of MPU.

5.7 PRIORITY:

The TMP82C37A has two types of priority which can be selected by software. The first type is the fixed priority. Channel priority is fixed by channel number. The lowest priority is channel 3, followed by 2, 1, and the highest priority is channel 0.

The second type is the rotating priority. In this type, an accepted channels is then given with the lowest priority .

On the rotating priority in the singel chip DMA system, the highest priority of any one channel comes after no more than three higher priority services have occurred. This rotating priority prevent a specific channel from occupying the system all the time. (See the following below diagram.)



The priority judging circuit selects a channel with the highest priority requesting the DMA service for every active edge of HLDA. Once the channel starts the service, that operation will not be suspended even when the service is demanded by another channel with higher priority. A channel with higher priority can get the control right only after a channel with lower priority relinquished HRQ. Whenever the control is transferred from a channel to another channel, MPU gets the system bus control right. This assures the leading edge of HLDA which is used for selecting a channel with the highest priority.

5.8 COMPRESSED TRANSFER TIMING:

In order to accomplish greater throughput allowed by system characteristics, the TMP82C37A is capable of compressing the transfer time to 2 clock cycles. As can be seen from Timing Diagram 3, State S3 is used to extend readout pulse access time. When State S3 is removed, readout pulse width becomes equal to write pulse width. Then, the transfer will consist of State S2 for changing address and State S4 for executing read/write. State S1 is produced when A_8 to A_{15} are updated (refer to Address Generation). Compressed transfer timing is shown in Timing Diagram 5.

During Memory-to-Memory transfer, compressed transfer is not available.

5.9 ADDRESS GENERATION:

To reduce number of pins, the TMP82C37A has the multiplexed address/data bus. State S1 is used to output high order address byte to the external latch. The trailing edge of ADSTB is used to load the address byte from the data line on the external latch circuit. AEN is used to enable latch outputs from 3 states. Low order address byte is ditectly output by the TMP82C37A.

A_0 to A_7 are connected to address bus. Timing Diagram 3 show the relationship among CLK, AEN, ADSTB, DB_0 to DB_7 and A_0 to A_7.

Address produced during the block and demand transfers are sequential. For many transfer the same address data will be held in the external address latch. This address data changes only when carry or borrow from A_7 to A_8 is produced in the normal sequence. To raise system throughput, on the TMP82C37A, S1 state is executed only for updating A_8 to A_{15} requiring the external latch.

6. DESCRIPTION OF REGISTERS

Register Name	Size	Number
Base address register	16-bit	4
Base word count register	16-bit	4
Curren address register	16-bit	4
Current word count register	16-bit	4
Temporary address register	16-bit	1
Temporary word count register	16-bit	1
Status register	8-bit	1
Command register	8-bit	1
Temporary register	8-bit	1
Mode register	6-bit	4
Mask register	4-bit	1
Request register	4-bit	1

050489

Figure 6.1 Internal Registers

6.1 CURRENT ADDRESS REGISTER:

Each channel has a 16-bit current address register. This register holds addresses that are used during the DMA transfer. After each transfer, this register is automatically incremented or decremented, and intermediate address values are stored in the current address register during the transfer. Write or read of this register is made by MPU. An original value is initialized again by the auto initialization.

The auto initialization is taken place only after $\overline{EOP}$.

6.2 CURRENT WORD COUNT REGISTER:

Each channel has a 16-bit current word count register. For this register, the number of words to be transferned that is one less than that to be tranferred must be programmed. The word counter is decremented after each transfer. Intermediate values of word count are stored in this register during the transfer. When the register value goes from 0000H to FFFFH, TC (Terminal Count) is produced.

When this register is in the program condition, load or read is made by MPU. Following the end of DMA service, this register is initialized to original values again by the auto initialization.

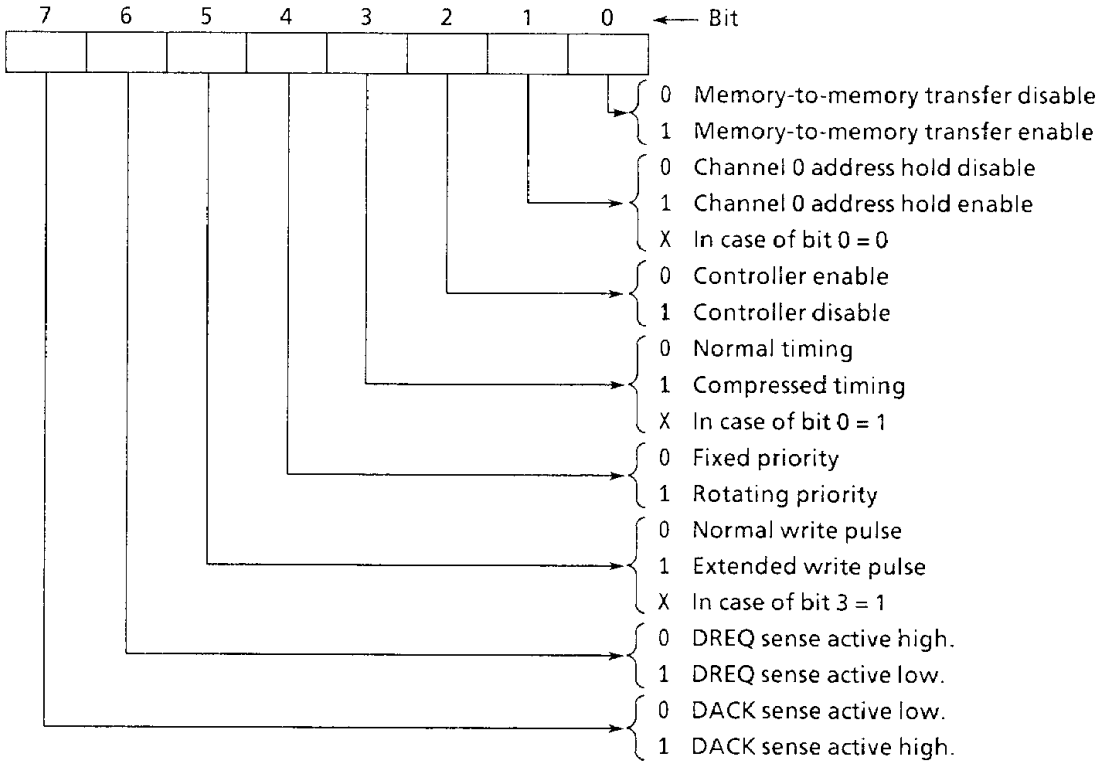
The auto initialization is taken place only when $\overline{EOP}$ is produced. Note that the content of the word count register becomes FFFFH following internally produced $\overline{EOP}$.

6.3 BASE ADDRESS REGISTER, BASE WORD COUNT REGISTER:

Each channel has a pair of registers; the base address register and base word count register. These 16-bit registers store original values of related current registers. These registers are used to store original values of current registers at time of the auto initialization. Write to the base register is made at the same time of write into equivalent current registers during the programming by MPU. Therefore, write into the current registers which store intermediate values are made over these intermediate values. The base register cannot be read out by MPU.

6.4 COMMAND REGISTER:

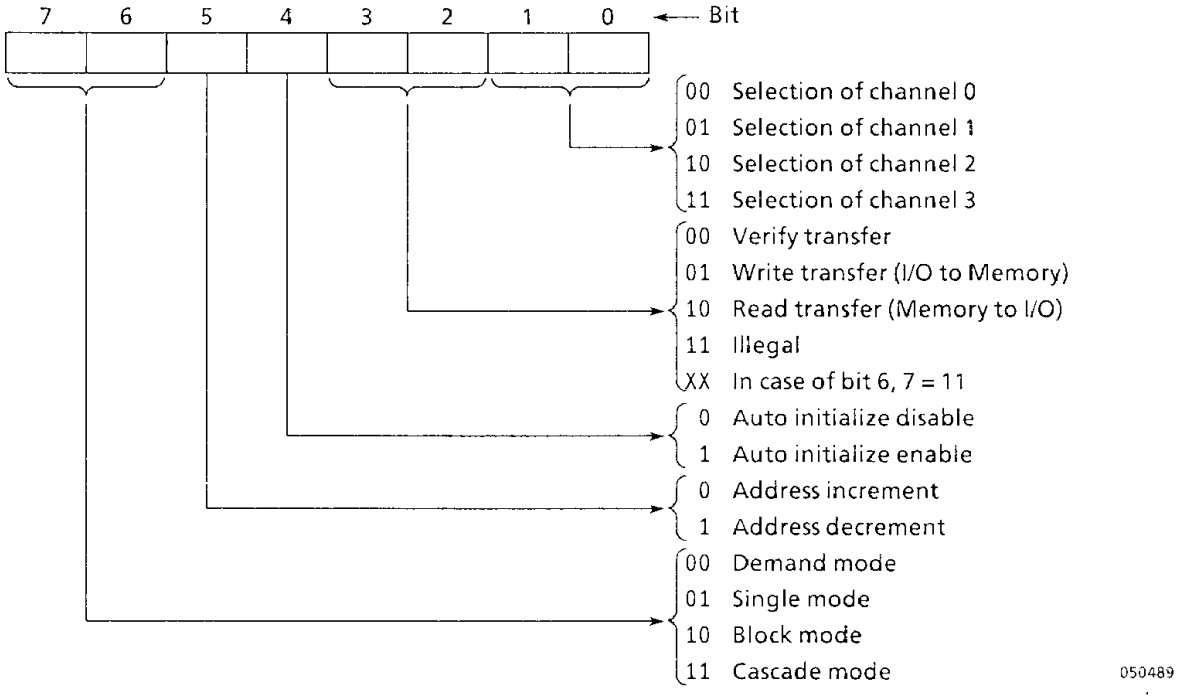
This 8-bit register controls the operation of TMP82C37A. This command register is programmed (clear or reset) by MPU when it is in the program condition. The figure below show the functions of command bits. For address codes, refer to Figure 6.2.



050489

6.5 MODE REGISTER:

All channels have a 6-bit mode register, respectively. This mode register is written by MPU when it is in the program condition, and Bit 0 and 1 select the channel to be programmed.

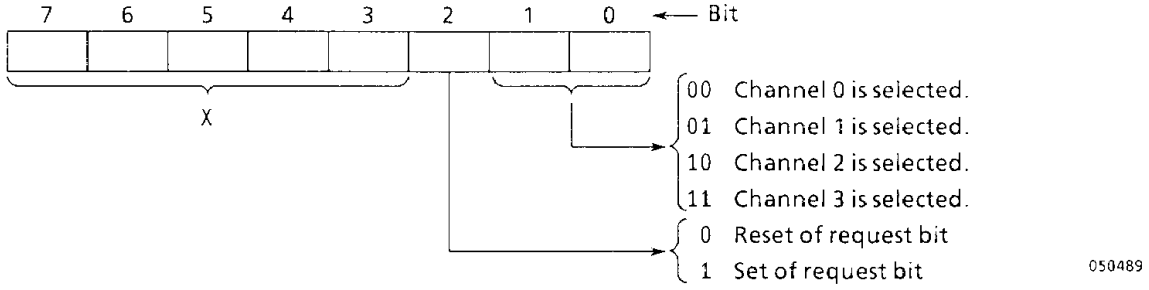


6.6 REQUEST REGISTER:

The TMP82C37A is capable of responding to DMA service request by software similar to DREQ. Each channel has a single bit request register which cannot be masked. Further, priority is given by the priority encode circuit.

Bit of each register is set or cleared by software and further, cleared by generation of TC or external $\overline{EOP}$. All registers are cleared by reset. In order to set or reset bit, a proper form of data word is loaded by software.

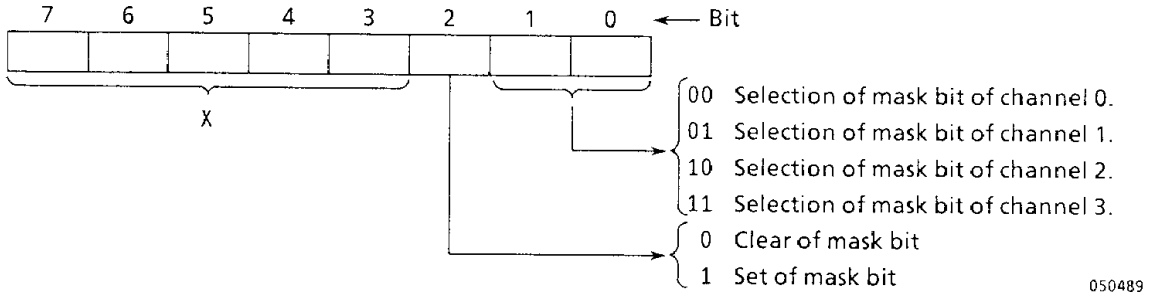
Address codes are shown in Figure 6.2. DMA service request by software is accepted only when the channels are in the block mode. In the Memory-to-Memory transfer, DMA service request only to Channel 0 by this software command becomes valid.



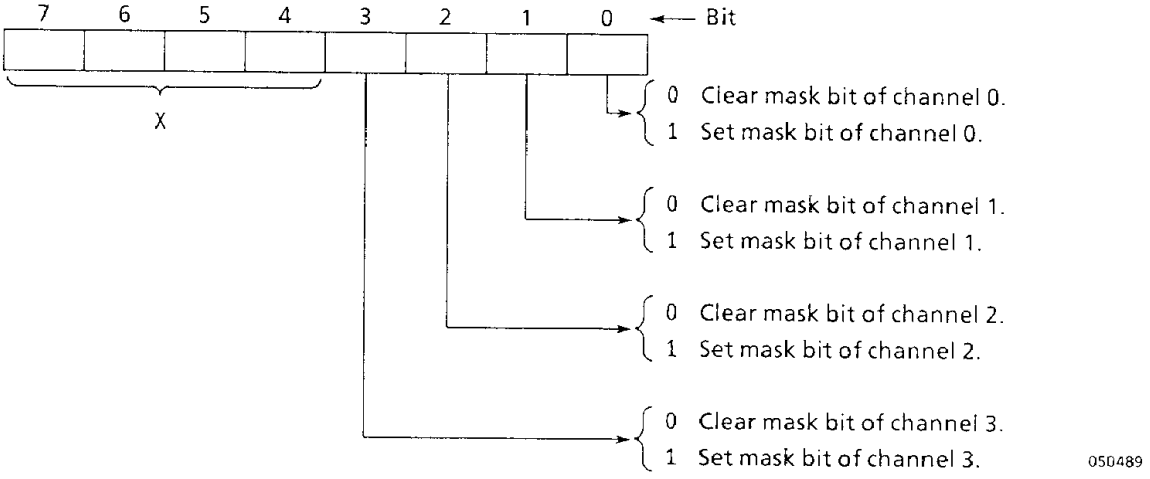
6.7 MASK REGISTER:

For each channel, mask bit are allocated to the mask register to disable DREQ input. If the auto initialization has not been programmed for the channels, the channel corresponding to a mask bit is set when $\overline{EOP}$ is produced. Each bit of the 4-bit mask register is also set or cleared by the software command. All bits are also set by reset. This will disable all DMA requests until the clear mask register command is enabled.

Command addressing is shown in Figure 6.2.



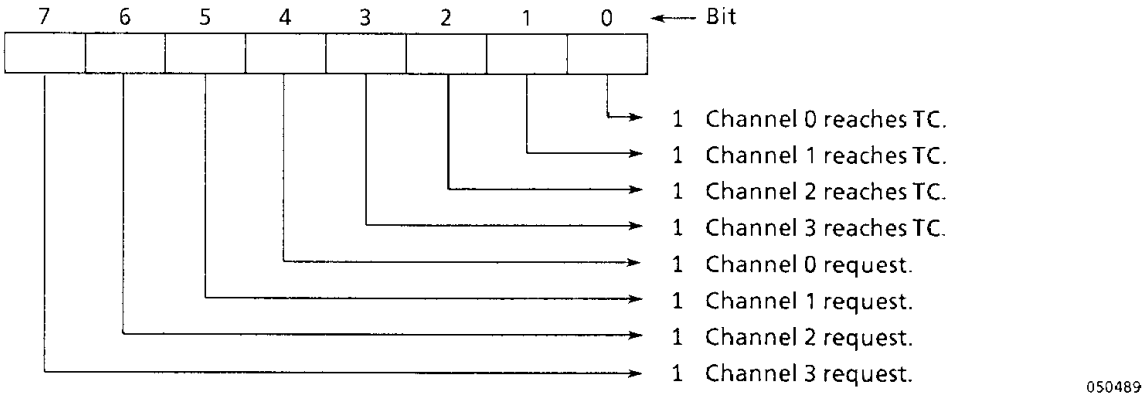
All four bits of the mask register can be written also by a single command.



6.8 STATUS REGISTER:

This register is read out by MPU through the TMP82C37A. Status information of the TMP82C37A at time of readout is included. Information as to which channel reaches the terminal count (TC) and which channel is pending the DMA request are included in this information. Bits 0 to 3 are set every time when a channel reaches TC including the auto initialization.

These bits are cleared by reset or when each status is read out. Bits 4 to 7 are always set when corresponding channels are requesting the DMA service



6.9 TEMPORARY REGISTER:

This register is used for holding data during the Memory-to-Memory transfer. A last word transferred following the end of transfer is read out by MPU that is in the program condition. Unless cleared by reset, this register contains the last word transferred during the preceding Memory-to-Memory transfer.

6.10 SOFTWARE COMMANDS:

These commands are the special software commands which are executed in the program condition and do not depend upon the specified bit pattern on the data bus. These commands are available in following three commands:

6.10.1 Clear First/Last Flip-Flop

This command is executed prior to write or read of address information or word count information of the TMP82C37A. Furthermore, this command is used when low order or high order 8 bits of register are accessed.

6.10.2 Master Clear

This software command has the same effect as the hardware reset. The command, status, request, temporary, and internal First/Last flip-flop registers are all cleared by this command, and the mask register is set.

The TMP82C37A enters into the idle cycle.

6.10.3 Clear Mask Register

This command clears all mask bits of four channels, enabling acceptance of the DMA service requests. Address codes of the software command are shown in Figure 6.2.

Signal						Operation
A_3	A_2	A_1	A_0	$\overline{IOR}$	$\overline{IOW}$	
1	0	0	0	0	1	Read of status register
1	0	0	0	1	0	Write to command register
1	0	0	1	0	1	–
1	0	0	1	1	0	Write to request register
1	0	1	0	0	1	–
1	0	1	0	1	0	Bit set, reset of mask register
1	0	1	1	1	0	–
1	0	1	1	1	0	Write to mode register
1	1	0	0	0	1	–
1	1	0	0	1	0	Clear First/Last fip-flop
1	1	0	1	0	1	Read of temporary register
1	1	0	1	1	0	Master clear
1	1	1	0	0	1	–
1	1	1	0	1	0	Clear mask register
1	1	1	1	0	1	–
1	1	1	1	1	0	All bit write of mask register

050489

Note : The oblique lined codes denote illegal codes.

Figure 6.2 Register and Function Addressing

Channel	Register	Operation	Signal							(*)	Data Bus DB_0~DB_7
			$\overline{CS}$	$\overline{IOR}$	$\overline{IOW}$	A_3	A_2	A_1	A_0		
0	Base & Current Address	Write	0	1	0	0	0	0	0	0	A_0 ~ A_7
			0	1	0	0	0	0	0	1	A_8 ~ A_{15}
	Current Address	Read	0	0	1	0	0	0	0	0	A_0 ~ A_7
			0	0	1	0	0	0	0	1	A_8 ~ A_{15}
	Base & Current Address	Write	0	1	0	0	0	0	1	0	W_0 ~ W_7
			0	1	0	0	0	0	1	1	W_8 ~ W_{15}
	Current Address	Read	0	0	1	0	0	0	1	0	W_0 ~ W_7
			0	0	1	0	0	0	1	1	W_8 ~ W_{15}
1	Base & Current Address	Write	0	1	0	0	0	1	0	0	A_0 ~ A_7
			0	1	0	0	0	1	0	1	A_8 ~ A_{15}
	Current Address	Read	0	0	1	0	0	1	0	0	A_0 ~ A_7
			0	0	1	0	0	1	0	1	A_8 ~ A_{15}
	Base & Current Address	Write	0	1	0	0	0	1	1	0	W_0 ~ W_7
			0	1	0	0	0	1	1	1	W_8 ~ W_{15}
	Current Address	Read	0	0	1	0	0	1	1	0	W_0 ~ W_7
			0	0	1	0	0	1	1	1	W_8 ~ W_{15}
2	Base & Current Address	Write	0	1	0	0	1	0	0	0	A_0 ~ A_7
			0	1	0	0	1	0	0	1	A_8 ~ A_{15}
	Current Address	Read	0	0	1	0	1	0	0	0	A_0 ~ A_7
			0	0	1	0	1	0	0	1	A_8 ~ A_{15}
	Base & Current Address	Write	0	1	0	0	1	0	1	0	W_0 ~ W_7
			0	1	0	0	1	0	1	1	W_8 ~ W_{15}
	Current Address	Read	0	0	1	0	1	0	1	0	W_0 ~ W_7
			0	0	1	0	1	0	1	1	W_8 ~ W_{15}
3	Base & Current Address	Write	0	1	0	0	1	1	0	0	A_0 ~ A_7
			0	1	0	0	1	1	0	1	A_8 ~ A_{15}
	Current Address	Read	0	0	1	0	1	1	0	0	A_0 ~ A_7
			0	0	1	0	1	1	0	1	A_8 ~ A_{15}
	Base & Current Address	Write	0	1	0	0	1	1	1	0	W_0 ~ W_7
			0	1	0	0	1	1	1	1	W_8 ~ W_{15}
	Current Address	Read	0	0	1	0	1	1	1	0	W_0 ~ W_7
			0	0	1	0	1	1	1	1	W_8 ~ W_{15}

050489

(*) : Internal First/Last Flip-Flop

Figure 6.3 Word Count, Address Registers

7. PROGRAMMING

If HLDA of MPU is inactive it is possible to program the TMP82C37A by MPU even when HRQ is active.

However, it is necessary for MPU to take care that programming of the TMP82C37A and anser of HLDA are taken place simultaneously.

It requires care when the DMA service is requested to an unmasked channel during the programming of the TMP82C37A.

It is considered that an embarrassing trouble may be caused in this case.

For instance, if MPU is going to rewrite the address register of channel 2 and in addition, the TMP82C37A is enabled and channel 2 is not masked when channel 2 received a DMA request. The DMA service will be started after one byte of the address register is written. Such a problem as exampled above can be taken place.

To avoid such problems as this, it is better to disable the controller or mask unmasked channels before reprogramming any register.

It is better to enable the controller or clear the masking when the programming is completed.

Example of Program Set (CH2)

```
DI                  : Interrupt disable
OUT   MCLR          : Master clear
MVI   A,XXXXXXXXB
OUT   CMND          : Command register set-up
MVI   A,XXXXXX10B
OUT   MODE          : Mode register set-up
MVI   A,37H
OUT   ADR2          : CH2 Address Reg. (low order)
MVI   A,82H
OUT   ADR2          : CH2 Address Reg. (high order)
MVI   A,17H
OUT   WCNT2         : CH2 Word count register (low order)
MVI   A,95H
OUT   WCNT2         : CH2 Word count register (high order)
MVI   A,00000010B
OUT   MSKB          : CH2 Mask clear (signal bit)
EI                  : Interrupt enable
```

8. ELECTRIC CHARACTERISTICS

8.1 ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEMS	TEST CONDITION	RATING	UNIT
V_{CC}	Supply Voltage	With Respect To GND.	− 0.5 to + 7.0	V
V_{IN}	Input Voltage		− 0.5 to V_{CC} + 0.5	V
V_{OUT}	Output Voltage		− 0.5 to V_{CC} + 0.5	V
PD	Power Dissipation	−	250	mW
T_{sol}	Soder Temperature	−	260 (10sec)	°C
T_{stg}	Strage Temperature	−	− 65 to + 150	°C
T_{opr}	Operating Temperature	−	− 40 to + 85	°C

050489

8.2 DC CHARACTERISTICS

Ta = − 40°C to + 85°C, VCC = 5V ± 10%, VSS (GND) = 0V

SYMBOL	ITEMS	CONDTION	MIN.	TYP.	MAX.	UNIT
V_{IL}	Input Low Voltage		− 0.5	−	0.8	V
V_{IH}	Input High Voltage		2.2	−	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 3.2mA	−	−	0.45	V
V_{OH1}	Output High Voltage	I_{OH1} = − 400μA	2.4	−	−	V
V_{OH2}	Output High Voltage	I_{OH2} = − 100μA	V_{CC} − 0.8	−	−	V
I_{IL}	Input Leak Current	$0V \leqq V_{IN} \leqq V_{CC}$	−	−	± 10	μA
I_{OFL}	Output Leak Current	$0.45V \leqq V_{OUT} \leqq V_{CC}$	−	−	± 10	μA
I_{CC1}	Operating Supply Current	CLK = 5MHz $V_{IH} = V_{CC} - 0.2V$ V_{IL} = 0.2V	−	−	10	mA
I_{CC2}	Stand-by Supply Current	CLK = DC $V_{IH} = V_{CC} - 0.2V$ V_{IL} = 0.2V	−	−	10	μA

050489

8.3 AC CHARACTERISTICS

8.3.1 Active Cycle (Notes : 2 and 9)

Ta = −40°C to +85°C, V_{CC} = 5V ± 10%, V_{SS} (GND) = 0V (1/2)

SYMBOL	PARAMETER		MIN.	MAX.	UNIT
T_{AEL}	AEN HIGH from CLK LOW (S1) Delay time		–	200	ns
T_{AET}	AEN LOW from CLK HIGH (SI) Delay time		–	130	ns
T_{AFAB}	ADR Active to Float Delay from CLK HIGH		–	90	ns
T_{AFC}	$\overline{READ}$ or $\overline{WRITE}$ Float Delay from CLK HIGH		–	120	ns
T_{AFDB}	DB Active to Float Delay from CLK HIGH		–	170	ns
T_{AHR}	ADR from $\overline{READ}$ HIGH Hold Time		TCY-100	–	ns
T_{AHS}	DB from ADSTB LOW Hold Time		30	–	ns
T_{AHW}	ADR from $\overline{WRITE}$ HIGH Hold Time		TCY-50	–	ns
T_{AK}	DACK Valid from CLK LOW Delay Time		–	170	ns
	$\overline{EOP}$ HIGH from CLK HIGH Delay Time		–	170	ns
	$\overline{EOP}$ LOW from CLK HIGH Delay Time		–	170	ns
T_{ASM}	ADR Stable from CLK HIGH		–	170	ns
T_{ASS}	DB to ADSTB LOW Setup Time		100	–	ns
T_{CH}	Clock HIGH Level Width		68	–	ns
* T_{CL}	Clock LOW Level Width		100	–	ns
T_{CY}	Clock Cycle Time		200	–	ns
T_{DCL}	CLK HIGH to $\overline{READ}$ or $\overline{WRITE}$ LOW Delay Time	(NOTE 3)	–	190	ns
T_{DCTR}	$\overline{READ}$ HIGH from CLK HIGH (S4) Delay Time	(NOTE 3)	–	190	ns
T_{DCTW}	$\overline{WRITE}$ HIGH from CLK HIGH (S4) Delay Time	(NOTE 3)	–	130	ns
T_{DQ1}	HRQ Valid from CLK HIGH Delay Time	(NOTE 4)	–	120	ns
* T_{DQ2}			–	140	ns
T_{EPS}	$\overline{EOP}$ Low from CLK LOW Setup Time		40	–	ns
T_{EPW}	$\overline{EOP}$ pulse width		220	–	ns
T_{FAAB}	DB Float to Active Dilay from CLK HIGH		–	170	ns
T_{FAC}	$\overline{READ}$ or $\overline{WRITE}$ Active from CLK HIGH		–	150	ns
T_{FADB}	DB Float to Active Dilay from CLK HIGH		–	200	ns
T_{HS}	HLDA Valid to CLK HIGH Setup Time		75	–	ns
T_{IDH}	Input Data from $\overline{MEMR}$ HIGH Hold Time		0	–	ns
T_{IDS}	Input Data to $\overline{MEMR}$ HIGH Setup Time		170	–	ns
T_{ODH}	Output Data from $\overline{MEMW}$ HIGH Hold Time		10	–	ns
T_{ODV}	Output Data Valid to $\overline{MEMW}$ HIGH		125	–	ns
* T_{QS}	DREQ to CLK LOW (SI, S4) Setup Time		30	–	ns
T_{RH}	CLK to READY LOW Hold Time		20	–	ns

050489

Ta = −40°C to +85°C, V_{CC} = 5V ± 10%, V_{SS} (GND) = 0V (2/2)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
T_{RS}	READY to CLK LOW Setup Time	60	–	ns
T_{STL}	ADSTB HIGH from CLK HIGH Delay Time	–	130	ns
T_{STT}	ADSTB LOW from CLK HIGH Delay Time	–	90	ns

050489

Note 1 : TCL and TDQ2.
The following AC specification can be also guaranteed under the conditions
: Ta = −40°C to 50°C
Vcc = 5V + 5%
Vss = 0V

Note 2 : Value with * is different from AC specification of N-MOS part.

8.3.2 Program Condition (Idle Cycle) (Notes : 2, 8 and 9)

Ta = −40°C to +85°C, V_{CC} = 5V ± 10%, V_{SS} (GND) = 0V

SYMBOL	ITEM	MIN.	MAX.	UNIT
T_{AR}	ADR Valid or $\overline{CS}$ LOW to $\overline{READ}$ LOW	50	–	ns
T_{AW}	ADR Valid or $\overline{WRITE}$ HIGH Setup Time	130	–	ns
T_{CW}	$\overline{CS}$ LOW to $\overline{WRITE}$ HIGH Setup Time	130	–	ns
T_{DW}	Data Valid to $\overline{WRITE}$ HIGH Setup Time	130	–	ns
T_{RA}	ADR or $\overline{CS}$ Hold from $\overline{READ}$ HIGH	0	–	ns
T_{RDE}	Data Access from $\overline{READ}$ LOW (Note 7)	–	140	ns
T_{RDF}	Data Bus Float Delay from $\overline{READ}$ HIGH	0	70	ns
T_{RSTD}	Power Supply HIGH to RESET LOW Setup Time	500	–	ns
T_{RSTS}	RESET to First $\overline{IOWR}$	2	–	TCY
T_{RSTW}	RESET pulse width	300	–	ns
T_{RW}	$\overline{READ}$ pulse width	200	–	ns
T_{WA}	ADR from $\overline{WRITE}$ HIGH Hold Time	20	–	ns
T_{WC}	$\overline{CS}$ HIGH from $\overline{WRITE}$ HIGH Hold Time	20	–	ns
T_{WD}	Data from $\overline{WRITE}$ HIGH Hold Time	30	–	ns
T_{WWS}	$\overline{WRITE}$ pulse width	160	–	ns

050489

Capacity Ta = 25°C, V_{CC} = GND = 0V

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_O	Output Capacitance	f_C = 1.0MHz, Input = 0V	–	–	8	pF
C_I	Input Capacitance		–	–	15	
$C_{I/O}$	I/O Capacitance		–	–	20	

050489

Note 1. TYP. value is that when rated voltage is applied at Ta = 25°C.

Note 2. Test conditions; a) Unless otherwise specified, timing defining signal voltage are;
Input High level = 2.4V, Low level = 0.45V
Output High level = 2.2V, Low level = 0.8V
b) Input rising and falling times are below 20ns.
c) Unless otherwise spesified, 1×TTL gate and 150 pF load are provided to output.

Note 3. Normal write pulse width is TCY-100 ns. Extension write pulse width is 2TCY-100 ns. Read pulse width is 2TCY-50 ns, and compressed read pulse width is TCY-50 ns.

Note 4. TDQ is measured at two different high levels.
TDQ1 = 2.2V, TDQ2 = 3.3V.

Note 5. It is necessary to keep DREQ active until DACK is received.

Note 6. Both low active and high active level are available for DREQ and DACK.

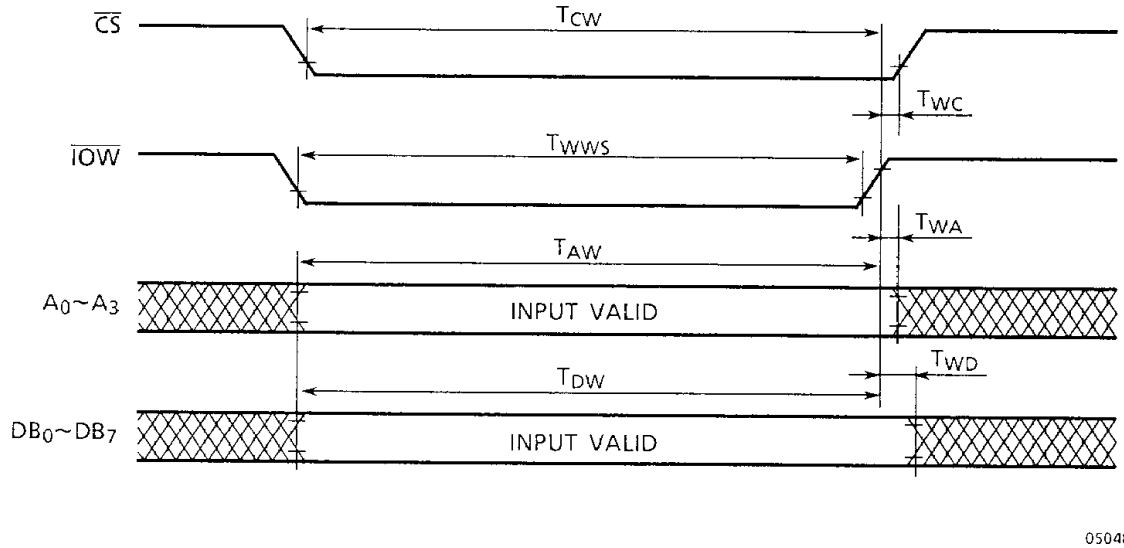
Note 7. Output load of the data bus are provided with 1 ×TTL gate and 15 pf as the minimum value, and 1×TTL gate and 150 pF as the maximum value.

Note 8. Sucessive read or/and write operations by the MPU to program must be timed to allow at least 400ns as recovery time between active read or write pulses.

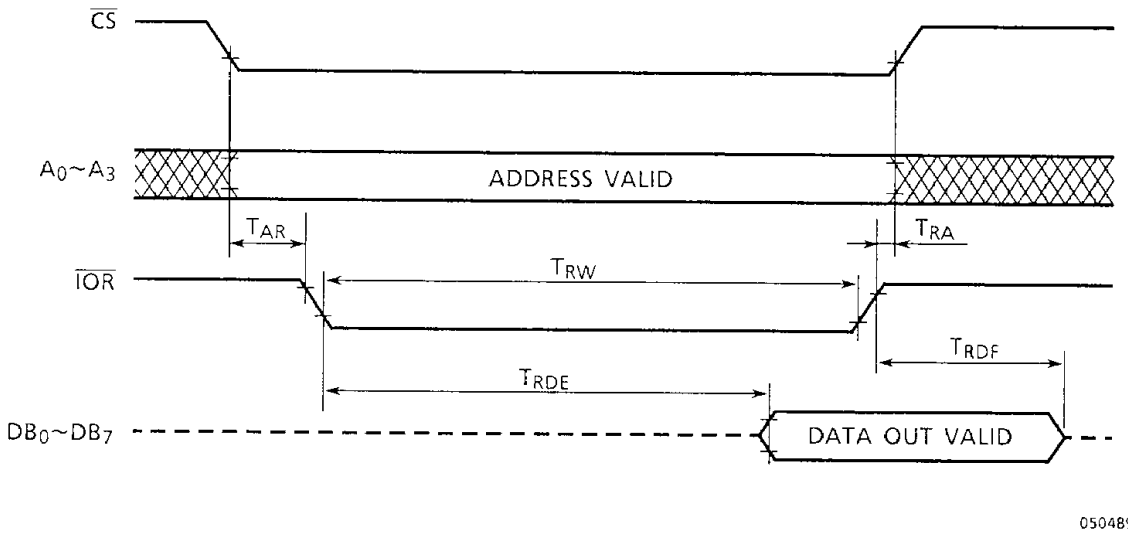
Note 9. Signal $\overline{\text{READ}}$ and $\overline{\text{WRITE}}$ are $\overline{\text{IOR}}$ and $\overline{\text{MEMW}}$ for the DMA operations from peripheral devices to the memory. In the DMA operations from the memory to peripheral devices, they are $\overline{\text{MEMR}}$ and $\overline{\text{IOW}}$.

Note 10. When N state wait is added at time of write to memory in the latter half memory-to-memory transfer, this parameter increases by N (TCY) at a time.

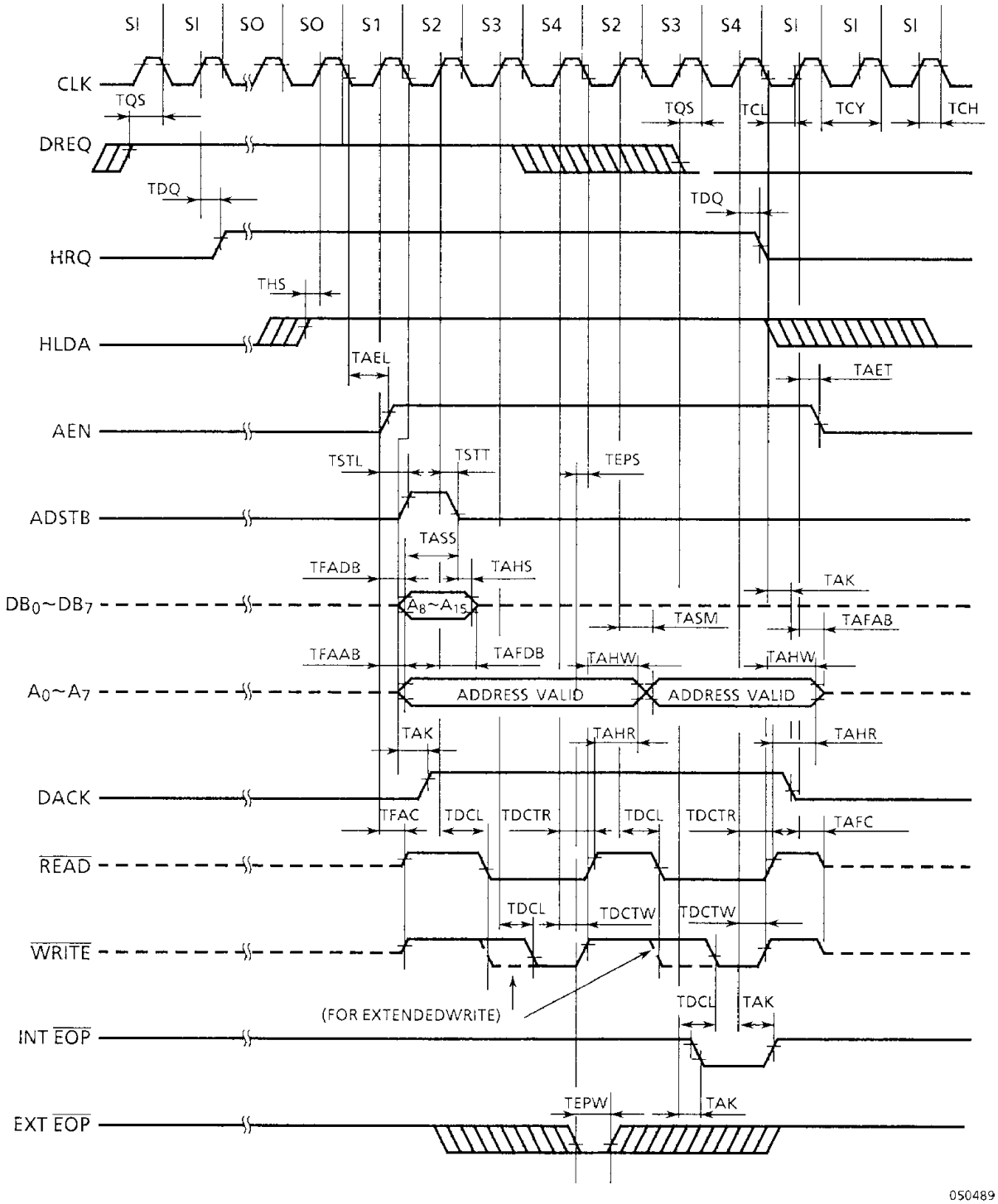
9. TIMING DIAGRAM



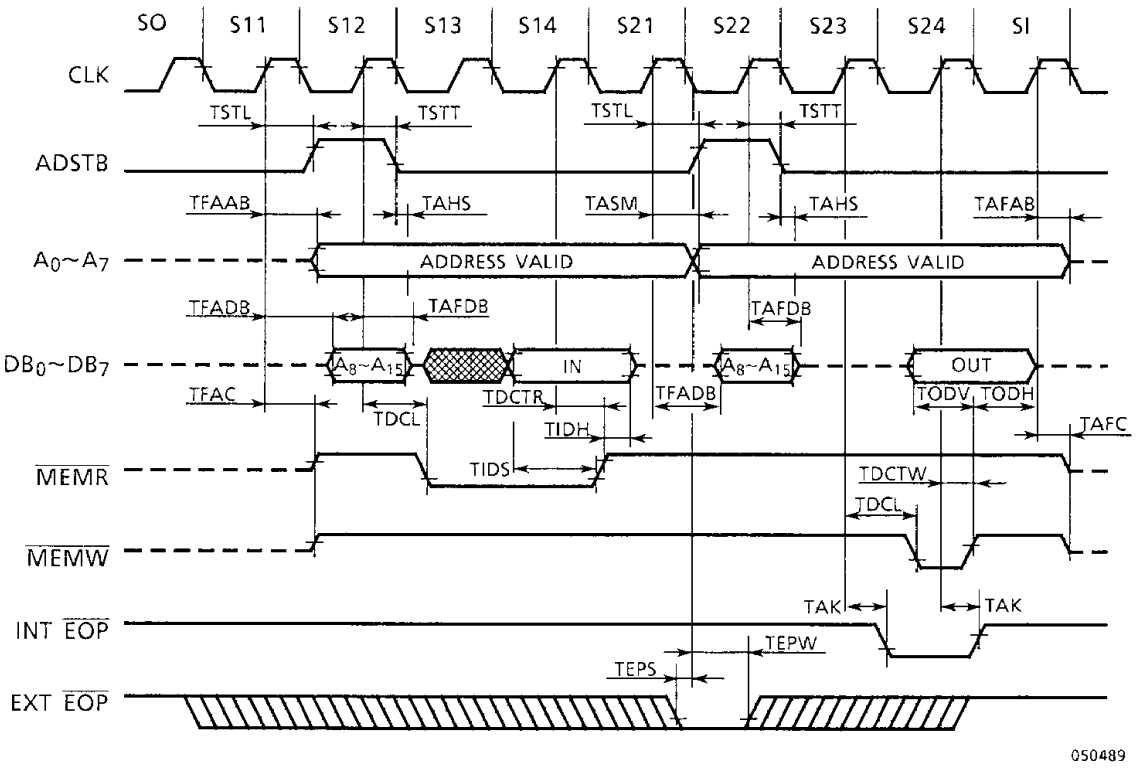
Timing Diagram 1 Program Condition Write Timing



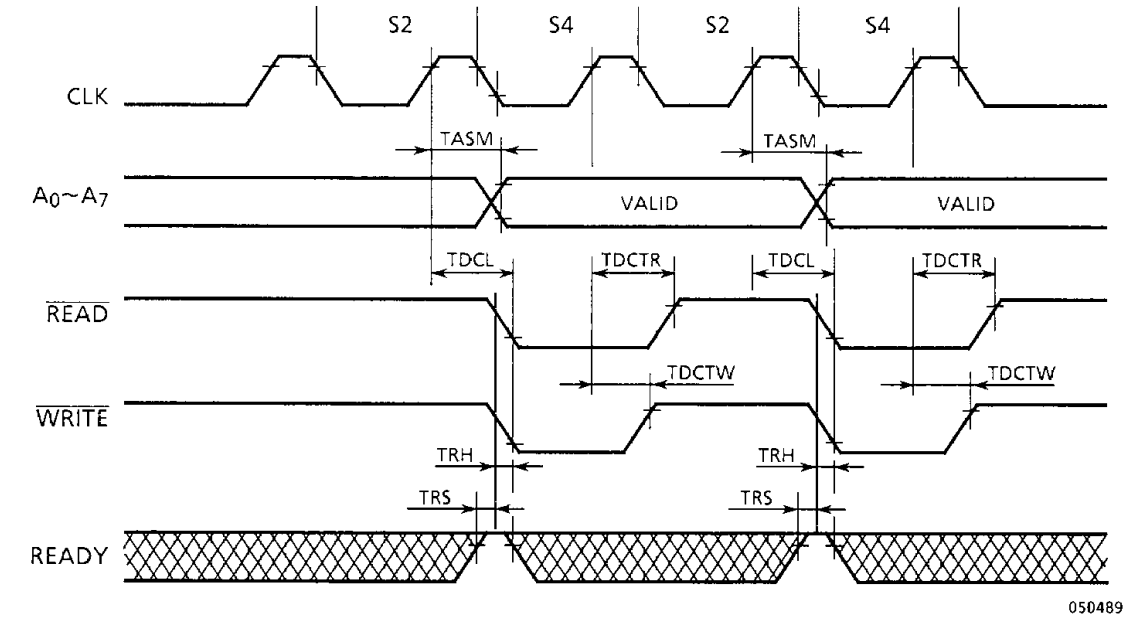
Timing Diagram 2 Program Condition Read Cycle



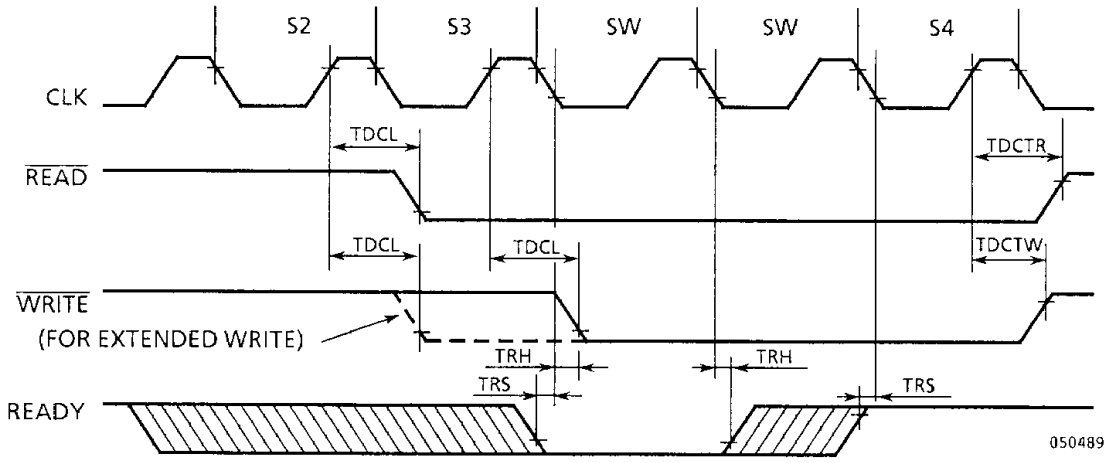
Timing Diagram 3 Active Cycle



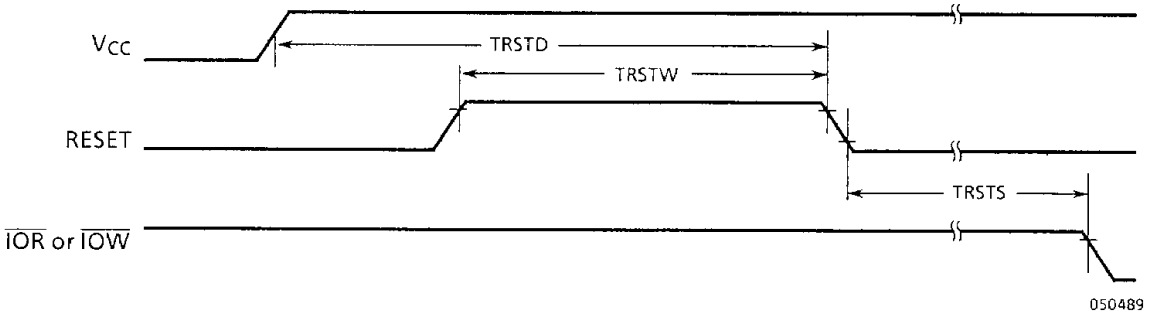
Timing Diagram 4 Memory-to-Memory Transfer



Timing Diagram 5 Compressed Transfer



Timing Diagram 6 Ready Timing



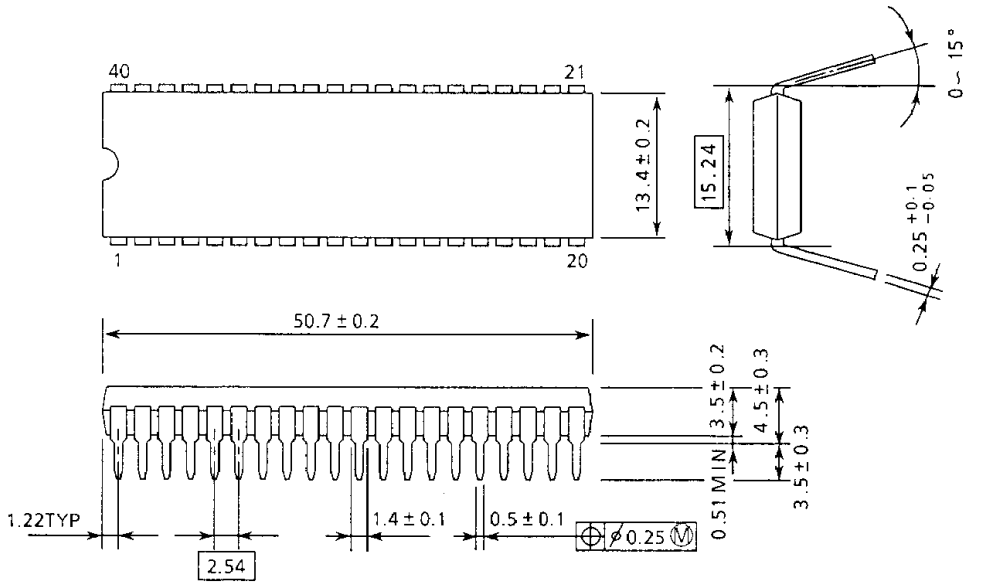
Timing Diagram 7 Reset Timing

10. EXTERNAL DIMENSION

10.1 40PIN DIP EXTERNAL DIMENSION

DIP40-P-600

Unit : mm



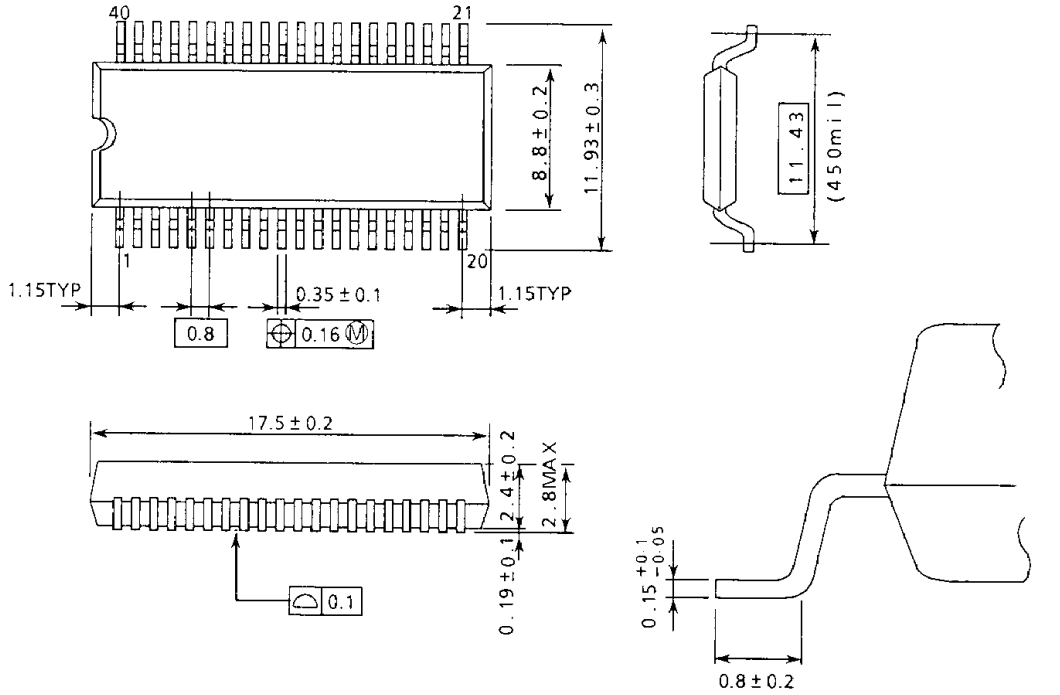
270289

Note : Each pitch is 2.54mm, and all the leads are located within ±0.25mm from their theoretical positions with respect to No. 1 and No. 40 leads.

10.2 40PIN SOP EXTERNAL DEMENSION

SSOP40-P-450

Unit : mm



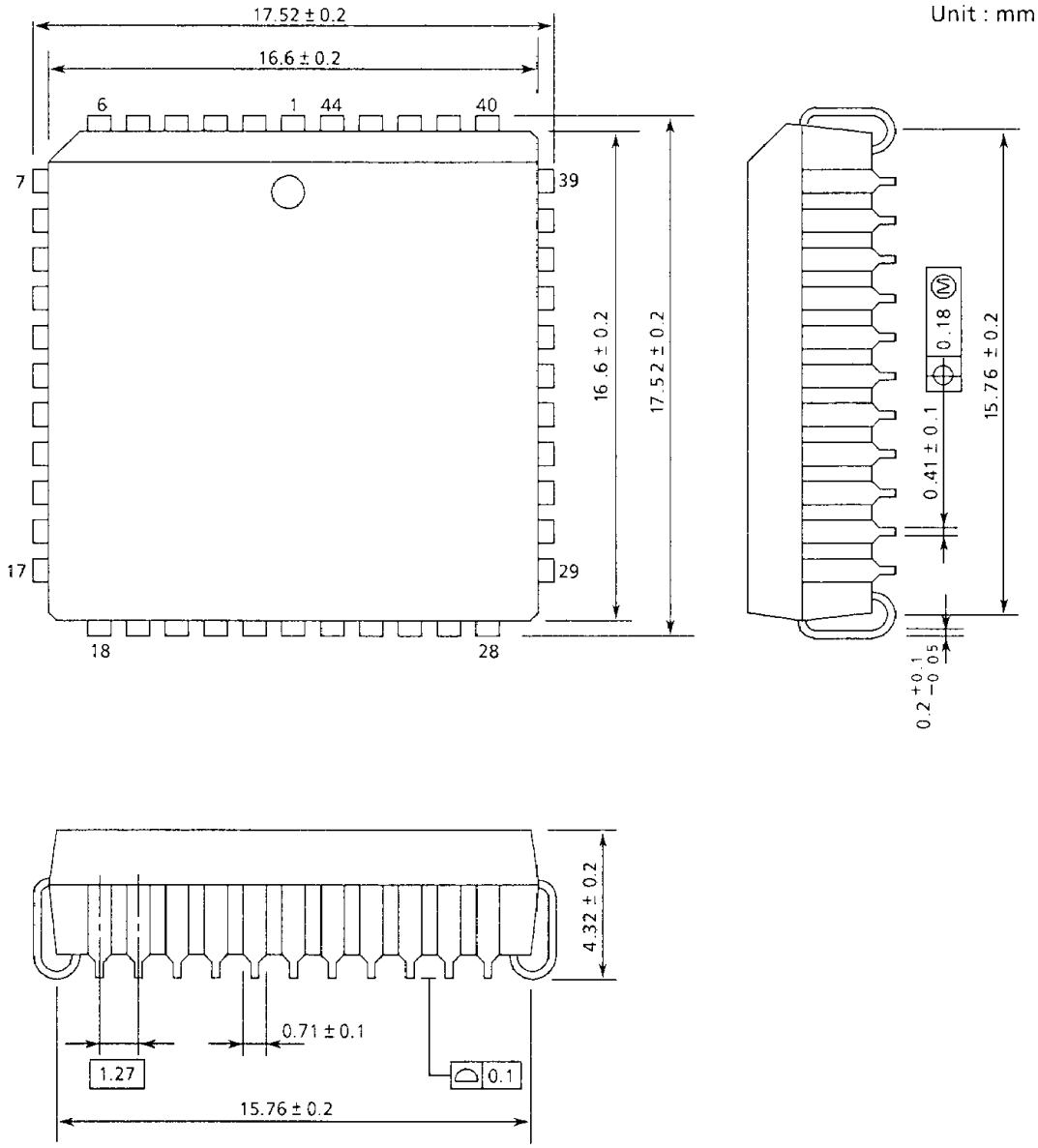
270289

Note : Package Width and Length do not include Mold Protrusions.
Allowable Mold Protrusion is 0.15mm.

10.3 44PIN PLCC EXTERNAL DEMENSION

QFJ44-P-S650

Unit : mm



270289

11. EXAMPLE OF APPLICATION CIRCUIT

The connecting method of the TMP82C37A and MPU is shown in Figure 11.1.

The multimode DMA controller outputs a hold request whenever valid DMA request is produced from peripheral device. When MPU answers by the hold acknowledge signal, the TMP82C37A receives the control right of the address bus, data bus, and control bus. In the first transfer, address (the least significant 8 bits of the address bits and the most significant 8 bits on the data bus) is output.

The content of the data bus is latched by the 8-bit latch (TC74HC373P) to make the address bus complete. After execution of the first transfer, that latched data is updated only when carry or borrow is produced on the least significant address byte. When one TMP82C37A is used, four DMA channels are provided.

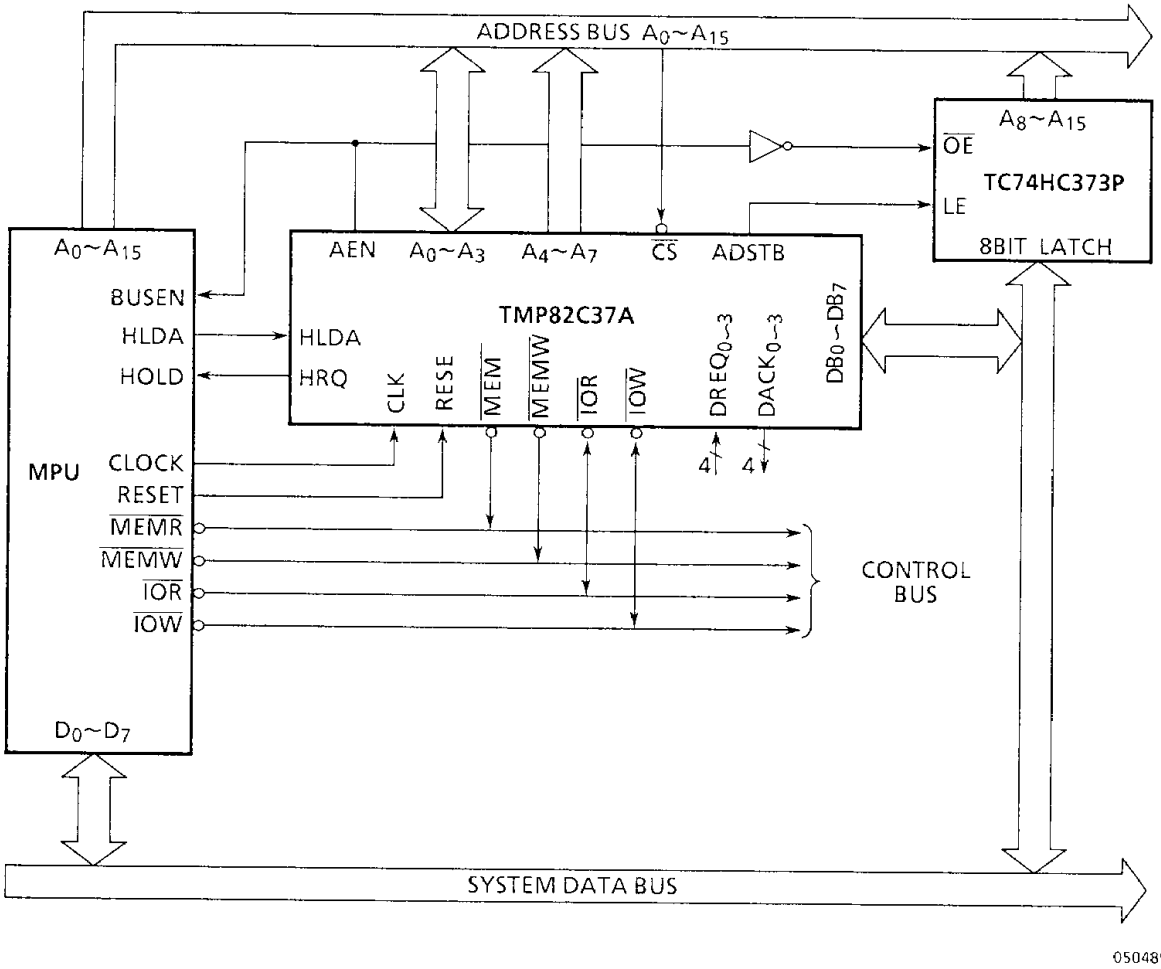


Figure 11.1 Basic System Connection Diagram

Figure 11.2 shows the expansion method for number of DMA channels. It is possible to realize net 7 DMA channels by connecting the second TMP82C37A to one of the DMA channels of the first TMP82C37A.

Two DMA chips commonly use the same 8-bit latch. Thus, any channel is used for expansion.

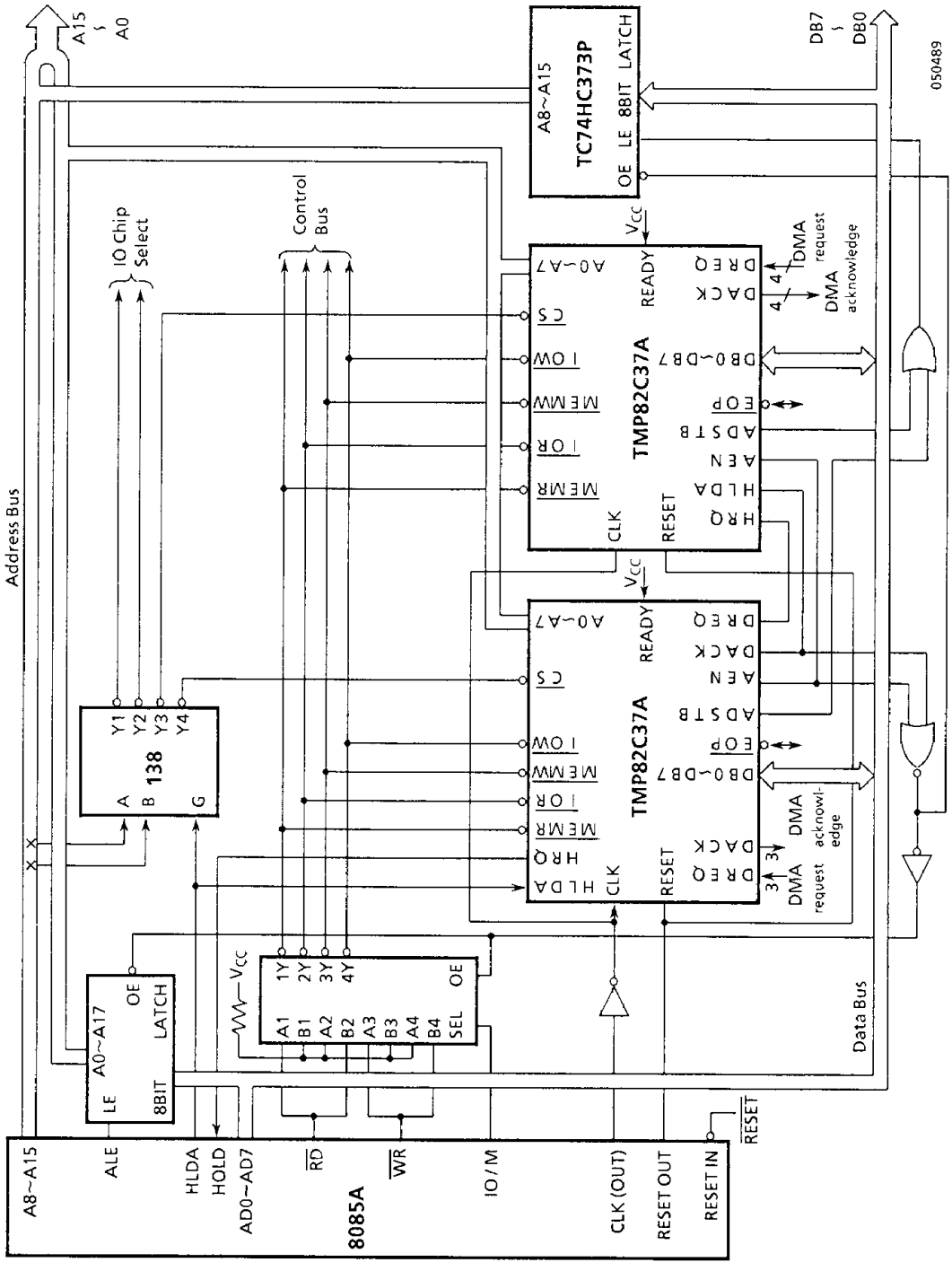


Figure 11.2 Expansion of TMP82C37A

MULTIMODE DMA CONTROLLER
TMP8237AP-5

1. GENERAL DESCRIPTION

The TMP8237AP-5 (hereinafter referred to as TMP8237A) is a multimode direct memory access (DMA) controller. The TMP8237A improves the system function by directly transferring information between the system memory and external devices. Memory-to-Memory data transfer capability is also provided.

The TMP8237A is provided with versatile programmable control functions in order to improve data throughput.

The TMP8237A is used with an 8-bit address register connected externally.
The TMP8237A has four built-in independent channels and it is possible to expand channels through cascade connection.

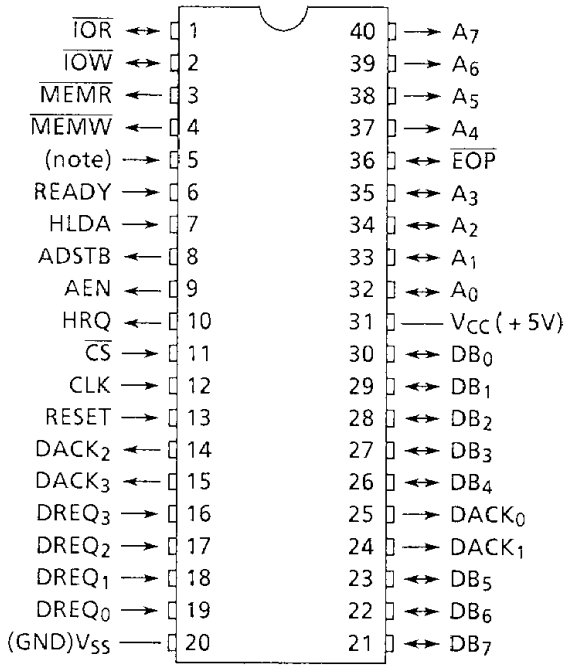
There are three basic data transfer modes which are programmable by the user. Each channel is programmable individually and autoinitialization is possible by End of Process ($\overline{EOP}$) signal.

Each channel has the maximum 64K capability for both address and word count. $\overline{EOP}$ signal is capable of terminating data transfer between DMA and memories. $\overline{EOP}$ signal is useful for block search or verify or for terminating erroneous service.

2. FEATURES

- Four independent DMA channels
- Three transfer modes; block, demand, and single transfer modes
- Independent auto initialize function provided to each of all channels
- Memory-to-Memory transfer
- Address increment or decrement
- All DMA request disabled by disabling the master system
- Individual DMA request enable/disable control
- Unrestricted channel expansion by cascade connection
- End of Process ($\overline{EOP}$) input for terminating transfer
- Software DMA Request
- Polarity control provided for DREQ signal and DACK signal
- Option for increasing transfer speed up to 2.5M word/sec
- Single +5V power supply

3. PIN CONNECTIONS (TOP VIEW)



Note : PIN 5 must be connected to VCC or opened

050489

Figure 3.1 Pin Connections

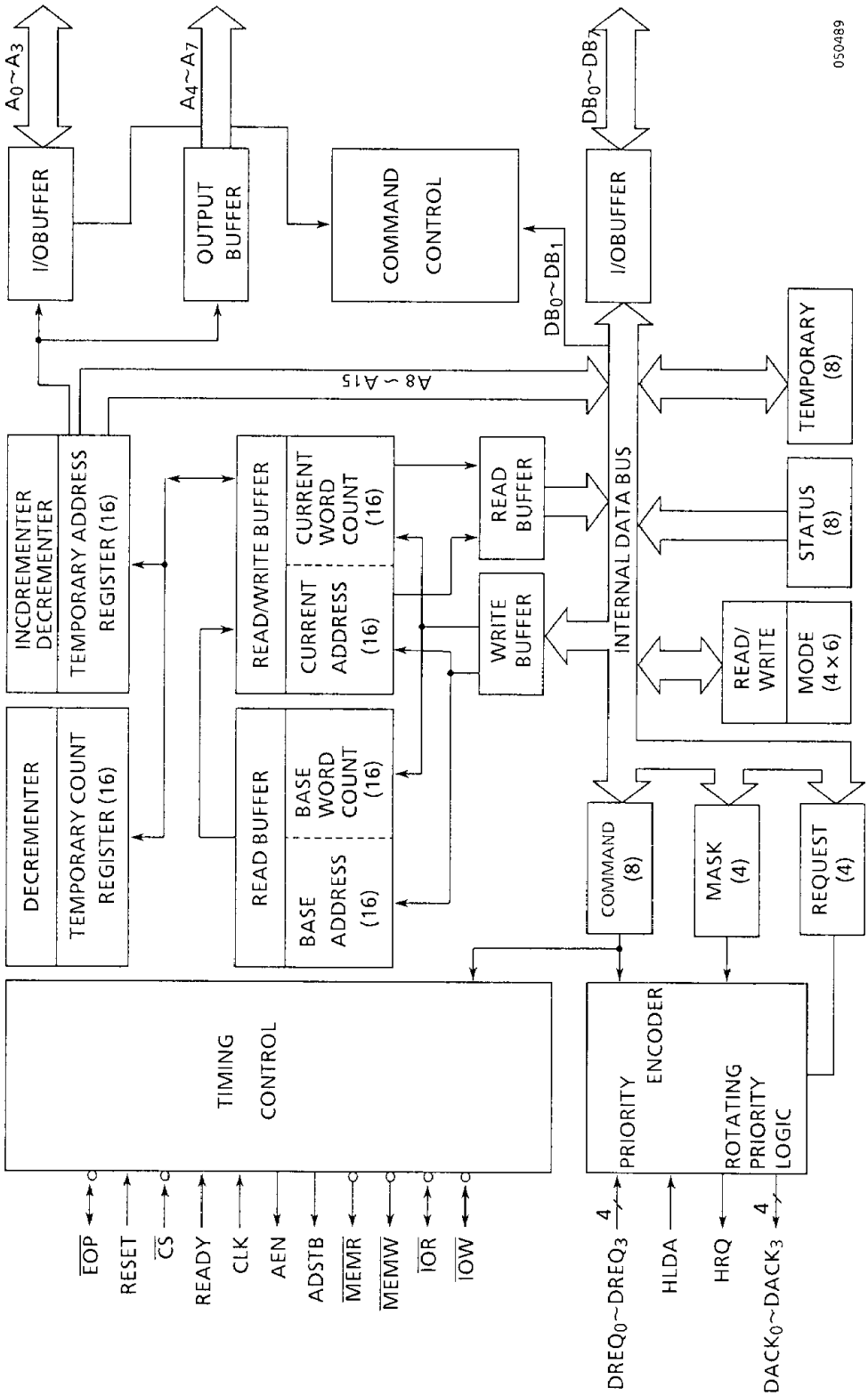


Figure 3.2 Block Diagram of TMP8237A

4. PIN NAME & FUNCTION

- VCC

  +5V power supply

- VSS

  Ground

- CLK (Clock, Input)

  This input controls the internal operation and data transfer rate of the TMP8237A.

- $\overline{CS}$ (Chip Select, Input)

  This input is low active and used to select the TMP8237A as an I/O device during an I/O read or I/O write by the host MPU. If $\overline{IOR}$ or $\overline{IOW}$ is toggled following each transfer when a host MPU and the TMP8237A are transferring data mutually, $\overline{CS}$ may be kept at low.

- RESET (Reset, Input)

  This input is asynchronous input to clear the command, status, request and temporary registers. In addition, this input is used to clear First/Last flip-flops and set the mask register. Following the reset, the TMP8237A is placed in the idle cycle.

- READY (Ready, Input)

  This input is used to extend the memory or I/O read and write pulses in DMA cycle in order to adapt to low speed memories or I/O peripheral devices.

- HLDA (Hold Acknowledge, Input)

  By this signal, the TMP8237A knows that the system bus control is turned over from MPU.

- $DREQ_0$-$DREQ_3$ (DMA Request, Input)

  DMA request signals are input from peripheral circuits. If priority is fixed, the highest priority is given to $DREQ_0$ and the lowest priority to $DREQ_3$. Polarity of DREQ is programmable. DREQ becomes high active by RESET.

- DB_0-DB_7 (Data Bus, Input/Output)

  The data bus are bidirectional 3-state lines connected to the system data bus. During MPU is in I/O read state, output is enabled and contents of the registers (address, status, temporary and word count) are output to MPU. During MPU is in I/O read state, the data bus serves as input and it becomes possible to program the control register of the TMP8237A.

  During the DMA cycle, the most significant 8 bits of address are output on the data bus and latched by ADSTB signal externally. During the Memory-to-Memory transfer, the data of the source memory location are loaded into the temporary register of the TMP8237A by the read operation and the contents of the temporary register are output to the destination memory location by the write operation.

- $\overline{IOR}$ (I/O Read, Input/Output)

  I/O read is a bidirectional, low active and 3-state signal. During the idle cycle, this signal serves as an input control signal used by MPU to read the control registers of the TMP8237A. During the active cycle, this signal serves as an output control signal used by the TMP8237A to access data from the peripheral circuit during the DMA read and transfer.

- $\overline{IOW}$ (I/O Write, Input/Output)

  I/O write is a bidirectional, low active, 3-state signal. During the idle cycle, this signal serves as an input control signal used by MPU to load the information to the TMP8237A. During the active cycle, this signal served as an output control signal used by TMP8237A to load the data to the peripheral. For write to the TMP8237A by MPU, the leading edge of the write signal ($\overline{IOW}$) is required for every data transfer. It is not possible to write more than two data by toggling $\overline{CS}$ while holding the $\overline{IOW}$ pin at low level.

- $\overline{EOP}$ (End of Process, Input/Ouptut)

  $\overline{EOP}$ (End of Process) is a signal relative to the end of DMA service, and is a low active, bidirectional and open drain signal. When the channel word count reaches from 0000H to FFFFH, the TMP8237A output low pulse of $\overline{EOP}$ to peripheral devices as the end signal.

  In addition, it is also possible to pull $\overline{EOP}$ to the low level by peripheral device in order to cause the end of process.

  When $\overline{EOP}$ is received (internally or externally), the channel which is presently active terminates the service, sets that TC bit of the status register and resets that request bit.

  If that channel is programmed for auto initialization, that current register is updated from the base register. In all other cases, mask bit is set and the content of that register remains unchanged.

During the Memory-to-Memory transfer, $\overline{EOP}$ is output when TC of channel 1 is produced. $\overline{EOP}$ is always used for channels with active DACK and external $\overline{EOP}$ has no connection when $DACK_0$-$DACK_3$ are all inactive.

$\overline{EOP}$ is an open drain signal and therefore, requires an external pull-up resistor.

- A_0-A_3 (Address, Input/Output)

  The four least significant address lines are the bidirectional 3-state signals. In the idle cycle, these lines serve as the input signals and used by MPU for write/read of the control register. In the active cycle, they serve as the output signals and become low order 4 bits of output address.

- A_4-A_7 (Address, Output)

  The four most significant address lines are 3-state output signals.
  These lines are enabled for the period of DMA service only.

- HRQ (Hold Request, Output)

  This is the hold request signal to MPU, and is used to request the system bus control. HRQ is output by the TMP8237A according to a software request or unmasked DREQ.

- $DACK_0$-$DACK_3$ (DMA Acknowledge, Output)

  The DMA acknowledge lines indicate that channels are active. Normally, these are used for selecting peripheral devices.

  Only one DACK becomes active but it does not become active unless DMA is controlling the system bus. Polarity of these lines are programmable. After reset, they initialize low active.

- AEN (Address Enable, Output)

  Address Enable is a high active signal and used to enable output of the external latch which holds high order byte of address and to disable the system bus during the DMA cycle.

  During the DMA transfer, HLDA and AEN are used to disable all I/O except programmed I/O. The TMP8237A disables $\overline{CS}$ input for DMA transfer to prevent itself from being selected automatically.

- ADSTB (Address Strobe, Output)

  This signal is a strobe output to an external latch circuit and is used to latch high order 8-bit address from DB_0-DB_7.

- $\overline{\text{MEMR}}$ (Memory Read, Output)

  This is a low active 3-state output used for transferring data from a memory to a peripheral device or for data accessing from a selected memory during the Memory-to-Memory transfer.

- $\overline{\text{MEMW}}$ (Memory Write, Output)

  This is a low active 3-state output used for transferring data from a peripheral device to a memory or for writing data into a selected memory during the Memory-to-Memory transfer.

5. OPERATIONAL DESCRIPTION

5.1 DMA OPERATION

The TMP8237A has two operations; idle cycle and active cycle. Each of these cycles consists of several states.

On the TMP8237A, it is possible to consider 7 states each of which consists of one clock cycle. State I (SI) is an idle state. This is such a state as there is no valid DMA request pending. SI is a program condition state which is programmable by MPU.

State 0 (S0) is the first DMA service state. This is a state that the TMP8237A made a hold request to MPU but not yet received the acknowledge signal from MPU. When the acknowledge signal is received from MPU, the transfer is started.

S1, S2, S3 and S4 are the DMA service states. If more time is required by the transfer, it is possible to insert the wait state (SW) before S4 by READY input to the TMP8237A.

In the Memory-to-Memory transfer, in order to assure complete transfer, read from the memory and write to the memory are required. 8 states are necessary for one transfer. The first four status (S11, S12, S13 and S14) are read from the memory and the latter four state (S21, S22, S23 and S24) are write to the memory.

The temporary data register is used as an intermediate storage area of memory bytes.

5.2 IDLE CYCLE

When DMA service is not requested by channels, the TMP8237A enters into the idle cycle and is placed in SI state. In order to check if the channels request DMA service, the TMP8237A samples DREQ for every clock.

The TMP8237A also samples $\overline{CS}$ to check if MPU is requesting read or write of internal registers. When $\overline{CS}$ is low and HLDA is also low, the TMP8237A is placed in the program condition.

At this time, MPU is able to change or check the content of any internal register through read or write from that register.

Address lines A_0-A_3 are input signals and used for selecting a register being read or written. $\overline{IOR}$ and $\overline{IOW}$ are used for selecting read or write and decide read/write timing.

The internal flip-flop is used for generating address extension bits according to number and size of internal registers. (First/Last flip-flop) This bit is used for deciding high or low order byte of 16-bit address and word count register.

The flip-flop is reset by the master clear or reset. In addition, this flip-flop also can be reset by an idependent software command.

On a special software command, the execution in the TMP8237A program condition is possible. These commands are decoded as in the address setting when both $\overline{CS}$ and $\overline{IOW}$ are active.

The data bus is not used for this command. This command is available in three types; clear First/Last flip-flop , master clear and clear mask register.

5.3 ACTIVE CYCLE

When the TMP8237A is in the idle cycle and the channels are requesting DMA service, the TMP8237A outputs HRQ to MPU and goes into the active cycle. In this cycle, the DMA service for any one of 4 modes is executed.

5.3.1 Single Transfer Mode:

In this mode, the TMP8237A performs a single byte transfer during each HRQ/HLDA handshake. When DREQ becomes active, HRQ becomes active.

After MPU responds by driving HLDA active, a single byte transfer will take place. After the transfer HRQ becomes inactive, its word count is decreased, and address is increased or decreased. When word count changes from 0000H to FFFFH, a terminal signal is generated and if the channels are programmed, the auto initialization is made.

To execute the single byte transfer, it is necessary to hold DREQ until DACK corresponding each DREQ becomes active. If DREQ is continuously active, HRQ becomes inactive following each transfer and then, becomes active again, and the new single byte is executed following the leading edge of HLDA.

On the 8085A system, one machine cycle can be executed during the DMA transfer.

5.3.2 Block Transfer Mode:

In this mode the TMP8237A continues the transfer until terminal count (TC) is generated or an external End of Process signal ($\overline{EOP}$) is encountered. Here, TC is produced when the word count changes from 0000H to FFFFH.

What is requied for DREQ is to hold it in active state until DACK becomes active. Auto initialization (if so programmed) is taken place at the end of DMA service.

5.3.3 Demand Transfer Mode:

In this mode the TMP8237A continues the transfer until TC is produced or $\overline{EOP}$ is or DREQ becomes inactive. Thus, it is possible for a device, which is requesting the DMA service, to suspend the transfer by making DREQ inactive. The service is resumed when DREQ is made active again. It is possible to read an intermediate value of address and word count from the current address and current word count register of the TMP8237A while the system bus is returned to MPU during execution of the DMA service.

The auto initialization is taken place following TC or $\overline{EOP}$ at the end of DMA service. In order to perform a new DMA service following the auto initialization, the active edge of DREQ is necessary.

5.3.4 Cascade Mode:

This mode is used when the TMP8237A is cascade connected for a simple system expansion. HRQ and HLDA of the additional TMP8237A are connected to DREQ and DACK of the first TMP8237A. DMA request to the TMP8237A which is added for the purpose of system expansion is authorized by the priority circuit of the first TMP8237A.

If the priority is already decided, the additional device must wait till the acknowledge request. The cascade channel of the first TMP8237A is used only for deciding priority of the additional TMP8237A and therefore, the channel itself does not output address nor control signal. This is to prevent the added device from colliding with output of the cascade channel. On the TMP8237A, DACK respond to DREQ.

However all other outputs except HRQ are disabled.

The state of cascade connection is shown in Figure 5.1. In Figure 5.1, two levels of DMA are formed. To further expand the TMP8237A, it is possible to add it to the second level using the remaining channel of the first TMP8237A. To further add another TMP8237A, the third level can be formed by cascade connecting it to the second level.

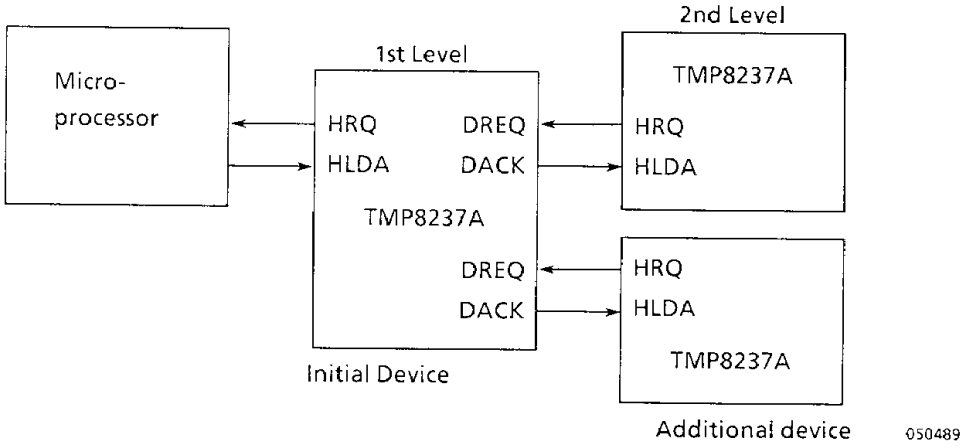


Figure 5.1 Example of Cascade Connection of TMP8237A

5.4 TRANSFER FORMAT

3 different transfer format are available for 3 active transfer modes.

They are read, write and verify. In the write transfer, data is transferred from I/O device to memory by $\overline{\text{MEMW}}$ and $\overline{\text{IOR}}$. In the read transfer, data is transferred from memory to I/O device by $\overline{\text{MEMR}}$ and $\overline{\text{IOW}}$.

The verify transfer is a pseudo transfer. The TMP82C37A perform such operations as address generation for read or write transfer, answer to $\overline{\text{EOP}}$, etc. However, memory or I/O control line does not become active.

5.5 MEMORY-TO-MEMORY TRANSFER:

The TMP8237A has the ability of block movement and is capable of transferring data block from one memory address location to another location. When Bit 0 of the command register is programmed at Logic 1, Channel 0 and 1 operate as the Memory-to-Memory transfer channels.

Channel 0 serves as a source address and Channel 1 as a destination address, and the word count of Channel 1 is used. The Memory-to-Memory transfer is executed when software DMA request is set for Channel 0.

The Memory-to-Memory transfer must use the block transfer mode.

When Channel 0 is programmed as a fixed source address, it is possible to write single source words into a memory block.

When the TMP8237A is programmed for the Memory-to-Memory transfer, Channel 0 and Channel 1 must be masked. The same value as that is set for Channel 1 must be set for the word count of Channel 0. During the Memory-to-Memory transfer, AEN became active but DACK does not become active.

During the Memory-to-Memory trnasfer, the TMP8237A respond to external $\overline{EOP}$ signal. In the block search, the data comparator uses this ($\overline{EOP}$) input to terminate the DMA service when match is found. The Memory-to-Memory transfer timing is shown in Timing Diagram 4.

5.6 AUTO INITIALIZATION:

When Bit 4 of the mode register is set to 1, the channels are set up for the auto initialization. During the auto initialization, data are loaded into the current address and current word count registers from the base address and base word count registers, respectively, following $\overline{EOP}$. The base registers are loaded by MPU simultaneously with the current registers and remain unchanged during the DMA service.

When the channels are under the auto initialization, mask bit is not set by $\overline{EOP}$.

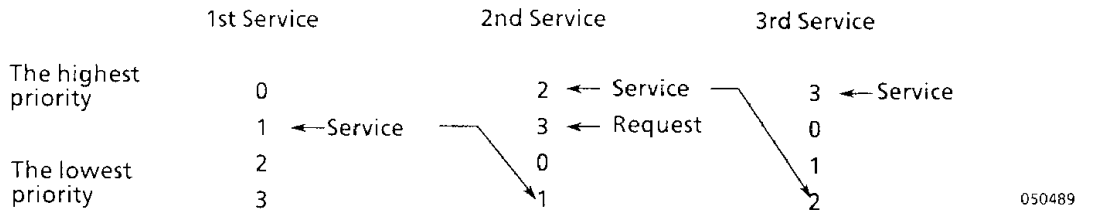
Following the auto initialization, that channel is prepared to execute the service without interposition of MPU.

5.7 PRIORITY:

The TMP8237A has two types of priority which can be selected by software. The first type is the fixed priority. Channel priority is fixed by channel number. The lowest priority is channel 3, followed by 2, 1, and the highest priority is channel 0.

The second type is the rotating priority. In this type, an accepted channels is then given with the lowest priority .

On the rotating priority in the single chip DMA system, the highest priority of any one channel comes after no more than three higher priority services have occurred. This rotating priority prevent a specfic channel from occupying the system all the time.(See the following next page diagram.)



The priority judging circuit selects a channel with the highest priority requesting the DMA service for every active edge of HLDA

Once the channel starts the service, that operation will not be suspended even when the service is demanded by another channel with higher priority. A channel with higher priority can get the control right only after a channel with lower priority relinquished HRQ.

Whenever the control is transferred from a channel to another channel, MPU gets the system bus control right. This assures the leading edge of HLDA which is used for selecting a channel with the highest priority.

5.8 COMPRESSED TRANSFER TIMING:

In order to accomplish greater throughout allowed by system characteristics, the TMP8237A is capable of compressing the transfer time to 2 clock cycles. As can be seen from Timing Diagram 3, State S3 is used to extend readout pulse access time. When State S3 is removed, readout pulse width becomes equal to write pulse width. Then, the transfer will consist of State S2 for changing address and State S4 for executing read/write. State S1 is produced when A_8 to A_{15} are updated (refer to Address Generation). Compressed transfer timing is shown in Timing Diagram 5.

During Memory-to Memory transfer, compressed transfer is not available.

5.9 ADDRESS GENERATION:

To reduce number of pins, the TMP8237A has the multiplexed address/data bus. State S1 is used to output high order address byte to the external latch. The trailing edge of ADSTB is used to load the address byte from the data line on the external latch circuit.

AEN is used to enable latch outputs from 3 states. Low order address byte is directly output by the TMP8237A.

A_0 to A_7 are connected to address bus. Timing Diagram 3 show the relationship among CLK, AEN, ADSTB, DB_0 to DB_7 and A_0 to A_7.

Addresses produced during the block and demand transfers are sequential. For many transfer the same address data will be held in the external address latch. This address data changes only when carry or borrow from A_7 to A_8 is produced in the normal sequence. To raise system through put, on the TMP8237A, S1 state is executed only for updating A_8 to A_{15} requiring the external latch.

6. DESCRIPTION OF REGISTERS

Register Name	Size	Number
Base address register	16-bit	4
Base word count register	16-bit	4
Count address register	16-bit	4
Current word count register	16-bit	4
Temporary address register	16-bit	1
Temporary word count register	16-bit	1
Status register	8-bit	1
Command register	8-bit	1
Temporary register	8-bit	1
Mode register	6-bit	4
Mask register	4-bit	1
Request register	4-bit	1

050489

Figure 6.1 Internal Registers

6.1 CURRENT ADDRESS REGISTER:

Each channel has a 16-bit current address register. This register holds addreses that are used during the DMA trnasfer. After each transfer, this register is automatically incremented or decremented, and intermediate address values are stored in the current address register during the transfer. Write or read of this register is made by MPU. An original value is initialized again by the auto initialization.

The auto initialization is taken place only after $\overline{EOP}$.

6.2 CURRENT WORD COUNT REGISTER:

Each channel has a 16-bit current word count register. For this register, the number of words to be transferred that is one less than that to be transferred must be programmed. The word counter is decremented after each transfer. Intermediate values of word count are stored in this register during the transfer. When the register value goes from 0000H to FFFFH, TC (Terminal Count) is produced.

When this register is in the program condition, load or read is made by MPU. Following the end of DMA service, this register is initialized to original values again by the auto initialization.

The auto initialization is taken place only when $\overline{EOP}$ is produced.

Note that the content of the word count register becomes FFFFH following internally produced $\overline{EOP}$.

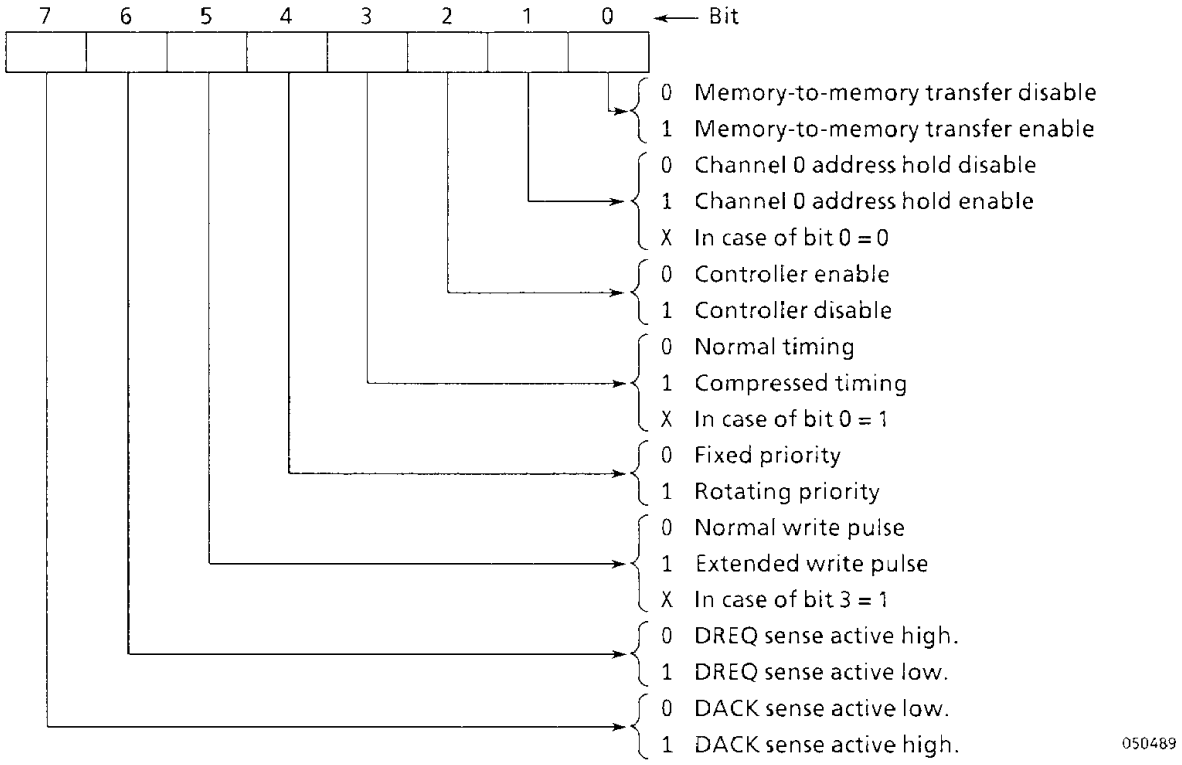
6.3 BASE ADDRESS REGISTER, BASE WORD COUNT REGISTER:

Each channel has a pair of registers; the base address register and base word count register. These 16-bit registers store original values of related current registers. These registers are used to store original values of current registers at time of the auto initialization. Write to the base register is made at the same time of write into equivalent current registers during the programming by MPU.

Therefore, write into the current registers which store intermediate values are made over these intermediate values. The base register cannot be read out by MPU.

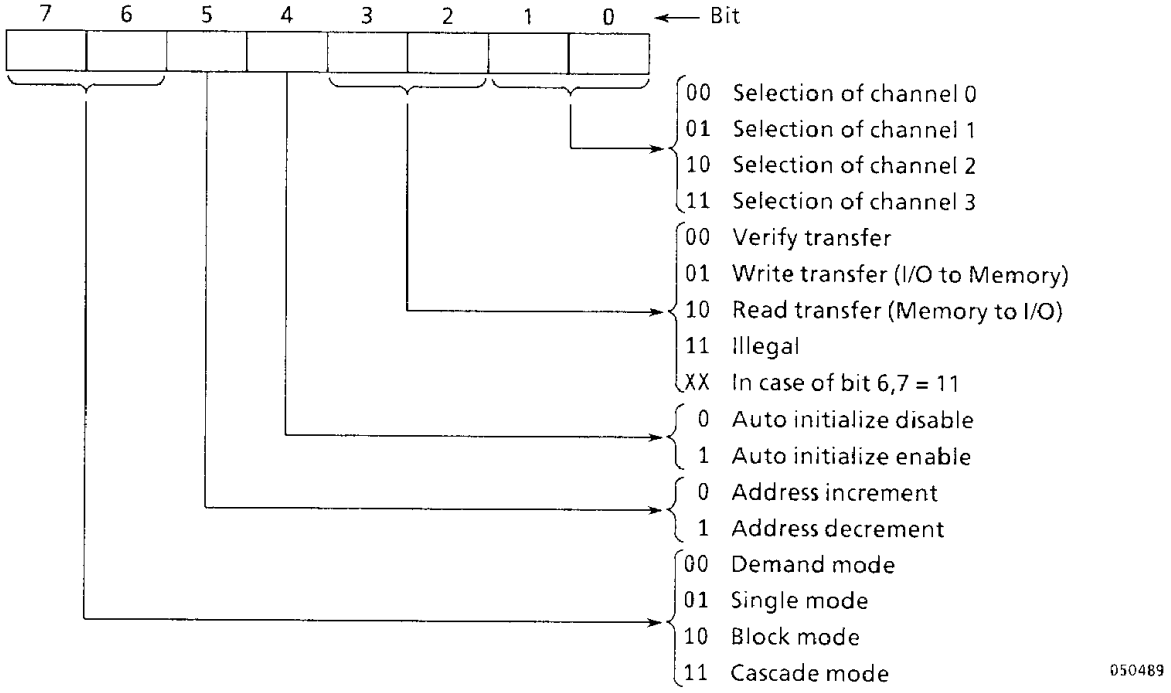
6.4 COMMAND REGISTER:

This 8-bit register controls the operation of TMP8237A. This command register is programmed (clear or reset) by MPU when it is in the program condition. The figure presented below show the functions of command bits. For address codes, refer to Figure 6.2.



6.5 MODE REGISTER:

All channels have a 6-bit mode register, respectively. This mode register is written by MPU when it is in the program condition, and Bit 0 and 1 select the channel to be programmed is to be written.

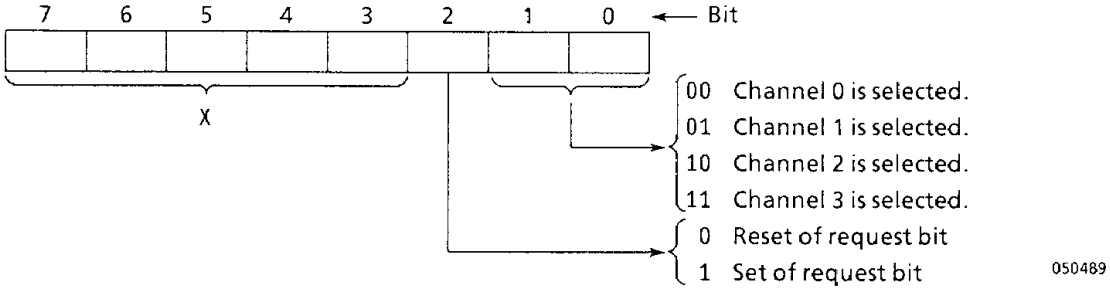


6.6 REQUEST REGISTER:

The TMP8237A is capable of responding to DMA service request by software similar to DREQ. Each channel has a single bit request register which cannot be masked. Further, priority is given by the priority encode circuit.

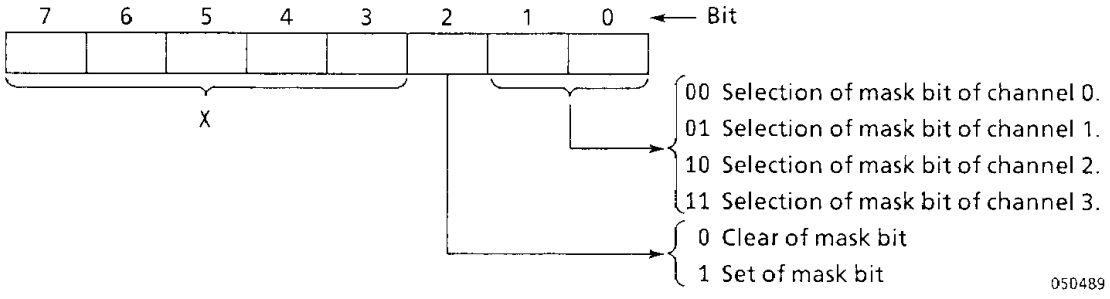
Bit of each register is set or cleared by software and further, cleared by generation of TC or external $\overline{EOP}$. All registers are cleared by reset. In order to set or reset bit, a proper form of data word is loaded by software.

Address codes are shown in Figure 6.2. DMA service request by software is accepted only when the channels are in the block mode. In the Memory-to-Memory transfer, DMA service request to only channel 0 by this software command becomes valid.

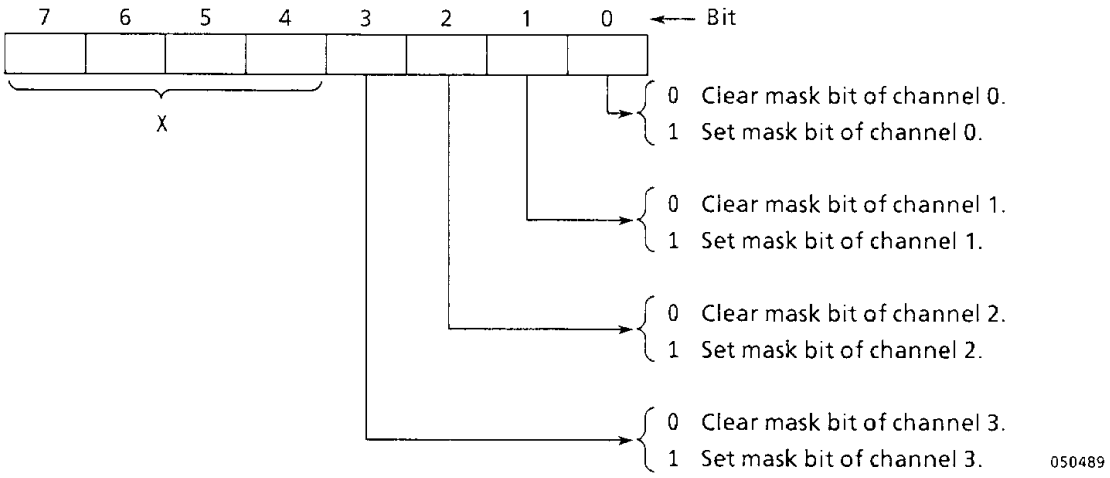


6.7 MASK REGISTER:

For each channel, mask bit are allocated to the mask register to disable DREQ input. If the auto initialization has not been programmed for the channels, the channel corresponding to a mask bit is set when $\overline{EOP}$ is produced. Each bit of the 4-bit mask register is also set or cleared by the software command. All bits are also set by reset. This will disable all DMA requests until the clear mask register command is enabled. Command addressing is shown in Figure 6.2.



All four bits of the mask register can be written also by a single command.



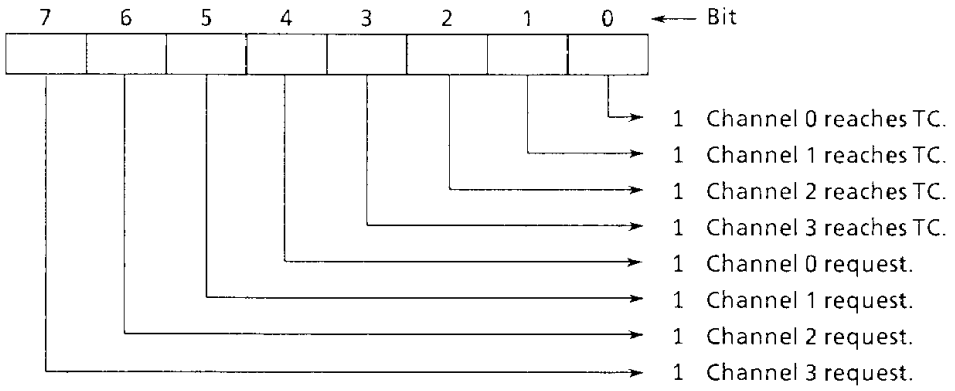
6.8 STATUS REGISTER

This register is read out by MPU through the TMP8237A. Status information of the TMP8237A at time of readout is included.

Information as to which channel reaches the terminal count (TC) and which channel is pending the DMA request are included in this information. Bits 0 to 3 are set every time when a channel reaches TC including the auto initialization.

These bits are cleared by reset or when each status is read out.

Bits 4 to 7 are always set when corresponding channels are requesting the DMA service



050489

6.9 TEMPORARY REGISTER:

This register is used for holding data during the Memory-to-Memory transfer. A last word transferred following the end of transfer is read out by MPU that is in the program condition. Unless cleared by reset, this register contains the last word transferred during the preceding Memory-to-Memory transfer.

6.10 SOFTWARE COMMANDS:

These commands are special software commands which are executed in the program condition and do not depend upon the specified bit pattern on the data bus. These commands are available in following third commands:

6.10.1 Clear First/Last flip-flop

This command is executed prior to write or read of address information or word count information of the TMP8237A. Furthermore, this command is used when low order or high order 8 bits of register are accessed.

6.10.2 Master Clear

This software command has the same effect as the hardware reset. The command, status, request, temporary, and internal First/Last flip-flop registers are all cleared by this command, and the mask register is set.

The TMP8237A enters into the idle cycle.

6.10.3 Clear Mask Register

This command clears all mask bits of four channels, enabling acceptance of the DMA service requests.

Address codes of the software commands are shown in Figure 6.2.

Signal						Operation
A_3	A_2	A_1	A_0	$\overline{IOR}$	$\overline{IOW}$	
1	0	0	0	0	1	Read of status register
1	0	0	0	1	0	Write to command register
1	0	0	1	0	1	–
1	0	0	1	1	0	Write to request register
1	0	1	0	0	1	–
1	0	1	0	1	0	Bit set, reset of mask register
1	0	1	1	0	1	–
1	0	1	1	1	0	Write to mode register
1	1	0	0	0	1	–
1	1	0	0	1	0	Clear First/Last flip-flop
1	1	0	1	0	1	Read of temporary register
1	1	0	1	1	0	Master clear
1	1	1	0	0	1	–
1	1	1	0	1	0	Clear mask register
1	1	1	1	0	1	–
1	1	1	1	1	0	All bit write of mask register

Note : The oblique lined codes denote illegal codes. 050489

Figure 6.2 Register and Function Addressing

Channel	Register	Operation	Signal							Internal F/L F/F	Data Bus DB_0~DB_7
			$\overline{CS}$	$\overline{IOR}$	$\overline{IOW}$	A_3	A_2	A_1	A_0		
0	Base & Current Address	Write	0	1	0	0	0	0	0	0	A_0 ~ A_7
			0	1	0	0	0	0	0	1	A_8 ~ A_{15}
	Current Address	Read	0	0	1	0	0	0	0	0	A_0 ~ A_7
			0	0	1	0	0	0	0	1	A_8 ~ A_{15}
	Base & Current Address	Write	0	1	0	0	0	0	1	0	W_0 ~ W_7
			0	1	0	0	0	0	1	1	W_8 ~ W_{15}
	Current Address	Read	0	0	1	0	0	0	1	0	W_0 ~ W_7
			0	0	1	0	0	0	1	1	W_8 ~ W_{15}
1	Base & Current Address	Write	0	1	0	0	0	1	0	0	A_0 ~ A_7
			0	1	0	0	0	1	0	1	A_8 ~ A_{15}
	Current Address	Read	0	0	1	0	0	1	0	0	A_0 ~ A_7
			0	0	1	0	0	1	0	1	A_8 ~ A_{15}
	Base & Current Address	Write	0	1	0	0	0	1	1	0	W_0 ~ W_7
			0	1	0	0	0	1	1	1	W_8 ~ W_{15}
	Current Address	Read	0	0	1	0	0	1	1	0	W_0 ~ W_7
			0	0	1	0	0	1	1	1	W_8 ~ W_{15}
2	Base & Current Address	Write	0	1	0	0	1	0	0	0	A_0 ~ A_7
			0	1	0	0	1	0	0	1	A_8 ~ A_{15}
	Current Address	Read	0	0	1	0	1	0	0	0	A_0 ~ A_7
			0	0	1	0	1	0	0	1	A_8 ~ A_{15}
	Base & Current Address	Write	0	1	0	0	1	0	1	0	W_0 ~ W_7
			0	1	0	0	1	0	1	1	W_8 ~ W_{15}
	Current Address	Read	0	0	1	0	1	0	1	0	W_0 ~ W_7
			0	0	1	0	1	0	1	1	W_8 ~ W_{15}
3	Base & Current Address	Write	0	1	0	0	1	1	0	0	A_0 ~ A_7
			0	1	0	0	1	1	0	1	A_8 ~ A_{15}
	Current Address	Read	0	0	1	0	1	1	0	0	A_0 ~ A_7
			0	0	1	0	1	1	0	1	A_8 ~ A_{15}
	Base & Current Address	Write	0	1	0	0	1	1	1	0	W_0 ~ W_7
			0	1	0	0	1	1	1	1	W_8 ~ W_{15}
	Current Address	Read	0	0	1	0	1	1	1	0	W_0 ~ W_7
			0	0	1	0	1	1	1	1	W_8 ~ W_{15}

050489

Figure 6.3 Word Count, Address Registers

7. PROGRAMMING

If HLDA of MPU is inactive it is possible to program the TMP8237A by MPU even when HRQ is active.

However, it is necessary for MPU to take care that programming of the TMP8237A and answer of HLDA are taken place simultaneously.

It requires care when the DMA service is requested to an unmasked channel during the programming of the TMP8237A.

It is considered that an embarrassing trouble may be caused in this case.

For instance, if MPU is going to rewrite the address register of channel 2 and in addition, the TMP8237A is enabled and channel 2 is not masked when channel 2 received a DMA request. The DMA service will be started after one byte of the address register is written. Such a problem as exampled above can be taken place.

To avoid such problems as this, it is better to disable the controller or mask unmasked channels before reprogramming any register.

It is better to enable the controller or clear the masking when the programming is completed.

Example of Program Set (CH2)

```
DI                          :  Interrupt disable
OUT   MCLR                  :  Master clear
MVI   A, XXXXXXXXB
OUT   CMND                  :  Command register set-up
MVI   A, XXXXXX10B
OUT   MODE                  :  Mode register set-up
MVI   A, 37H
OUT   ADR2                  :  CH2 Address Reg. (low order)
MVI   A, 82H
OUT   ADR2                  :  CH2 Address Reg. (high order)
MVI   A, 17H
OUT   WCNT2                 :  CH2 Word count register (low order)
MVI   A, 95H
OUT   WCNT2                 :  CH2 Word count register (high order)
MVI   A, 00000010B
OUT   MSKB2                 :  CH2 Mask clear (single bit)
EI                          :  Interrupt enable
```

8. ELECTRIC CHARACTERISTICS

8.1 ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	Supply Voltage	With Respect to GND.	−0.5~+7.0	V
V_{IN}	Input Voltage		−0.5~+7.0	V
V_{OUT}	Output Voltage		−0.5~+7.0	V
P_D	Power Dissipation	—	1.5	W
T_{sol}	Solder Temperature	—	260 (10 sec)	°C
T_{stg}	Strage Temperature	—	−65~+150	°C
T_{opr}	Operating Temperature	—	0~+70	°C

050489

8.2 DC CHARACTERISTICS

Ta = 0°C to 70°C, V_{CC} = 5V ± 5%, V_{SS} (GND) = 0V

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{IL}	Input Low Voltage		−0.5	—	0.8	V
V_{IH}	Input High Voltage		2.2	—	V_{CC}+0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 3.2mA	—	—	0.45	V
V_{OH1}	Output High Voltage	I_{OH1} = −200μA	2.4	—	—	V
V_{OH2}	Output High Voltage	I_{OH2} = −100μA (HRQ ONLY)	3.3	—	—	V
I_{IL}	Input Leakage Current	$0V \leqq V_{IN} \leqq V_{CC}$	—	—	±10	μA
I_{OFL}	Output Leakage Current	$0.45V \leqq V_{OUT} \leqq V_{CC}$	—	—	±10	μA
I_{CC}	Supply Current		—	—	150	mA

050489

8.3 AC CHARACTERISTICS

8.3.1 Active Cycle (1/3) (Notes : 2 and 9)

Ta = 0°C to 70°C, V_{CC} = 5V ± 5%, V_{SS} = 0V

SYMBOL	PARAMETER	MIN.	MAX.	Unit
T_{AEL}	AEN HIGH from CLK LOW (S1) Delay Time	—	200	ns
T_{AET}	AEN LOW from CLK HIGH (SI) Delay Time	—	130	ns
T_{AFAB}	ADR Active to FLoat Delay from CLK HIGH	—	90	ns
T_{AFC}	READ or $\overline{\text{WRITE}}$ Float Delay from CLK HIGH	—	120	ns

050489

Active Cycle (2/3)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
T_{AFDB}	DB Active to Float Delay from CLK HIGH	—	170	ns
T_{AHR}	ADR from $\overline{READ}$ HIGH Hold Time	TCY – 100	—	ns
T_{AHS}	DB from ADSTB LOW Hold Time	30	—	ns
T_{AHW}	ADR from $\overline{WRITE}$ HIGH Hold Time	TCY – 50	—	ns
T_{AK}	DACK Valid from CLK LOW Delay Time	—	170	ns
	$\overline{EOP}$ HIGH from CLK HIGH Delay Time	—	170	ns
	$\overline{EOP}$ LOW to CLK HIGH Delay Time	—	170	ns
T_{ASM}	ADR Stable from CLK HIGH	—	170	ns
T_{ASS}	DB to ADSTB LOW Setup Time	100	—	ns
T_{CH}	Clock HIGH Level Width	80	—	ns
T_{CL}	Clock LOW Level Width	68	—	ns
T_{CY}	Clock Cycle Time	200	—	ns
T_{DCL}	CLK HIGH to $\overline{READ}$ or $\overline{WRITE}$ LOW Delay Time (Note 3)	—	190	ns
T_{DCTR}	$\overline{READ}$ HIGH from CLK HIGH (S4) Delay Time (Note 3)	—	190	ns
T_{DCTW}	$\overline{WRITE}$ HIGH from CLK HIGH (S4) Delay (Note 3)	—	130	ns
T_{DQ1}	HRQ Valid from CLK HIGH Delay TIme (Note 4)	—	120	ns
T_{DQ2}		—	120	ns
T_{EPS}	$\overline{EOP}$ Low from CLK LOW Setup Time	40	—	ns
T_{EPW}	$\overline{EOP}$ pulse width	220	—	ns
T_{FAAB}	DB Float to Active Delay from CLK HIGH	—	170	ns
T_{FAC}	$\overline{READ}$ or $\overline{WRITE}$ Active from CLK HIGH	—	150	ns
T_{FADB}	DB Float to Active Delay from CLK HIGH	—	200	ns
T_{HS}	HLDA Valid to CLK HIGH Setup Time	75	—	ns
T_{IDH}	Input Data from $\overline{MEMR}$ HIGH Hold Time	0	—	ns
T_{IDS}	Input Data to $\overline{MEMR}$ HIGH Setup Time	170	—	ns
T_{ODH}	Output Data to $\overline{MEMR}$ HIGH Hold Time	10	—	ns
T_{ODV}	Output Data Valid to $\overline{MEMW}$ HIGH	125	—	ns
T_{QS}	DREQ to CLK LOW (SI, S4) Setup Time	0	—	ns
T_{RH}	CLK to READY LOW Hold Time	20	—	ns

050489

Active Cycle (3/3)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
T_{RS}	READY to CLK LOW Setup Time	60	—	ns
T_{STL}	ADSTB HIGH from CLK HIGH Delay TIme	—	130	ns
T_{STT}	ADSTB LOW from CLK HIGH Delay TIme	—	90	ns

050489

8.3.2 Program Condition (Idle Cycle) (Notes : 2, 8 and 9)

Ta = 0°C to 70°C, V_{CC} = 5V ± 5%, V_{SS} = 0V

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
T_{AR}	ADR Valid or $\overline{CS}$ LOW to $\overline{READ}$ LOW	50	—	ns
T_{AW}	ADR Valid or $\overline{WRITE}$ HIGH Setup Time	130	—	ns
T_{CW}	$\overline{CS}$ LOW to $\overline{WRITE}$ HIGH Setup Time	130	—	ns
T_{DW}	Data Valid to $\overline{WRITE}$ HIGH Setup Time	130	—	ns
T_{RA}	ADR or CS Hold from $\overline{READ}$ HIGH	0	—	ns
T_{RDE}	Data Access from $\overline{READ}$ LOW	—	140	ns
T_{RDF}	Data Bus Float Delay from $\overline{READ}$ HIGH	0	70	ns
T_{RSTD}	Power Supply HIGH to RESET LOW Setup Time	500	—	ns
T_{RSTS}	RESET to First $\overline{IOWR}$	2	—	TCY
T_{RSTW}	RESET pulse width	300	—	ns
T_{RW}	$\overline{READ}$ pulse width	200	—	ns
T_{WA}	ADR from $\overline{WRITE}$ HIGH Hold Time	20	—	ns
T_{WC}	$\overline{CS}$ HIGH from $\overline{WRITE}$ HIGH Hold Time	20	—	ns
T_{WD}	Data from $\overline{WRITE}$ HIGH Hold Time	30	—	ns
T_{WWS}	$\overline{WRITE}$ pulse width	160	—	ns

050489

8.4 CAPACITY

Ta = 25°C, V_{CC} = GND = 0V

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_O	Output Capacitance	f_C = 1.0MHz, Input = 0V	—	—	8	pF
C_I	Input Capacitance		—	—	15	
$C_{I/O}$	I/O Capacitance		—	—	20	

050489

Note 1 : Typ. value is that when rated voltage is applied at Ta = 25°C.

Note 2 : Test conditions; a) Unless otherwise specified, timing defining signal voltages are;
Input High level = 2.4V, Low level = 0.45V
Output High level = 2.0V, Low level = 0.8V

b) Unless otherwise specified, 1 × TTL gate and 150pF load are provided to output.

Note 3 : Normal write pulse width is TCY − 100 ns. Extension write pulse width is 2TCY − 100 ns. Read pulse width is 2TCY-50 ns, and compressed read pulse width is TCY − 50 ns.

Note 4 : TDQ is measured at two different high levels.
TDQ1 = 2.0V, TDQ2 = 3.3V

Note 5 : It is necessary to keep DREQ active until DACK is received.

Note 6 : Both low active and high active level ae available for DREQ and DACK.

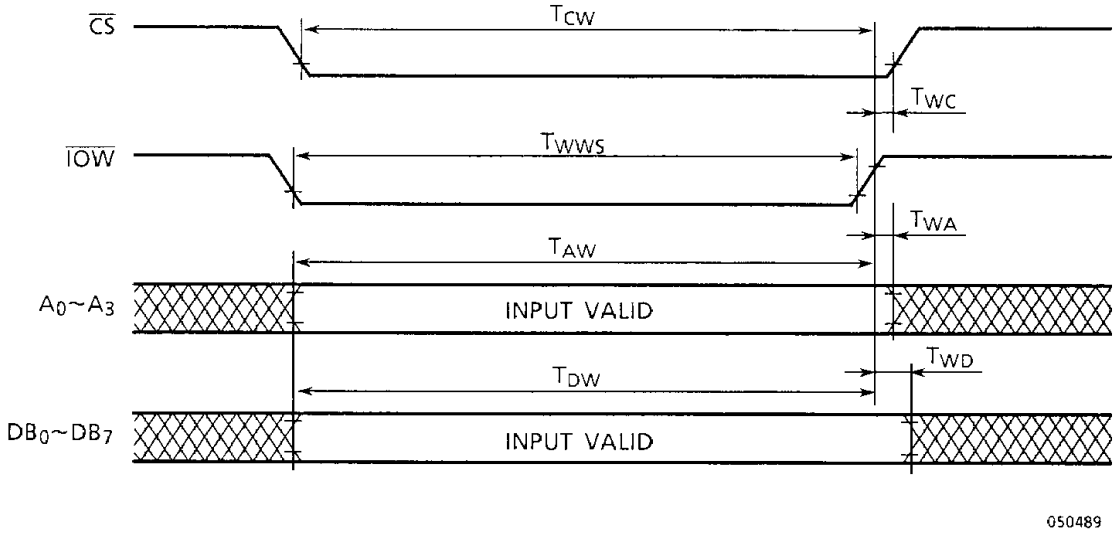
Note 7 : Output load of the data bus are provided with 1 × TTL gate and 15 pF as the minimum value, and 1 × TTL gate and 150 pF as the maximum value.

Note 8 : Sucessive read or/and write operations by the MPU to program must be timed to allow at least 600ns for the TMP8237AP and at least 400ns for the TMP8237AP-5 as recovery time between active read or write pulses.

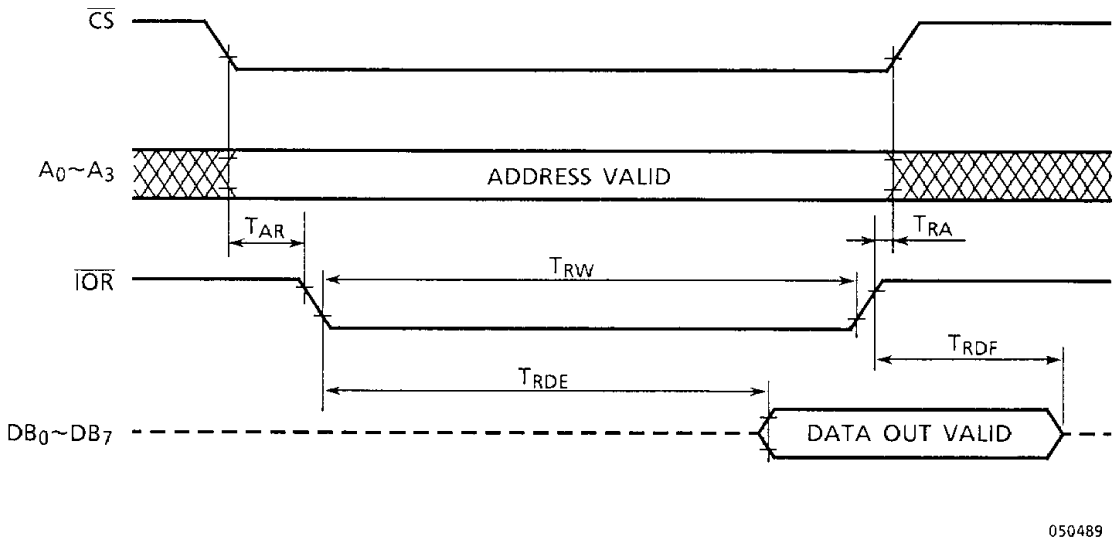
Note 9 : Signal $\overline{\text{READ}}$ and $\overline{\text{WRITE}}$ are $\overline{\text{IOR}}$ and $\overline{\text{MEMW}}$ for the DMA operations from peripheral devices to the memory. In the DMA operations from the memory to peripheral devices, they are $\overline{\text{MEMR}}$ and $\overline{\text{IOW}}$.

Note10 : When N state wait is added at time of write to memory in the latter half of memory-to-memory transfer, this parameter increases by N (TCY) at a time.

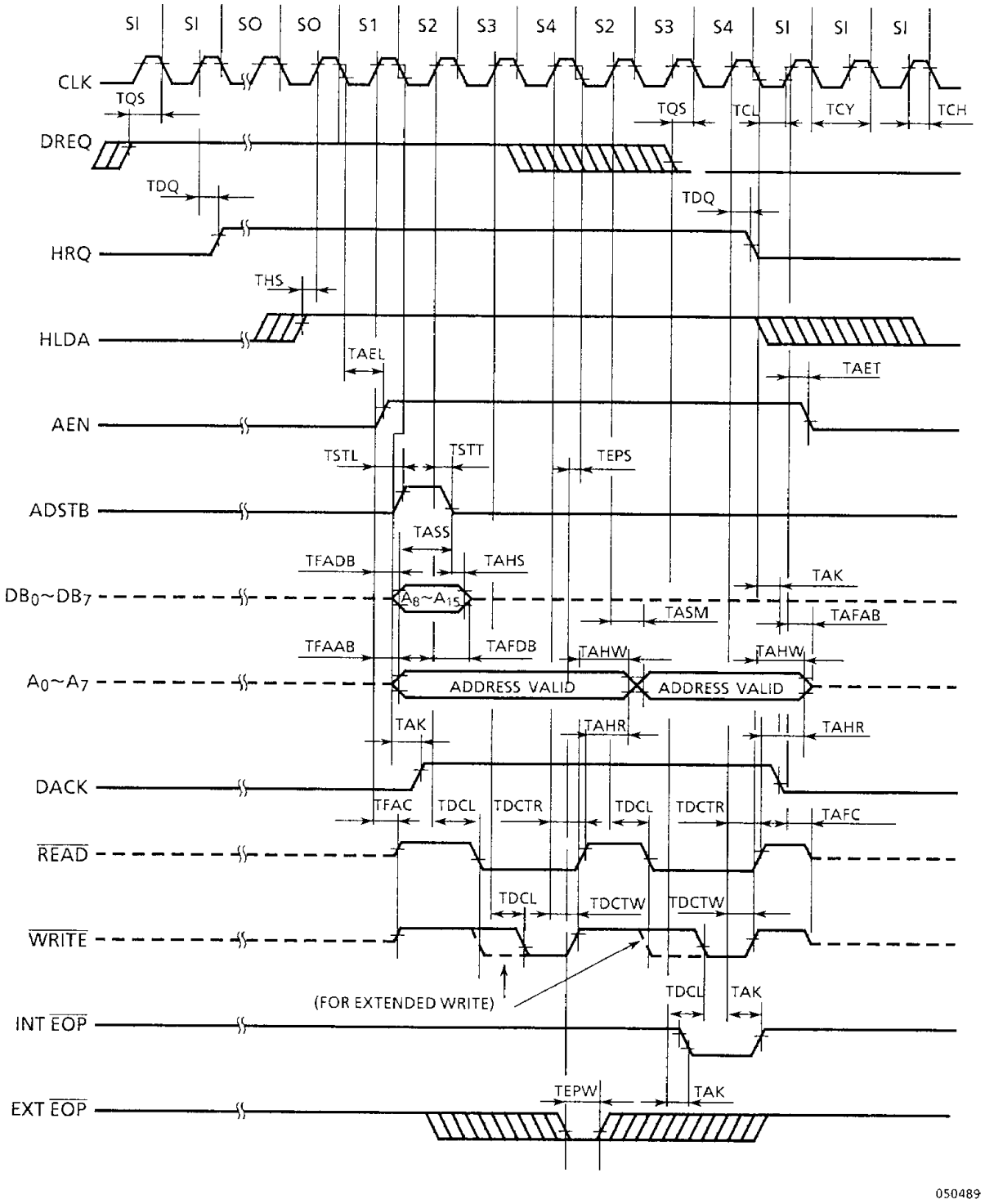
9. TIMING DIAGRAM



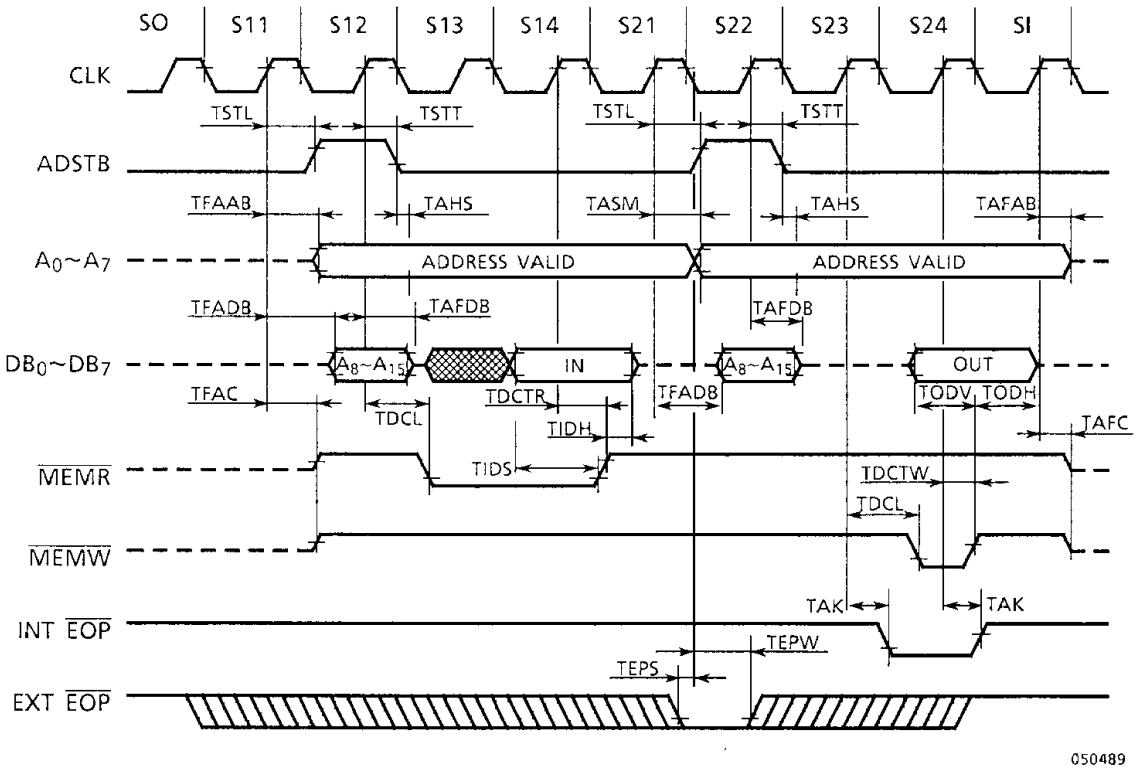
Timing Diagram 1 Program Condition Write Timing



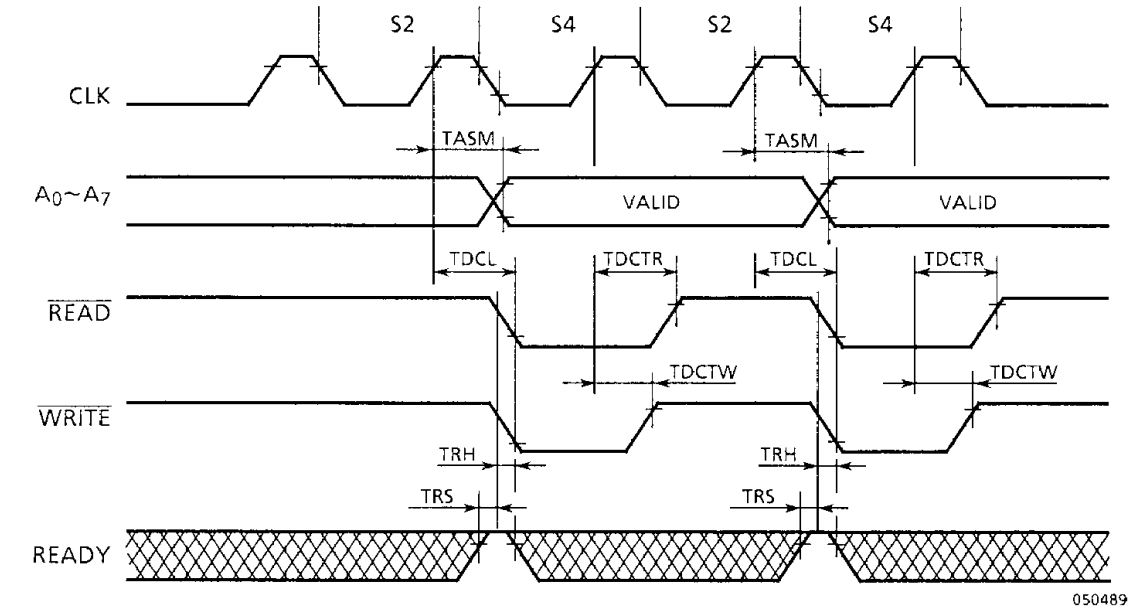
Timing Diagram 2 Program Condition Read Cycle



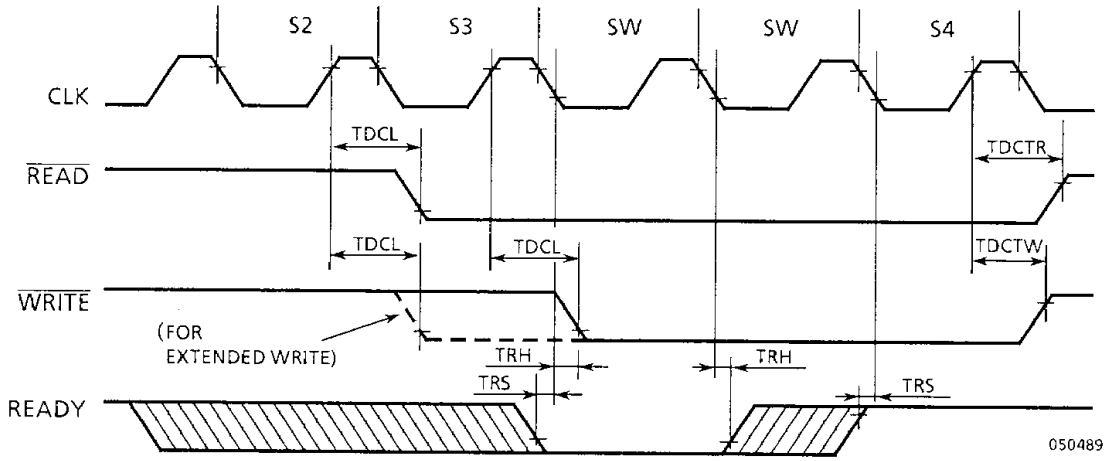
Timing Diagram 3 Active Cycle



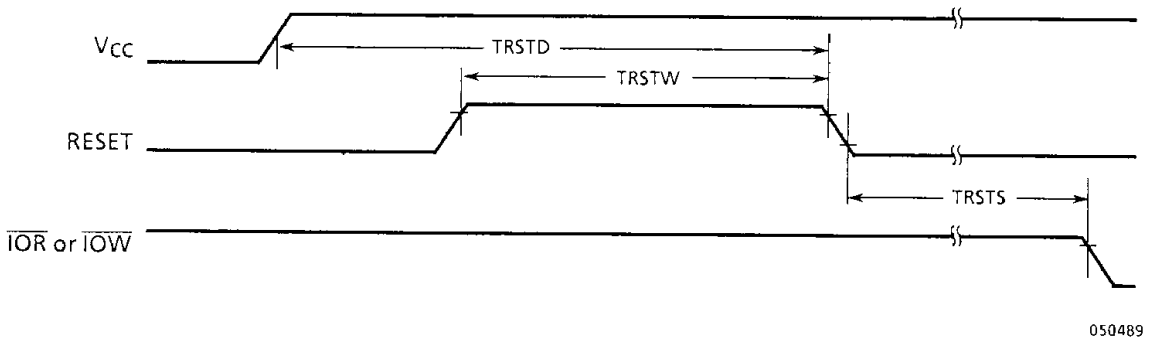
Timing Diagram 4 Memory-to-Memory Transfer



Timing Diagram 5 Compressed Transfer



Timing Diagram 6 Ready Timing

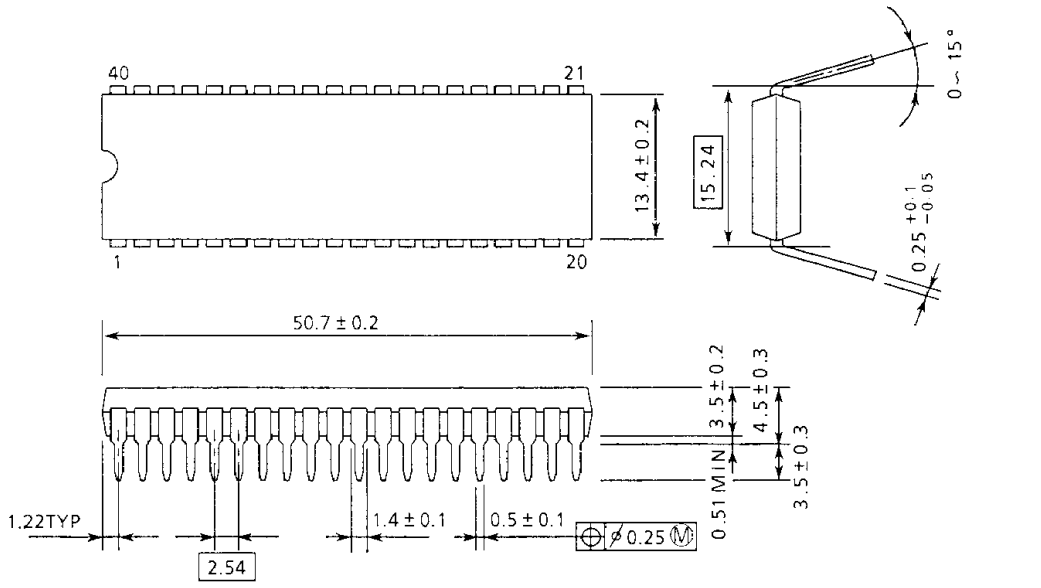


Timing Diagram 7 Reset Timing

10. EXTERNAL DIMENSION VIEW (PLASTIC PACKAGE)

DIP40-P-600

Unit : mm



270289

Note : Each pitch is 2.54mm, and all the leads are located within ±0.25mm from their theoretical positions with respect to No.1 and No.40 leads.

11. EXAMPLE OF APPLICATION CIRCUIT

The connecting method of the TMP8237A and MPU is shown in Figure 11.1.

The multimode DMA controller outputs a hold request whenever valid DMA request is produced from peripheral device. When MPU answers by the hold acknowledge signal, the TMP8237A receives the contorl right of the address bus, data bus, and control bus. In the first transfer, address (the least significant 8 bits of the address bits and the most significant 8 bits on the data bus) is output.

The content of the data bus is latched by the 8-bit latch (TC74HC373P) to make the address bus complete. After execution of the first transfer, that latched data is updated only when carry or borrow is produced on the least significant address byte.

When one TMP8237A is used, four DMA channels are provided.

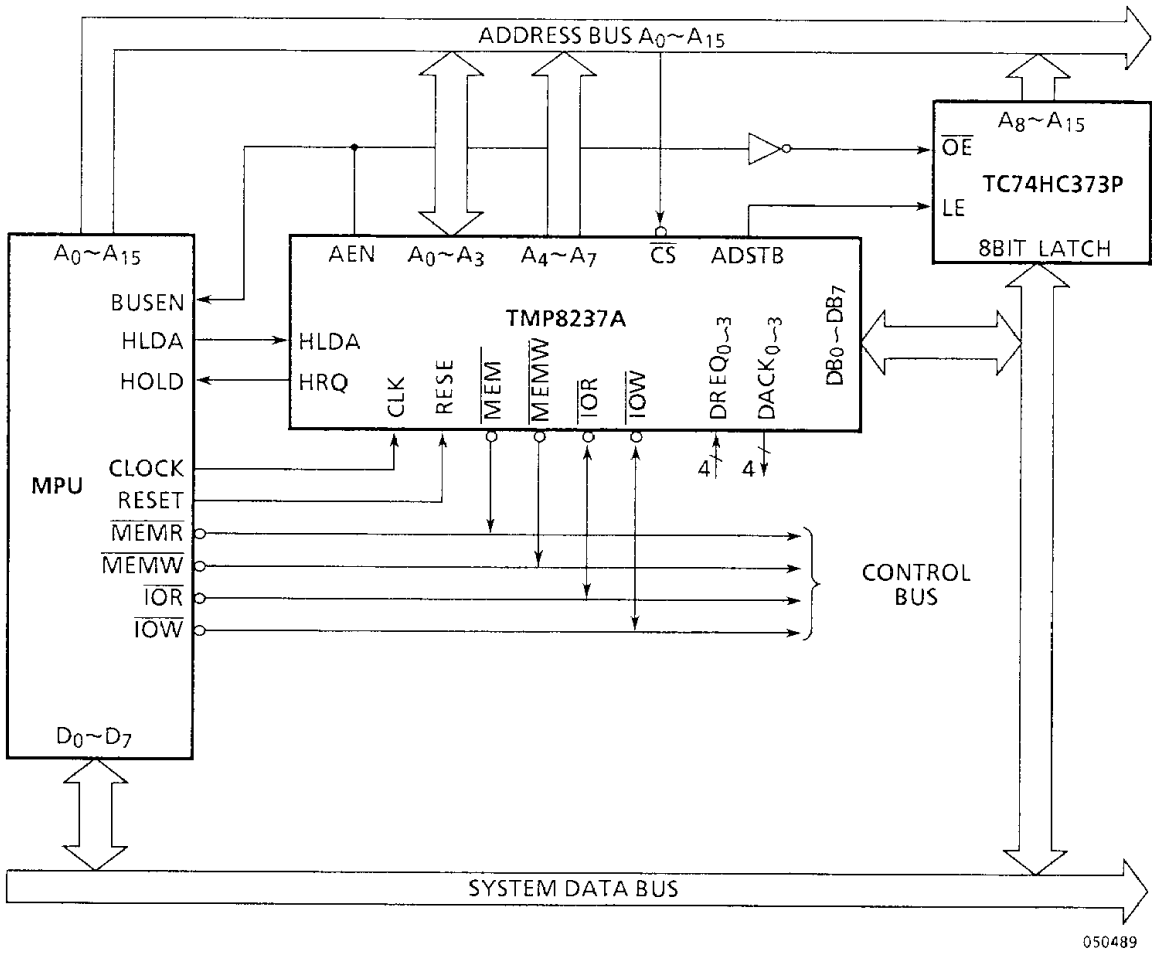


Figure 11.1 Basic System Connection Diagram

Figure 11.2 shows the expansion method for number of DMA channels. It is possible to realize net 7 DMA channels by connecting the second TMP8237A to one of the DMA channels of the first TMP8237A.

Two DMA chips commonly use the same 8-bit latch. Thus, any channel is used for expansion.

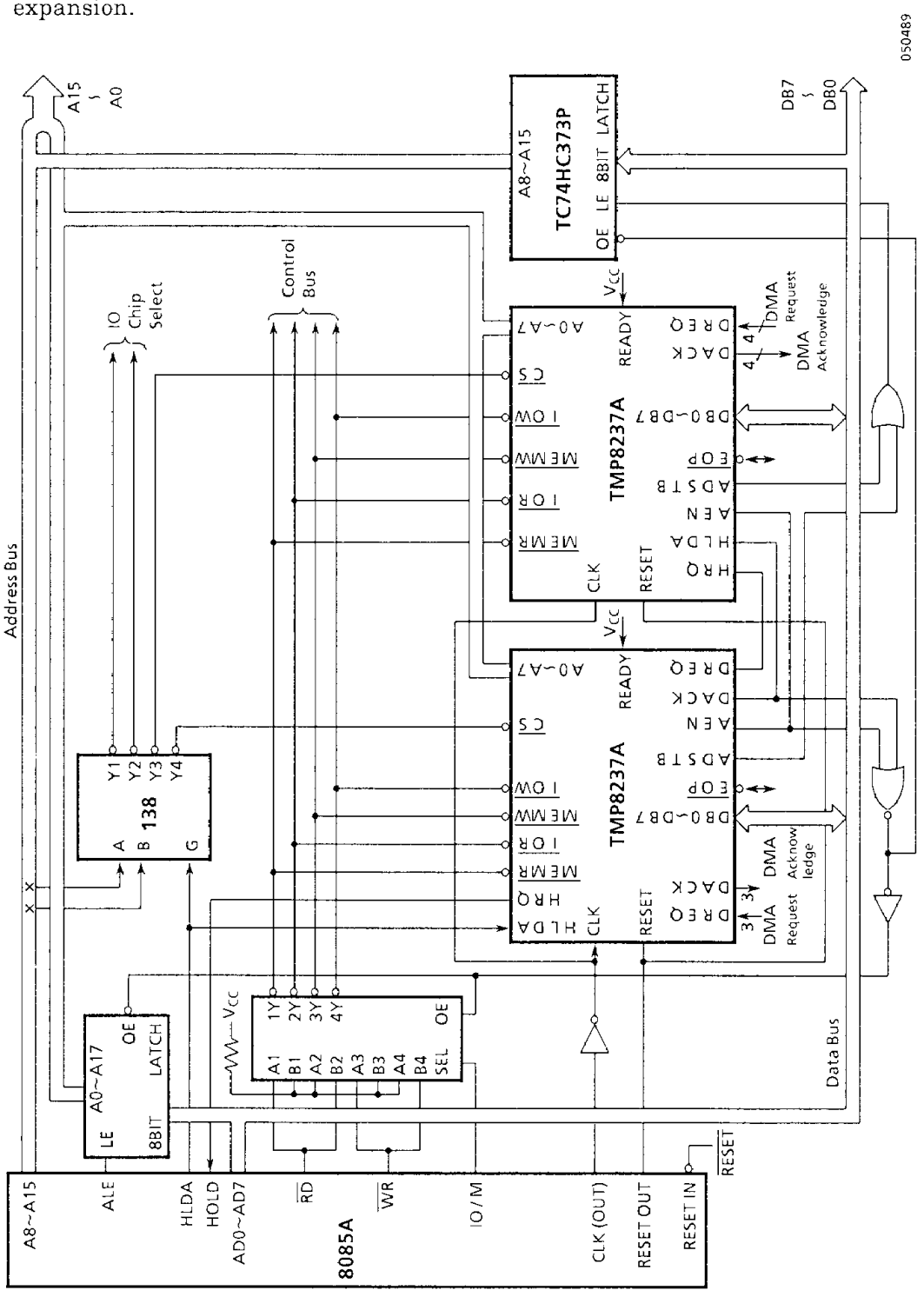


Figure 11.2 Expansion of TMP8237A