



MX23C8111

8M-BIT MASK ROM (8/16 BIT OUTPUT)

FEATURES

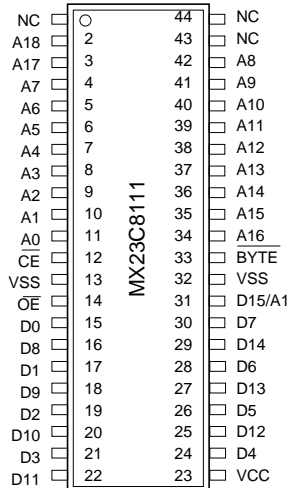
- Bit organization
 - 1M x 8 (byte mode)
 - 512K x 16 (word mode)
- Fast access time
 - Random access: 90ns (max.)
 - Page access: 50ns (max.)
- Current
 - Operating: 60mA
 - Standby: 100uA
- Supply voltage
 - 5V±10%
- Package
 - 44 pin SOP (500mil)
 - 42 pin PDIP (600mil)

ORDER INFORMATION

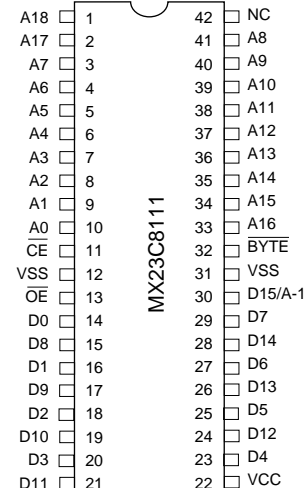
| Part No. | Access Time | Page Access Time | Access Package |
|----------------|-------------|------------------|----------------|
| MX23C8111MC-90 | 90ns | 50ns | 44 pin SOP |
| MX23C8111MC-10 | 100ns | 50ns | 44 pin SOP |
| MX23C8111MC-12 | 120ns | 60ns | 44 pin SOP |
| MX23C8111PC-10 | 100ns | 50ns | 42 pin PDIP |
| MX23C8111PC-12 | 120ns | 60ns | 42 pin PDIP |

PIN CONFIGURATION

44 SOP



42 PDIP

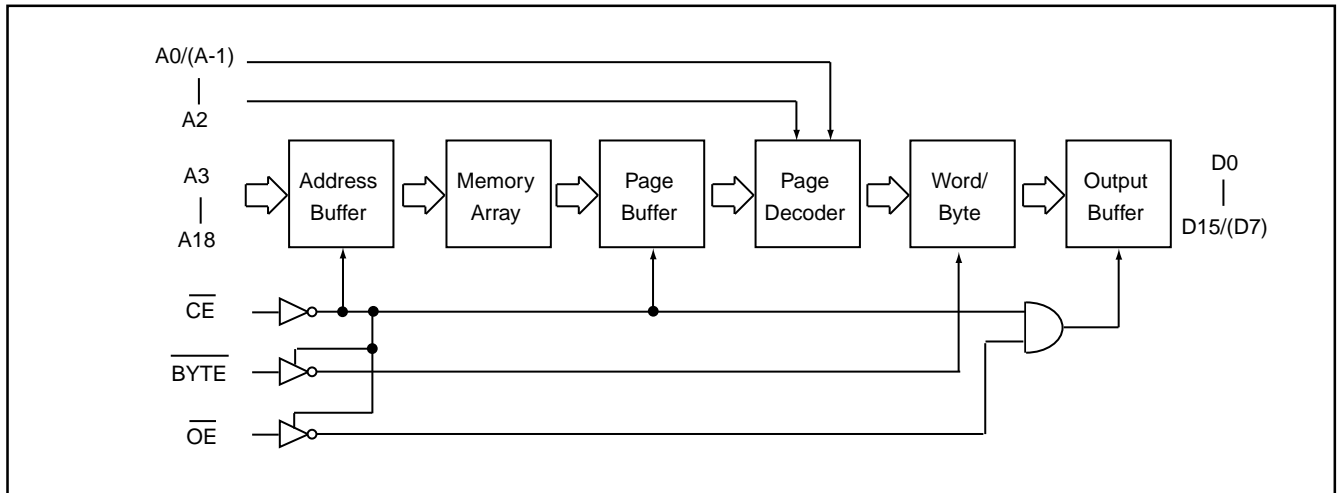


PIN DESCRIPTION

| Symbol | Pin Function |
|-----------------|---------------------|
| A0~A18 | Address Inputs |
| D0~D7 | Data Outputs |
| \overline{CE} | Chip Enable Input |
| \overline{OE} | Output Enable Input |
| VCC | Power Supply Pin |
| VSS | Ground Pin |
| NC | No Connection |

MODE SELECTION

| \overline{CE} | \overline{OE} | Byte | D15/A-1 | D0~D7 | D8~D15 | Mode | Power |
|-----------------|-----------------|------|---------|--------|--------|------|----------|
| H | X | X | X | High Z | High Z | - | Stand-by |
| L | H | X | X | High Z | High Z | - | Active |
| L | L | H | Output | D0~D7 | D8~D15 | Word | Active |
| L | L | L | Input | D0~D7 | High Z | Byte | Active |

BLOCK DIAGRAM

ABSOLUTE MAXIMUM RATINGS

| Item | Symbol | Ratings |
|------------------------------------|------------------|---------------------|
| Voltage on any Pin Relative to VSS | VCC | -0.3V to 7.0V |
| Input Voltage | VI | -0.3V to VCC + 0.5V |
| Output Voltage | VO | -0.3V to VCC + 0.5V |
| Ambient Operating Temperature | T _{opr} | 0°C to 70°C |
| Storage Temperature | T _{stg} | -65°C to 125°C |

DC CHARACTERISTICS (T_a = 0°C ~ 70°C, VCC = 5V±10%)

| Item | Symbol | MIN. | MAX. | Conditions |
|------------------------|--------|-------|----------|---------------------------------|
| Output High Voltage | VOH | 2.4V | - | IOH = -1.0mA |
| Output Low Voltage | VOL | - | 0.4V | IOL = 2.1mA |
| Input High Voltage | VIH | 2.2V | VCC+0.3V | |
| Input Low Voltage | VIL | -0.3V | 0.8V | |
| Input Leakage Current | ILI | - | 10uA | 0V, VCC |
| Output Leakage Current | ILO | - | 10uA | 0V, VCC |
| Operating Current | ICC1 | - | 60mA | f=10MHz, all output open |
| Standby Current (TTL) | ISTB1 | - | 1mA | CE=VIH |
| Standby Current (CMOS) | ISTB2 | - | 100uA | CE > VCC - 0.2V |
| Input Capacitance | CIN | - | 10pF | T _a = 25°C, f = 1MHZ |
| Output Capacitance | COUT | - | 10pF | T _a = 25°C, f = 1MHZ |

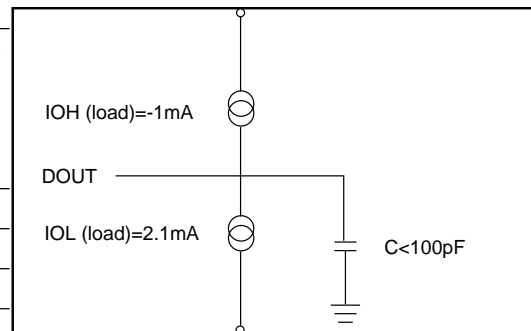
AC CHARACTERISTICS (Ta = 0°C ~ 70°C, VCC = 5V±10%)

| Item | Symbol | 23C8111-90 | | 23C8111-10 | | 23C8111-12 | |
|---------------------------|--------|------------|------|------------|-------|------------|-------|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. |
| Read Cycle Time | tRC | 90ns | - | 100ns | - | 120ns | - |
| Address Access Time | tAA | - | 90ns | - | 100ns | - | 120ns |
| Chip Enable Access Time | tACE | - | 90ns | - | 100ns | - | 120ns |
| Page Mode Access Time | tPA | - | 50ns | - | 50ns | - | 60ns |
| Output Enable Time | tOE | - | 50ns | - | 50ns | - | 60ns |
| Output Hold After Address | tOH | 0ns | - | 0ns | - | 0ns | - |
| Output High Z Delay | tHZ | - | 20ns | - | 20ns | - | 20ns |

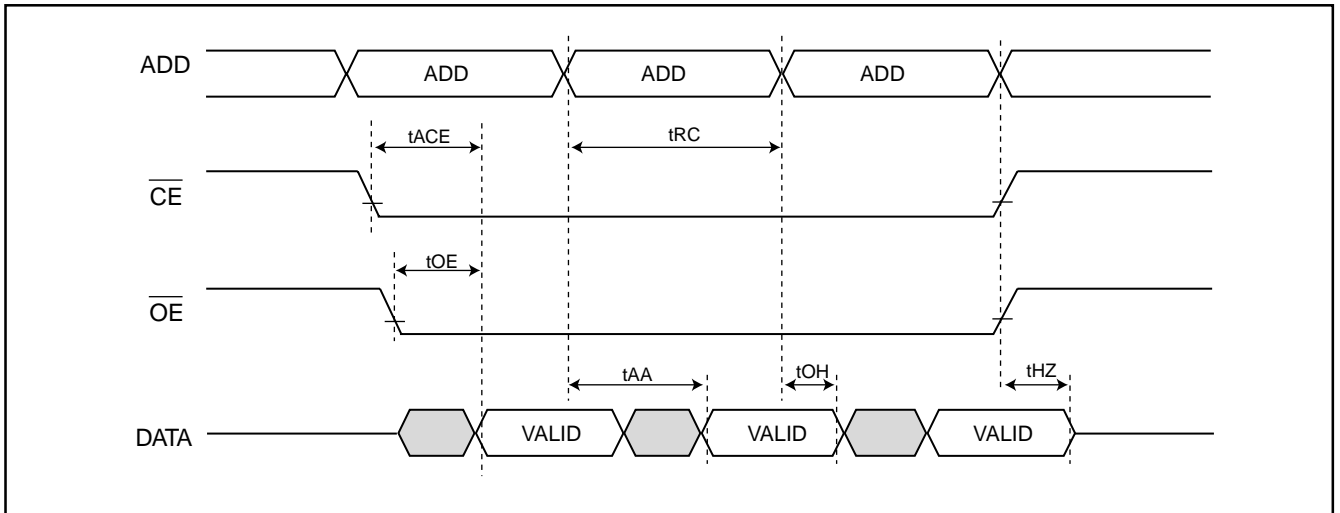
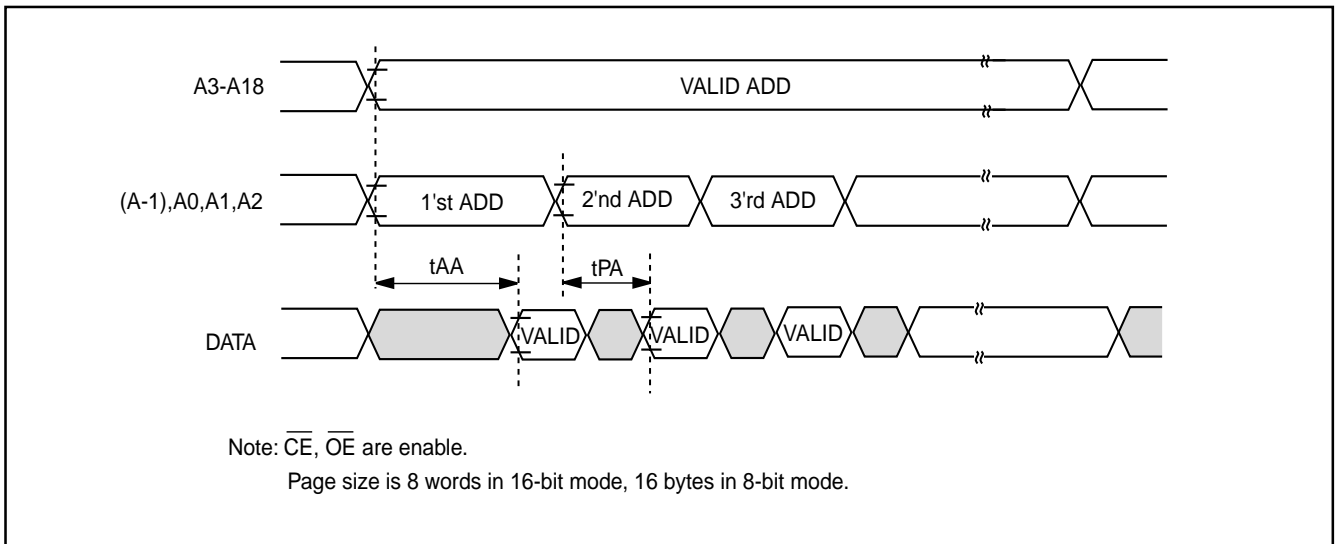
Note: Output high-impedance delay (tHZ) is measured from OE or CE going high, and this parameter guaranteed by design over the full voltage and temperature operating range - not tested.

AC Test Conditions

| | |
|---------------------------|---|
| Input Pulse Levels | 0.4V~2.7V for 90ns and 100ns speed grade 0.4V~2.4V for 120ns speed grade |
| Input Rise and Fall Times | 10ns |
| Input Timing Level | 1.5V |
| Output Timing Level | 0.8V and 2.0V |
| Output Load | See Figure |

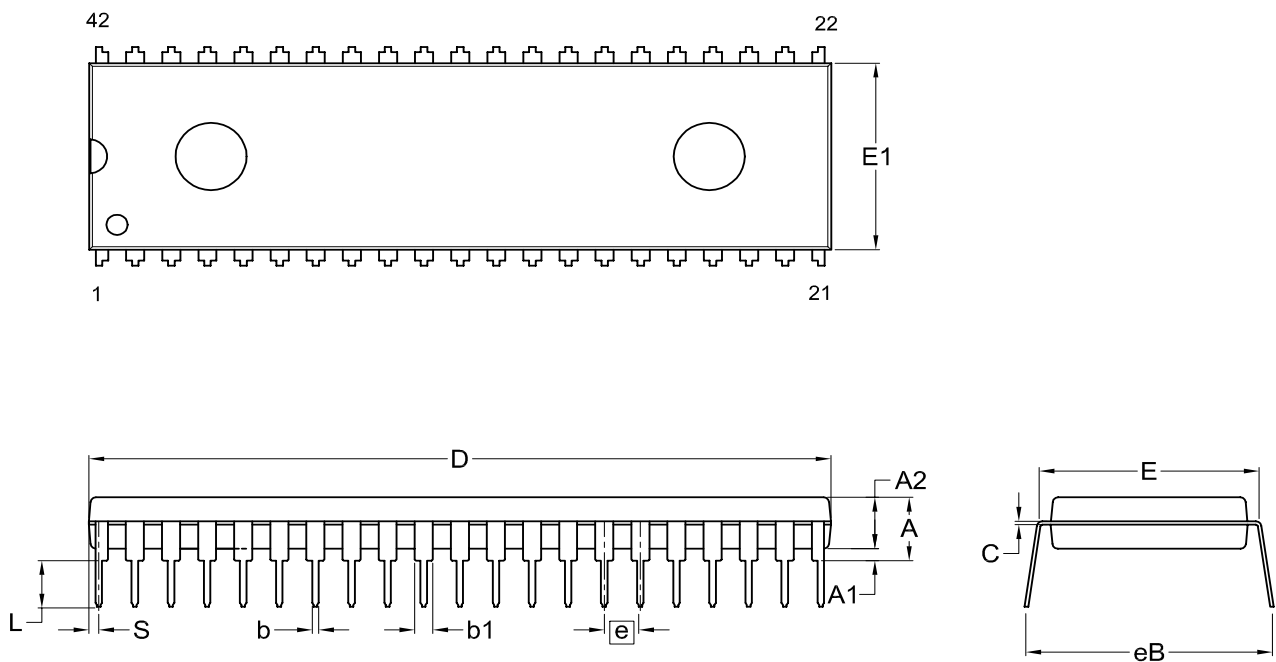


Note: No output loading is present in tester load board.
Active loading is used and under software programming control.
Output loading capacitance includes load board's and all stray capacitance.

TIMING DIAGRAM
Access Timing (Normal Access)

Page Read


PACKAGE INFORMATION

Title: Package Outline for PDIP 42L (600MIL)

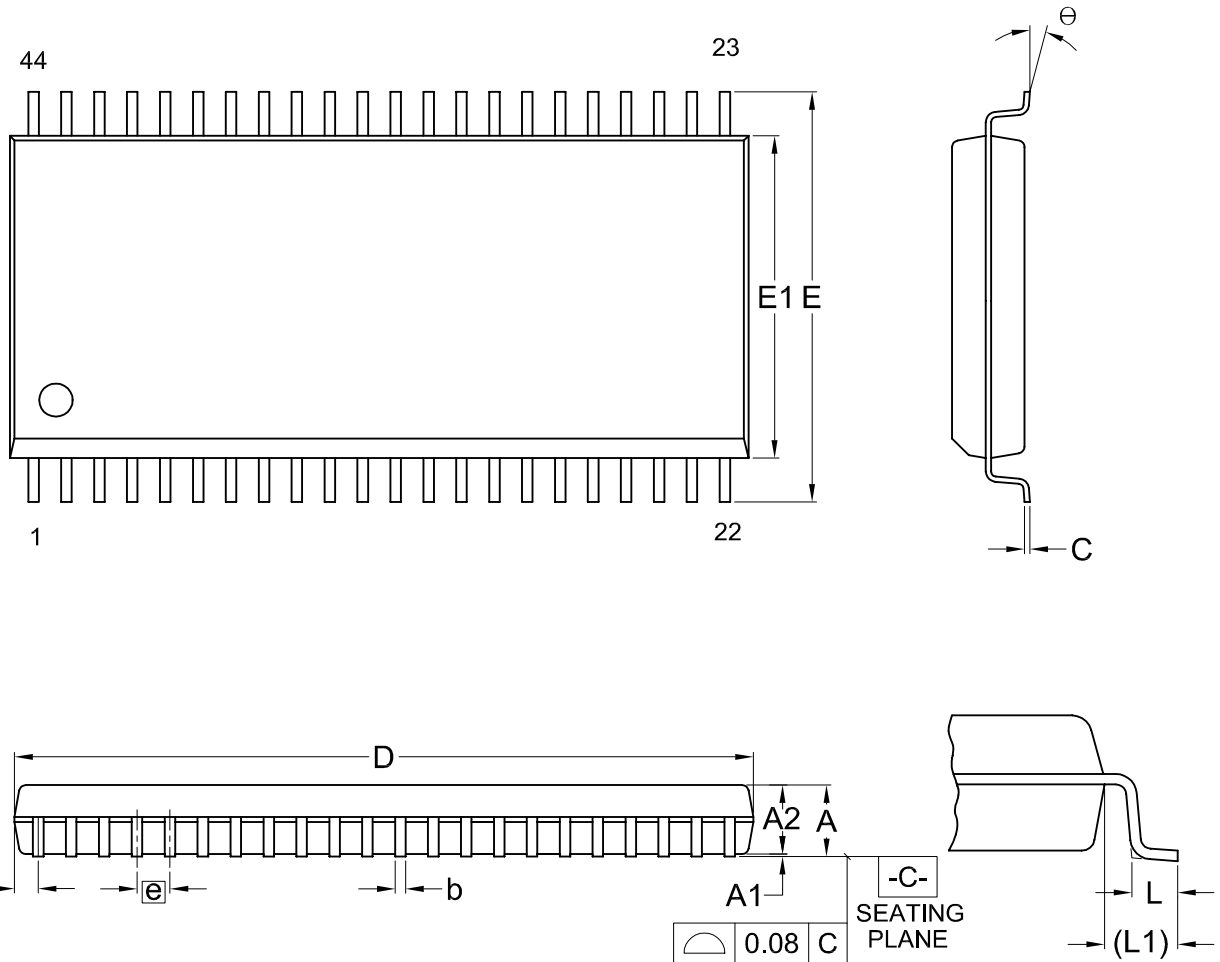


Dimensions (inch dimensions are derived from the original mm dimensions)

| SYMBOL | | A | A1 | A2 | b | b1 | C | D | E | E1 | e | eB | L | S |
|--------|------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| UNIT | | | | | | | | | | | | | | |
| mm | Min. | --- | 0.25 | 3.73 | 0.38 | 1.14 | 0.20 | 51.31 | 15.11 | 13.84 | | 15.75 | 2.92 | 0.38 |
| | Nom. | --- | --- | 3.94 | 0.46 | 1.27 | 0.25 | 51.94 | 15.24 | 13.97 | 2.54 | 16.51 | 3.30 | 0.64 |
| | Max. | 4.90 | 0.76 | 4.14 | 0.53 | 1.40 | 0.30 | 52.57 | 15.37 | 14.10 | | 17.27 | 3.68 | 0.89 |
| Inch | Min. | --- | 0.010 | 0.147 | 0.015 | 0.045 | 0.008 | 2.020 | 0.595 | 0.545 | | 0.620 | 0.115 | 0.015 |
| | Nom. | --- | --- | 0.155 | 0.018 | 0.050 | 0.010 | 2.045 | 0.600 | 0.550 | 0.100 | 0.650 | 0.130 | 0.025 |
| | Max. | 0.193 | 0.030 | 0.163 | 0.021 | 0.055 | 0.012 | 2.070 | 0.605 | 0.555 | | 0.680 | 0.145 | 0.035 |

| DWG.NO. | REVISION | REFERENCE | | | ISSUE DATE |
|-------------|----------|-----------|------|--|------------|
| | | JEDEC | EIAJ | | |
| 6110-0202.5 | 8 | | | | 11-24-'03 |

Title: Package Outline for SOP 44L (500MIL)



Dimensions (inch dimensions are derived from the original mm dimensions)

| SYMBOL | | A | A1 | A2 | b | C | D | E | E1 | e | L | L1 | S | θ |
|--------|------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|----------|
| UNIT | | | | | | | | | | | | | | |
| mm | Min. | --- | 0.10 | 2.59 | 0.36 | 0.15 | 28.37 | 15.83 | 12.47 | | 0.56 | 1.51 | 0.78 | 0 |
| | Nom. | --- | 0.15 | 2.69 | 0.41 | 0.20 | 28.50 | 16.03 | 12.60 | 1.27 | 0.76 | 1.71 | 0.91 | 5 |
| | Max. | 3.00 | 0.20 | 2.80 | 0.51 | 0.25 | 28.63 | 16.23 | 12.73 | | 0.96 | 1.91 | 1.04 | 10 |
| Inch | Min. | --- | 0.004 | 0.102 | 0.014 | 0.006 | 1.117 | 0.623 | 0.491 | | 0.022 | 0.059 | 0.031 | 0 |
| | Nom. | --- | 0.006 | 0.106 | 0.016 | 0.008 | 1.122 | 0.631 | 0.496 | 0.050 | 0.030 | 0.067 | 0.036 | 5 |
| | Max. | 0.118 | 0.008 | 0.110 | 0.020 | 0.010 | 1.127 | 0.639 | 0.501 | | 0.038 | 0.075 | 0.041 | 10 |

| DWG.NO. | REVISION | REFERENCE | | | ISSUE DATE |
|-----------|----------|-----------|------|--|------------|
| | | JEDEC | EIAJ | | |
| 6110-1405 | 6 | MO-175 | | | 11-26-03 |



REVISION HISTORY

| REVISION | DESCRIPTION | PAGE | DATE |
|-----------------|---------------------------------------|-------------|-------------|
| 2.1 | AC Characteristics: tOH--10ns --> 0ns | P3 | JAN/29/1999 |
| 2.2 | Modify Package Information | P5,6 | NOV/22/2001 |
| 2.3 | Modify Package Information | P5,6 | NOV/21/2002 |
| 2.4 | Modify 42-PDIP Package Information | P5 | JUN/19/2003 |
| 2.5 | Removed access time: 95ns | P1,3 | JUL/01/2003 |
| 2.6 | Added access time:90ns | P1,3 | JUL/29/2003 |



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