

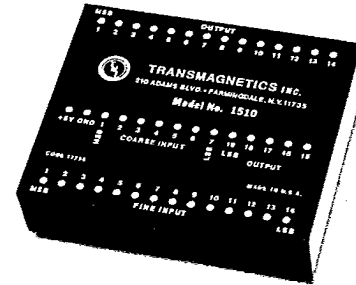
SERIES 1510

Revised July 1989

TWO-SPEED PROCESSOR

FEATURES:

- 36:1, 18:1, 9:1 ratio with same module
- Up to 19 bit resolution
- Usable with MUX Systems
- Nonambiguous output
- TTL/DTL compatible
- No calibration or adjustments required
- Meets MIL-STD-202D, Methods 101C, 105B, 106C, 107C, 202D, 204B, and 205D
- High reliability 883B or MIL-M-38510 units on request



DESCRIPTION:

This module is used to combine the binary outputs of synchro-to-digital converters whose inputs are connected to two speed synchro systems where the fine and coarse synchros are geared to each other by ratios of 36:1, 18:1, or 9:1. The combined outputs of the two input synchros can thus develop a resolution of 19 bits.

SPECIFICATIONS:

- Ratios:** 36:1, 18:1, 9:1 (Other ratios are available)
- Fine Synchro input:** Up to 14 bits
- Coarse Synchro input:** Up to 7 bits
- Logic:** Parallel, positive logic, TTL levels, binary coded angle
- Fan In:** 5 TTL Loads
- Digital Output:** Up to 21 bits
- Fan Out:** 3 TTL Loads
- Conversion Time:** 500 nanoseconds
- Gear Error:** 2° max. between coarse and fine synchros with full accuracy.
- DC Power required:** +5VDC ±5% at 800mA
- Operating Temperature:** Model C: 0°C to +70°C Model M: -55°C to +105°C
- Storage Temperature:** -65°C to +125°C
- Potting:** For high shock or vibration requirements units should be potted. Add "P" to part number.
- Weight:** 6.5 oz.

OUTPUT ACCURACY VS. REQUIRED INPUT BITS

Two Speed combined output	36:1 RATIO		18:1 RATIO		9:1 RATIO	
	Use Fine S/D Bits	Use Coarse S/D Bits	Use Fine S/D Bits	Use Coarse S/D Bits	Use Fine S/D Bits	Use Coarse S/D Bits
14 bits	1-10	1-7	1-10	1-6	1-11	1-5
15 bits	1-10	1-7	1-11	1-6	1-12	1-5
16 bits	1-11	1-7	1-12	1-6	1-13	1-5
17 bits	1-12	1-7	1-13	1-6	1-14	1-5
18 bits	1-13	1-7	1-14	1-6	---	---
19 bits	1-14	1-7	---	---	---	---

PART NUMBER DESIGNATION:

1510 * * * * *

- Add 883 for High Reliability
- Add P for Potting
- Add H for Hermetic seal
- Add Y for 21 bits
- Temperature range (C or M)

INTERCONNECTION:

For all ratios, output bits from 1651 Fine S/D converter are connected to Fine input of 1510 processor i.e. fine bit (1) out to fine bit (1) in through fine bit (14) out to fine bit (14) in.

For 36:1 Ratio:

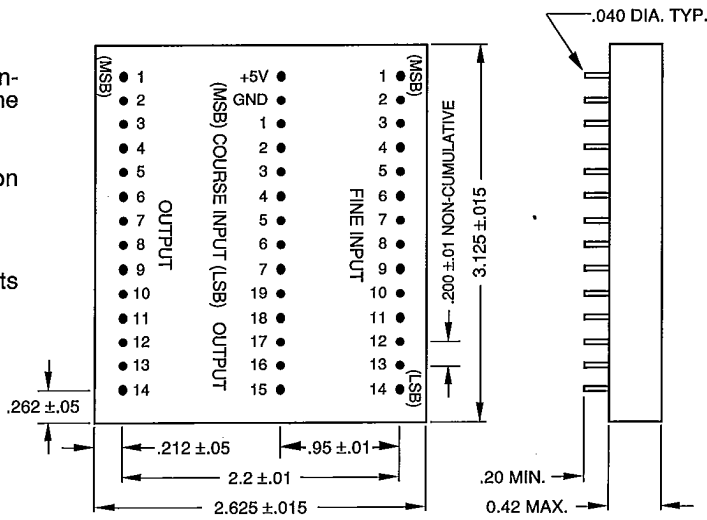
Connect bits 1-7 from 1651 coarse S/D to coarse input 1-7 on 1510 processor.
Outputs will be bits 1-19 (Bit 1 = 180°)

For 18:1 Ratio:

Connect output bits 1-6 from 1651 coarse S/D to coarse input bits 2-7 on 1510 processor.
Outputs will be bits 2-19 (Bit 2 = 180°)

For 9:1 Ratio:

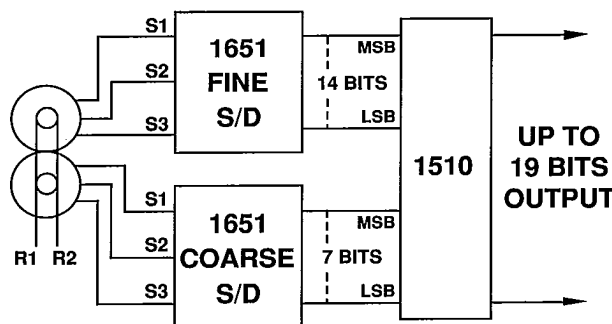
Connect output bits 1-5 from 1651 coarse S/D to coarse input bits 3-7 on 1510 processor.
Outputs will be bits 3-19 (Bit 3 = 180°)
Unused inputs should be grounded.
Unused outputs are to be left unconnected.



Application Notes:

Output data should be transferred after the trailing edge and before the next leading edge of the "CONVERTER BUSY" pulse produced by the fine converter only. The elapsed time between "CONVERTER BUSY" pulses depends on the rotational speed of the fine mechanical input angle and thus could be as short as 6µs at 3600 rpm. The "CONVERTER BUSY" from the coarse converter is not used because the maximum error introduced by the conversion process is the magnitude of the fine LSB.

Another transfer method is to freeze the data output with an applied "INHIBIT" signal. This signal must be applied to *both* converters for a minimum of 2µs before transferring data, thus allowing the converter to complete its conversion process and eliminating data ambiguity during data transfer.



DETERMINING THE AVAILABLE COMBINED ACCURACY AND RESOLUTION OF TWO SPEED SYSTEMS

Procedure:

1. The number of usable bits from the coarse synchro converter is determined by matching the result of 90 - gear ratio to the nearest value of Table 1.
 2. Two-speed resolution: Coarse bits + fine bits - 2 bits
 3. Two-speed accuracy: 1.5 LSB of two-speed resolution.
- EX. Gear ratio is 36:1 and two ten bit converters are available.
1. $90 \div 36 = 2.5$. Therefore 7 bits are used from coarse converter.
 2. Two-speed resolution: $7 + 10 - 2 = 15$ bits.
 3. Two-speed accuracy: 14 bits.

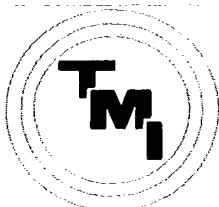
If we would substitute a 14 bit fine converter then:
Two-speed resolution: $7 + 14 - 2 = 19$ bits.
Two-speed accuracy: 18 bits.

TABLE 1

BITS AVAILABLE	RATIO
1	180
2	90
3	45
4	22.5
5	11.5
6	5.63
7	2.81
8	1.42

BINARY RATIO TWO SPEED CONVERTERS

4:1, 8:1, 16:1, 32:1 and 64:1 systems utilize our processor Models 1510-4, 1510-8, etc.
Application and interconnection are the same as for Model 1510.



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