XR-1010

Second Order Switched Capacitor Filter

EXAR ...the analog plus company™

October 1996–1

FEATURES

- Easy to Use: Simple Resistor Divider Equations for Filter Q
- No External Capacitors Needed to Set Corner Frequency
- Cascadable to Obtain Higher Order Filter Functions
- Pin-for-Pin Compatible With the National Semiconductor MF-10

APPLICATIONS

- Low Pass, High Pass, Band Pass, Notch & All Pass Filters
- Group Delay Compensation Filtering
- Modem Filters (CCITT V.21, V.23, V.26)
- Band Separation for Analog Front End
- Linear Phase Filtering (All Pole Filtering)
- Loop Filter for Phase-Lock Loops

GENERAL DESCRIPTION

The XR-1010 is a fully adjustable dual second order switched capacitor filter. With the intermediate nodes of the switched capacitor filter brought out, many different filter functions can be obtained. One half of the XR-1010 is composed of an operational amplifier, and two switched capacitor integrators. With the use of external resistors, to adjust the amplitude of the feedback, notch, band pass, all pass, low pass and high pass filter functions can be obtained.

By cascading the two halves of the XR-1010, a fourth order filter can be obtained. With the use of additional XR-1010, higher order filters can be obtained.

The XR-1010 is fabricated in polysilicon gate 3-micron CMOS. With single +6 VDC operation (at 250kHz) low power consumption can be obtained.

ORDERING INFORMATION

Part No.	Package	Operating Temperature Range
XR-1010CN	20 Lead 300 Mil CDIP	0°C to +70°C
XR-1010CP	20 Lead 300 Mil PDIP	0°C to +70°C
XR-1010CD	20 Lead 300 Mil JEDEC SOIC	0°C to +70°C

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BLOCK DIAGRAM

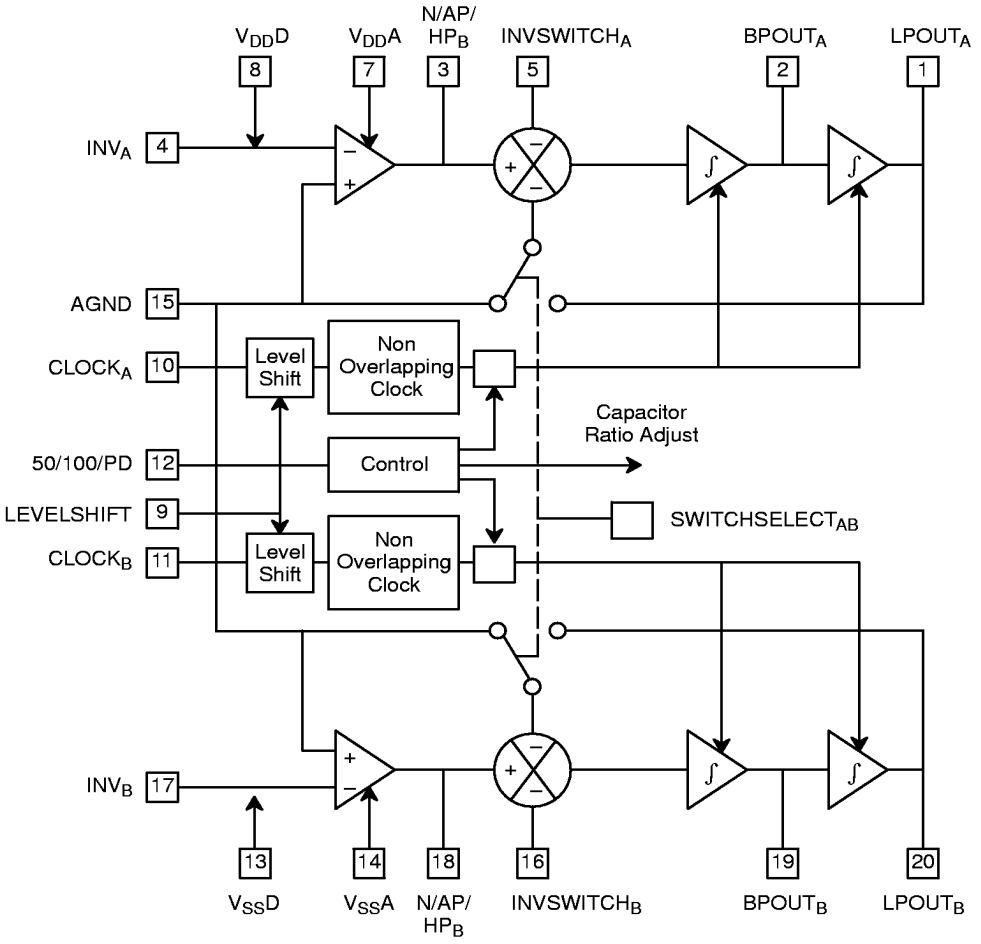
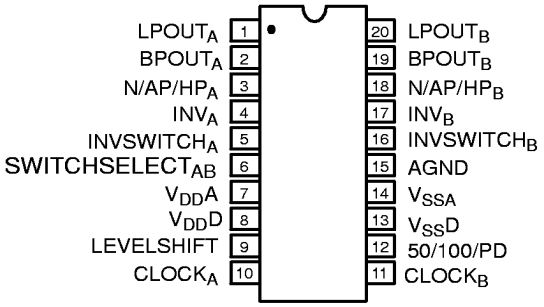
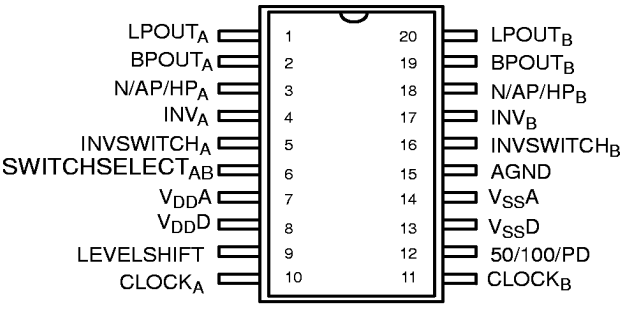


Figure 1. Block Diagram



20 Lead PDIP, CDIP (0.300")



20 Lead SOIC (Jedec, 0.300")

PIN DESCRIPTION

Pin#	Symbol	Desciption
1	LPOUT$_A$	**Low Pass Output A.** The output of the second switched capacitor integrator. The low pass filter function is obtained at this pin. It can typically drive a 10kΩ load.
2	BPOUT$_A$	**Band Pass Output A.** The output of the first switched capacitor integrator. The bandpass filter function would be obtained at this output. This output can typically drive a 10kΩ load.
3	N/AP/HP$_A$	**Notch/All Pass/High Pass Output.** This output provides the notch, all pass or high pass filter functions. The actual filter on the output is dependant upon the connection of external resistors and is described in the section on Modes of Operation.
4	INV$_A$	**Inverting Input A.** This is the inverting input of op amp A. It is normally used as the input for the filter function. Please note that the input impedance of the filter depends upon the value of the input resistor, R1, when used in some modes of operation. The noninverting input to this operational amplifier is tied internally to the AGND, Pin 15.
5	INVSWITCH$_A$	**Negative Switch Input A.** This input is used for the, filter input in some modes of operation. The input impedance of this point varies with the clock frequency. For typical operation the source for the signal applied here should be 1kΩ or less. With a 1 MHz sampling frequency, the input impedance is typically 20kΩ.
6	SWITCHSE-LECT$_{AB}$	**Signal Switch AB.** This logic input controls the other negative summing input of the filter. When low, the negative input of the summing section of the switched capacitor filter is connected to AGND, Pin 15. If this input is tied high, the other negative summing input is tied internally to the LP output. With this switch the various filter functions can be implemented. Please note that this input is not affected by the setting of LEVELSHIFT. A logic low is at V$_{SS}$; a logic high is at V$_{DD}$.
7	V$_{DD}$A	**Analog Positive Supply.** This input provides the positive voltage for the analog portions of the filter. It should be decoupled using a 0.68µF capacitor to ground. If it is known that the noise on the supply is large due to the use of a switching power supply, an additional 10µF capacitor should be used.
8	V$_{DD}$D	**Digital Positive Supply.** This input provides the positive voltage for the digital portions of the XR-1010. It should be decoupled with a 1.0µF capacitor to digital ground.
9	LEVELSHIFT	**Logic Level Select.** This input controls the acceptable clock input swing. With ±5 VDC operation, LEVELSHIFT should be tied to ground. This will allow either TTL or CMOS level clocks to be applied. With single supply operation, this pin should be tied to a voltage that is 1/2 of the algebraic sum of the supply voltages. This will allow input clocks at the V$_{SS}$ level to clock the XR-1010.

Pin#	Symbol	Description
10	$CLOCK_A$	**Clock Input A.** This is the clock input for the XR-1010 side A. It must be at the same levels as the clock applied to $CLOCK_B$. The frequency of this clock and the setting of 50/100/PD will determine the center frequency of the filter response. The sampling frequency is always one half of the clock frequency applied to CLOCK A.
11	$CLOCK_B$	**Clock Input B.** This is the clock input for the XR-1010 side B. The level applied can be either CMOS or TTL depending upon the voltage present on the pin LEVELSHIFT.
12	50/100/PD	**Clock to Corner/Power Down.** This input controls the clock to corner ratio as well as providing a power down standby mode. With this pin tied to V_{DD} (digital) the clock to corner ratio is set for 50:1. When this pin is tied to a voltage that is one-half of the sum of the amplitudes of V_{DD} and V_{SS}, the clock to corner ratio is 100:1. When this pin is tied to V_{SS}, the XR-1010 is in the power down mode and the filter no longer provides an output. If the INVSWITCH input is used, then the input impedance should be infinite. If other modes of operation are used with the op amp the impedance will depend on external resistor values.
13	$V_{SS}D$	**Negative Digital Supply.** This input provides the negative supply for the digital portions of the XR-1010. It should be decoupled with a 1 µF capacitor to digital ground.
14	$V_{SS}A$	**Negative Analog Supply.** This input provides the negative supply for the analog portions of the XR-1010. It should have a 0.68µF ceramic capacitor to decouple any noise to analog ground. If the analog negative supply is known to be noisy such as from a switching power supply, then an additional 1µF capacitor for decoupling of the supply should be used.
15	AGND	**Analog Reference.** This input is used for providing the reference for the analog signals applied to the XR-1010. With equal split supplies, this pin should be tied to the analog ground of the system. When single supplies or unequal split supplies are used, then this input should be biased to a point that is one half of the algebraic sum of the V_{DD} and V_{SS} voltages. In this application, the AGND pin should be decoupled to the system ground with a 0.68µF capacitor.
16	$INVSWITCH_B$	**Negative Switch Input B.** This is the negative switch input used for producing the various filter responses. Its input impedance varies with the clocking frequency. When it is being used as an input, the signal source should be 1kΩ or less in output impedance. With a 1MHz sampling clock, the input impedance is typically 20kΩ. As the sampling frequency decreases, the input impedance increases.
17	INV_B	**Inverting Input B.** This is the inverting input of operational amplifier B. It is normally used as the input for the filter function.
18	$N/AP/HP_B$	**Notch, All Pass, High Pass Output B.** This output provides three of the filter functions as well as a source for feedback for producing other filter functions.
19	$BPOUT_B$	**Band Pass Filter Output B.** This output provides the band pass filter response as well as a a source for feedback signals for other filter functions. This output is typically capable of driving a 10kΩ load.
20	$LPOUT_B$	**Low Pass Filter Output B.** This provides the low pass filter response. It is capable of driving a 10kΩ load.

ELECTRICAL CHARACTERISTICS

Test Conditions: V+ = 5V, V– =–5V, f_{clock} = 1MHz, R_{load} = 1 MΩ, C_{load} = 40pF, T_A = 25°C: Mode 1 with R1 = 100kΩ, R2 = 10kΩ, and R3 = 100kΩ, unless specified otherwise.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
General Characteristics						
V_{DD}	Positive Supply Voltage		5.0	5.25	V	f_{clock} = 1MHz
		3			V	f_{clock} = 250kHz
V_{SS}	Negative Supply Voltage	–5.25	–5.0		V	f_{clock} = 2MHz
				–3	V	f_{clock} = 250kHz
I_{DD}	Current on V_{DD}		10	15	mA	
I_{SS}	Current on V_{SS}	–15	–10		mA	
I_{PDDD}	Power Down Current		300		µA	Pin 12 = –5 VDC
Filter Characteristics						
f_o	Frequency Range	20	30		kHz	Pin 12 High
$f_{clock\ /\ fo}$	Clock-to-Corner Frequency Ratio		49.94	±3.5	%	Pin 12 High
			99.35	±3.5	%	Pin 12 at 0V
Q	Accuracy of f_O Bandwidth			±8	%	Q = 10, f_o x Q 200kHz
f_{clock}	Maximum Clock Frequency	1	1.5		MHz	
$H_{lowpass}$	DC Low Pass Gain Accuracy			12%		
	Crosstalk		70		dB	
	Clock Feedthrough		30		mVpp	f_{clock} = 1MHz
V_{IN}	Maximum Input (Unclipped)	8			Vpp	A_V = 1 V/V
THD	Total Harmonic Distortion		0.1%			Input Level = 1 Vpp
tco_Q	Temperature Coefficient of Q		700		ppm/°C	From –40°C to +85°C not tested in production
	Temperature Coefficient of f_o		120		ppm/°C	From –40°C to +85°C not tested in production
Operational Amplifier Characteristics						
GBW	Gain Bandwidth Product		2.5		MHz	
I_{OSS}	Output Short Circuit Current					
	Source		26		mA	
	Sink		-1.5		mA	

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS

Power Supply . . . . . 14 V_{DC}
Input Signal Level (Logic) V_{DD} +0.3 to V_{SS} –0.3 V_{DC}
Power Dissipation (Package Limitation)
Ceramic Package 1.3W
Derate Above 25°C . . . . . 5 mW/°C
Plastic Package 1.0W
Derate Above 25°C . . . . . 8 mW/°C
Storage Temperature . . . . . –55°C to +150°C

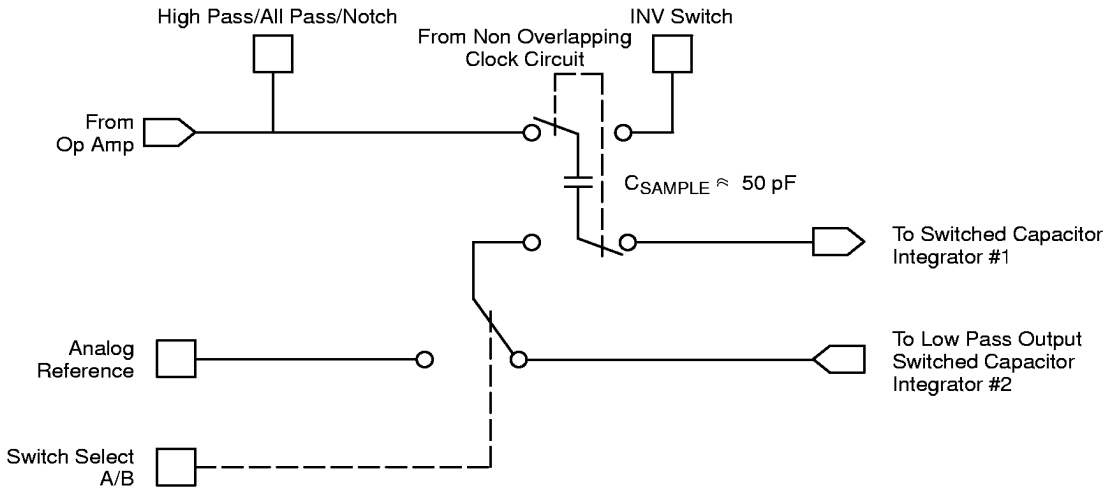


Figure 2. Detail Switched Capacitor Summer

SYSTEM DESCRIPTION

The XR-1010 can be operated with either dual supplies or with a single supply. The center frequency of the filter response is set precisely by the clock frequency. This clock to center ratio can be changed with the use of the 50/100/PD pin on the XR-1010. Either TTL or CMOS clocks can be used.

With the use of external resistors to control the amplitude of the feedback, many different filter functions can be obtained with the XR-1010. Simple algebraic calculations allow for the determination of the values of the resistor to obtain the filter shape needed.

PRINCIPLES OF OPERATION

The XR-1010 is a dual second order switched capacitor state variable filter. Since the state variable filter provides all of the basic filter functions at the same time, it is the most versatile building block to use. With only a few external feedback resistors, band pass, low pass, high pass, notch, and all pass filter functions can be obtained.

With the switched capacitor implementation of the state variable filter, capacitors, switched at a certain frequency will simulate resistors of a particular value. To allow greater flexibility, the feedback resistors to create the particular filter function are external to the device.

Since switched capacitor filters are sampled data systems, in that they divide a continuous time signal into samples of charge, some thought must be given to out-of-band signals causing an aliased component to appear in the band of interest. To prevent the appearance of aliased signals, there should be at least two samples per cycle of signal applied to the input of the XR-1010. The sampling frequency of the filter is 1/2 of the clock frequency applied to Pin 10 and 11.

One reference on the subject of sampled data systems is the book “Digital Signal Processing” by Oppenheim and Schaffer, published by Prentice Hall. This book fully covers the concept of aliased signals as well as the Nyquist Criteria.

SELECTION OF MODE

Table 1. shows which mode can provide which filter shape. Also shown in the table is which input is used. This helps to determine the most efficient use of the dual XR-1010 since Pin 6, $SWITCHSELECT_{AB}$ controls both sides of the XR-1010.

If one of the modes selected requires the internal feedback path from the low pass filter output to the switched capacitor summer mode, then the mode for the second half must have the same configuration, although not necessarily the same mode. This is not normally a problem since in most designs, both halves are used to obtain the final filter function needed.

OFFSET VOLTAGES

With any operational amplifier or integrator circuit, some offset voltage is seen on the output. The XR-1010 output offset voltages typically are less than 100mV. This in most applications is neglible.

If the output offset voltage is not acceptable, then typical offset compensation circuits can be employed, as used with any operational amplifier.

	Mode 1	Mode 1a	Mode 2	Mode 3	Mode 3a	Mode 4	Mode 5	Mode 6a	Mode 6b
Low Pass	yes	yes	yes	yes	yes	yes	yes	yes	inv. non-inv.
High Pass	no	no	no	yes	yes	no	Note[1]	yes	no
Band Pass	yes	inv. non-inv.	yes	yes	yes	yes	yes	no	no
Notch	yes	no	yes	no	yes	no	yes	no	no
All Pass	no	no	no	no	no	yes	yes	no	no
Input Used	Op Amp	Inv. Switch	OP Amp	OP Amp	OP Amp	OP Amp & Inv. Switch	OP Amp & Inv. Switch	OP Amp	Inv. Switch

Notes
[1]Depends on Band Pass location

Table 1. Filter Shapes Available with a Particular Mode

GLOSSARY

f_{CLOCK} The frequency of the clock applied to the switched capacitor filter. It is this clock that will determine the position of the corner or center of the filter (along with 50/100/PD).

f_O The center frequency of the filter. This also sets the complex pole pair of the filter. *Figure 3.* shows a normalized complex pole pair on the jω vs. ω axis. *Figure 4.* shows the response seen on the band pass filter output with this pole pair position. f_{center} corresponds to the peak of the band pass filter.

Q The quality of the filter. With a band pass filter it is defined as the center frequency of the band pass response divided by the –3dB bandwidth of the band pass filter.

The Q of the filter also indicates the position of the complex conjugate pole positions. *Figure 5.* shows the position of the complex pole positions and *Figure 6.* shows its affect on the band pass filter's –3dB bandwidth.

$H_{bandpass}$ The gain of the band pass filter at $f_o = f_{center}$. This parameter is unit-less.

$H_{lowpass}$ The gain of the low pass filter as f approaches 0Hz. This is shown in *Figure 7.*

$H_{highpass}$ The gain of the high pass filter output as f_o approaches $f_{clock}/2$. This is shown in *Figure 8.*

Q_{zero} The quality of the complex zero pair. This specification has no units. It is difficult to measure this specification externally from the band pass output. *Figure 9.* shows the effect of a particular complex zero position on a output frequency response.

Figure 10. also shows an all pass filter response. This synthesized filter response has no amplitude ripple which would be the ideal response. *Figure 11.* shows the phase response of the all pass filter.

f_{zero} The center frequency of the notch as see at the N/AP/HP output.

f_{notch} The center frequency of the notch as seen at the N/AP/HP output.

$H_{notch@0}$ The gain of the notch output as f_{notch} approaches 0Hz.

$H_{notch@fclock/2}$ The gain of the notch output as f_{notch} approaches $f_{clock}/2$.

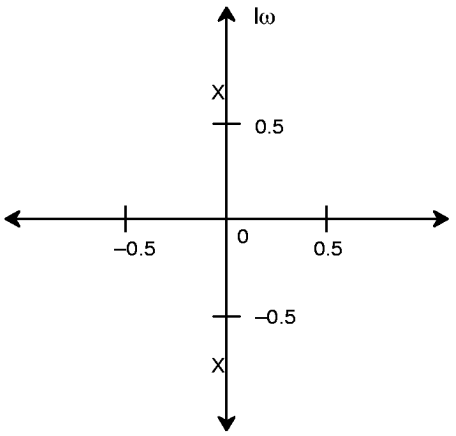


Figure 3. Band Pass Complex Pole Position

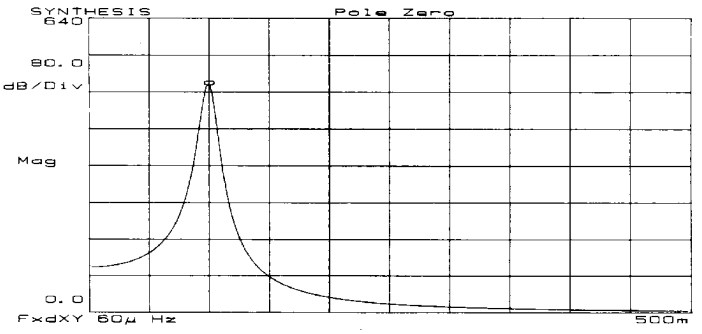


Figure 4. Band Pass Filter

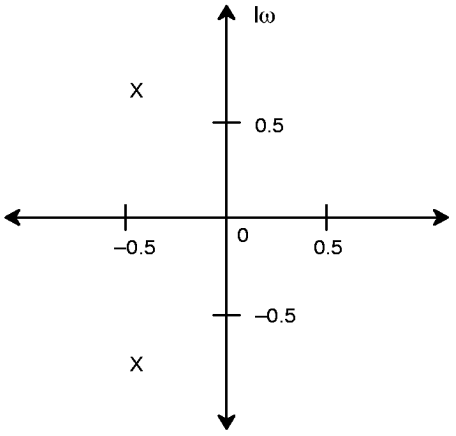


Figure 5. Low Pass Complex Pole Position.

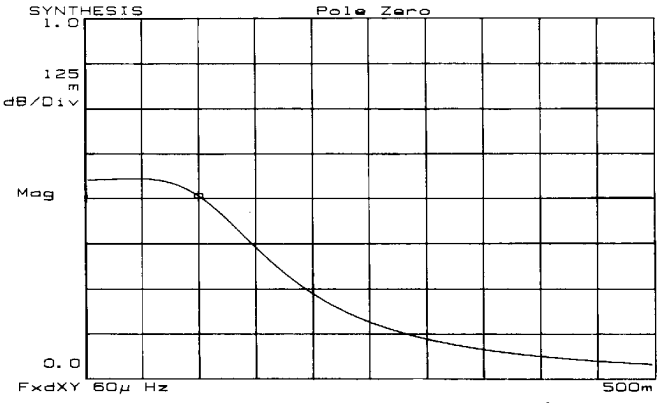


Figure 6. Low Pass Filter.

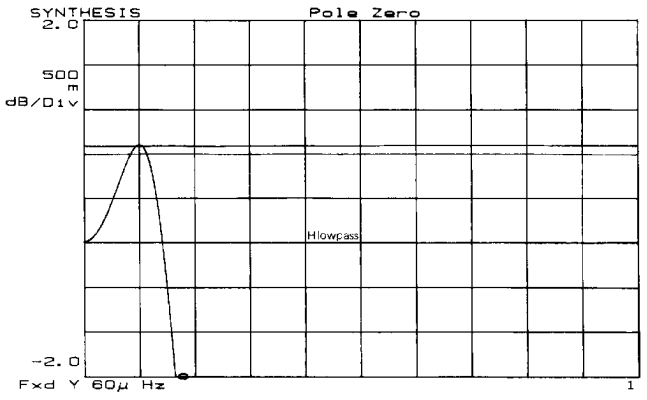


Figure 7. Definition of $H_{LOWPASS}$

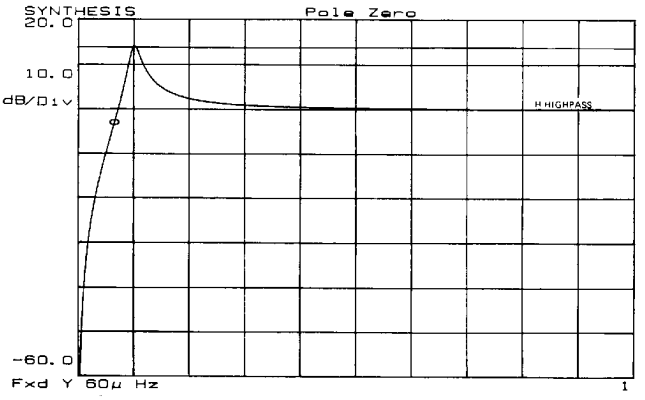


Figure 8. Definition of $H_{HIGHPASS}$

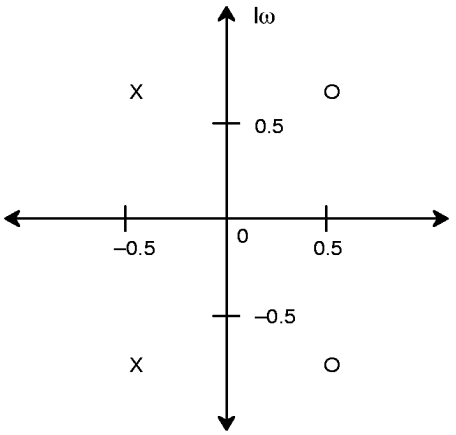


Figure 9. All Pass Filter

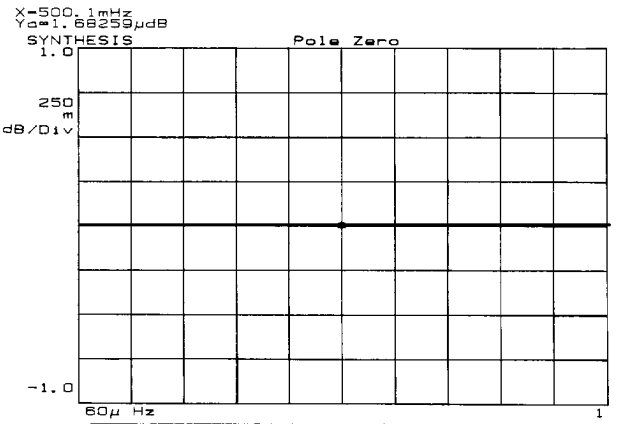


Figure 10. Amplitude Response of a Perfect All Pass Filter

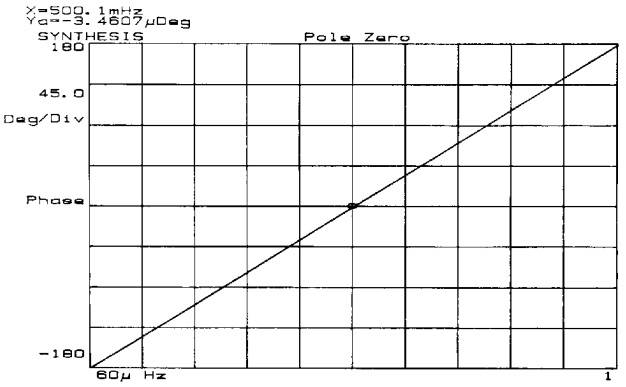


Figure 11. Phase Response of a Perfect All Pass Filter

MODES OF OPERATION

The XR-1010 is a switched capacitor filter using switched capacitors to simulate resistors and controlled feedback to simulate inductors. This is a sampled data device which is most easily studied in the frequency domain.

The value of the resistors control the amount of feedback, and consequently, the gain of the filter responses and the Q of the filters. The following are the formulas used to calculate the resistor values needed to obtain the various filter responses.

Mode 1: Inverting Notch, Bandpass or Lowpass Filter Response

This mode involves a small number of external resistors. High Q band pass filters can be constructed with this circuit, however at the same time, the gain of the low pass filter response is dependent on the Q of the bandpass filter. The gain of all outputs are controlled by a separate feedback resistor. *Figure 12.* shows the connections to be made to side A of the XR-1010.

$$F_o = \frac{f_{clock}}{100} \text{ or } \frac{f_{clock}}{50}$$

depending on the level at 50/100/PD.

$$H_{lowpass} = -\frac{R2}{R1}$$

Please note that in this configuration R1 is the input impedance of the filter. In this fashion, the formula becomes an equation with only one unknown, R_2, the amount of feedback.

$$f_{zero} = f_o$$

The center frequency of the complex zero pair is equal to the center frequency of the real pole pair. In this mode, the uncertainty of the position of the zero is reduced.

$$H_{bandpass} = -\frac{R3}{R1}$$

The gain of the band pass filter at the center frequency is set by this resistor ratio.

$$H_{notch} = -\frac{R2}{R1}$$

The gain of the notch filter output as fo approaches 0Hz or as f_O approaches $f_{clock}/2$. Please note that the depth of the notch is a factor band pass filter's Q.

$$Q = \frac{R3}{R2}$$

The quality factor of the second order pole pair is control led by the ratio of R3/R2. This quality is also defined by f_0/bandwidth where the bandwidth is the –3dB points of the band pass filter.

Dynamic Gain Calculations

$$H_{bandpass} = H_{lowpass} \times Q$$
$$H_{bandpass} = H_{notch} \times Q$$

This can be seen through the algebraic manipulations of the formula for notch low pass and Q from above. It can be seen from this that the device gain of the bandpass filter is independent of the Q of the filter.

$$H_{lowpass(peak)} = Q \times H_{lowpass}$$

The gain of the low pass filter is affected by the Q of the filter at the center frequency of the band pass filter. If clipping of the low pass filter output occurs, the feedback of this clipping used to create the band pass response will cause distortion.

Mode 1a: Inverting Band Pass, Non-inverting Band Pass, and Low Pass Filter Responses

This is the simplest configuration of the XR-1010, requiring only two external resistors. Please refer to *Figure 13.* for details.

$$f_o = \frac{f_{clock}}{100} \text{ or } f_o = \frac{f_{clock}}{50}$$

Depending on the level at Pin 12, 50/100/PD.

$$Q = \frac{R3}{R2}$$

The Q and the gain of the band pass are related. In the situation of large Q values, clipping may occur at certain signal levels.

$H_{lowpass} = 1$

This is due to the unity gain configuration.

$H_{lowpass}@f_o = Q \times H_{lowpass}$

This is true for applications with high Q values.

$$H_{bandpass(inverting)} = -\frac{R3}{R2}$$

Dynamic Calculations

$$H_{bandpass(inverting)} = Q$$

If the input signal is too large, the output at this pin will be clipped causing an increase of noise. Clipping at this output will affect the device operation at other outputs.

$$H_{lowpass(peak)} = Q \times H_{lowpass}$$

This is true in the case of high Q filter. This again shows the importance of preventing clipping from occurring in the filter. Such clipping would not be normally visible on the low pass filter output, but, this would affect the performance.

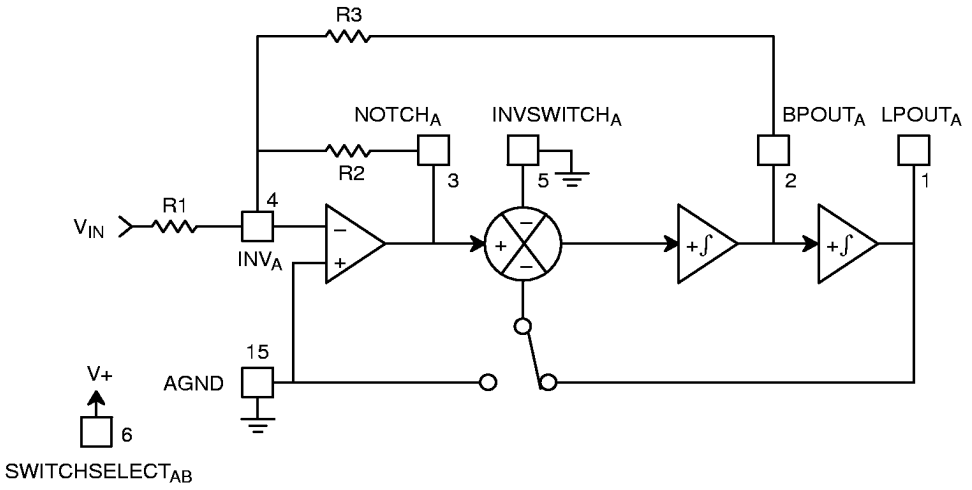


Figure 12. Mode 1 Shown for Side A of XR-1010

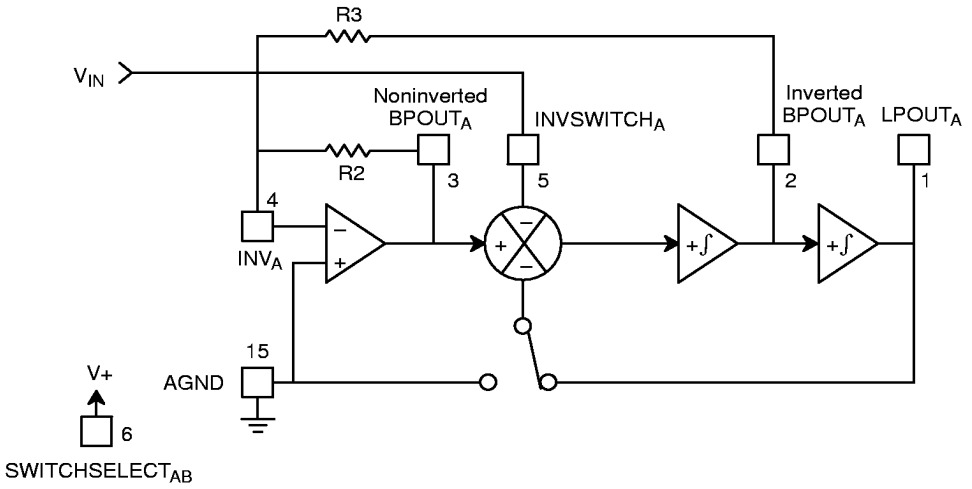


Figure 13. Mode 1A

This mode can provide a very large gain band pass filter due to the effect of the Q on the filter gain. It is not normally recommended for high Q filters due to the danger of clipping the inverting band pass output. The clock-to-corner ratio is fixed in this mode of operation due to the simplicity of the feedback of the filter.

The signal input impedance, Pin 5 or Pin 16, will vary with the clock frequency. With a clock frequency of 1 MHz, the input impedance is 20kΩ typically.

Mode 2: $Notch_{mode2}$ (f_{notch} less than f_o) Band Pass, Low Pass Filters

Mode 2 provides adjustment of the center frequency of the band pass and low pass filters. This is done through the use of the feedback resistor R4. Please note that in Mode 2, the feedback path of the low pass filter output is through R4 to the inverting input of the operational amplifier, Pin 4 (17) as well as to the inverting input of the switched summing circuit. *Figure 14.* provides the detail for connection of the external resistors for side A of the XR-1010. Mode 2 is best suited for notch filter applications since the clock-to-corner ratio is reduced for the other shape.

Design Equations

$$f_o = \frac{f_{clock}}{100}\left(\frac{R2}{R4}+1\right)^{1/2} \text{ or } f_o = \frac{f_{clock}}{50}\left(\frac{R2}{R4}+1\right)^{1/2}$$

depending on the level at Pin 12, 50/100/PD. It should be noted that the f_o frequency must be greater than 100 times (50 times – Pin 12 high) the clock frequency or negative resistance will result when these equations are used.

$$f_{notch} = \frac{f_{clock}}{50} \text{ or } f_{notch} = \frac{f_{clock}}{100}$$

depending on the level set on Pin 12, 50/100/PD.

$$Q = \left(1+\frac{R2}{R4}\right)^{1/2}\frac{R2}{R3}$$

The Q of the filter is related to the gain of the low pass and notch filter as well as the band pass gain.

$$H_{lowpass} = \frac{-\frac{R2}{R1}}{\frac{R2}{R4}+1}$$

$$H_{notch} = \frac{-\frac{R2}{R1}}{\frac{R2}{R4}+1}$$

The low pass filter gain is the same as the gain for the notch filter as f_o approaches 0Hz.

Mode 3: Inverting High Pass, Band Pass, and Low Pass Filters

This circuit allows high Q band pass filters with the ability to adjust the band pass filter gain without significantly affecting the Q of the filter. It is also possible to obtain a shift in the f_{corner} or the f_o of the filter with the adjustment of the values of the resistors R2 and R4, as shown in the equations below. This allows, with a single clock frequency, multiple-pole filters. *Figure 15.* shows the external resistor interconnections.

Design Equations

$$f_o = \frac{f_{clock}}{100}\left(\frac{R2}{R4}\right)^{1/2}$$

This formula calculates the center frequency of the band pass filter, or the corner frequency of the low pass filter. When 50/100/PD is tied to ground. It is with the adjustment of the value of R2 and R4 that the variation of the center frequency or the corner frequency is obtained.

$$f_o = \frac{f_{clock}}{50}\left(\frac{R2}{R4}\right)^{1/2}$$

This formula is used if Pin 12, 50/100/PD is tied to V+.

$$Q = \frac{R3}{R2}\left(\frac{R2}{R4}\right)^{1/2}$$

The Q of the filter is affected by the value of the feedback resistors R2 and R4 as well.

$$H_{highpass} = -\frac{R2}{R1}$$

It can be seen that the adjustment of the gain of the high pass filter output will have some effect on the Q of the filter as well as on the f_o of the filter outputs.

$$H_{bandpass} = -\frac{R3}{R1}$$

The gain of the band pass filter output will affect the Q of the filter.

$$H_{lowpass} = -\frac{R4}{R1}$$

The gain of the low pass filter output will have some effect on the f_o of the filter as well as on the Q of the filter.

Equations for Dynamic Circuit Operation

$$H_{highpass} = H_{lowpass}$$

This equation shows that the band pass filter will be affected by the Q of the filter as well as by the amount of shift created by the ratio R2 of the corner frequency.

$$H_{lowpass\ @\ f_o} = Q \times H_{lowpass}$$

The Q of the filter will have an effect on the amount of gain at the corner frequency of the low pass response. In situations of extremely large values of Q, this can cause clipping and should be considered.

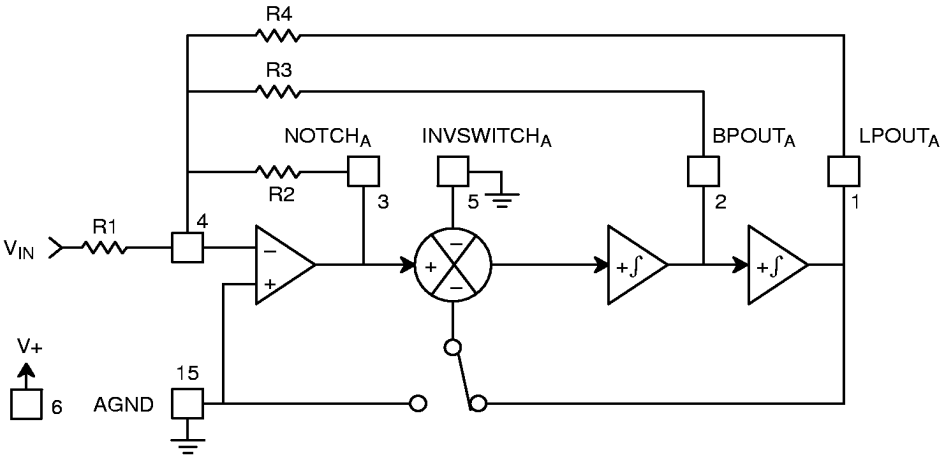


Figure 14. Mode 2

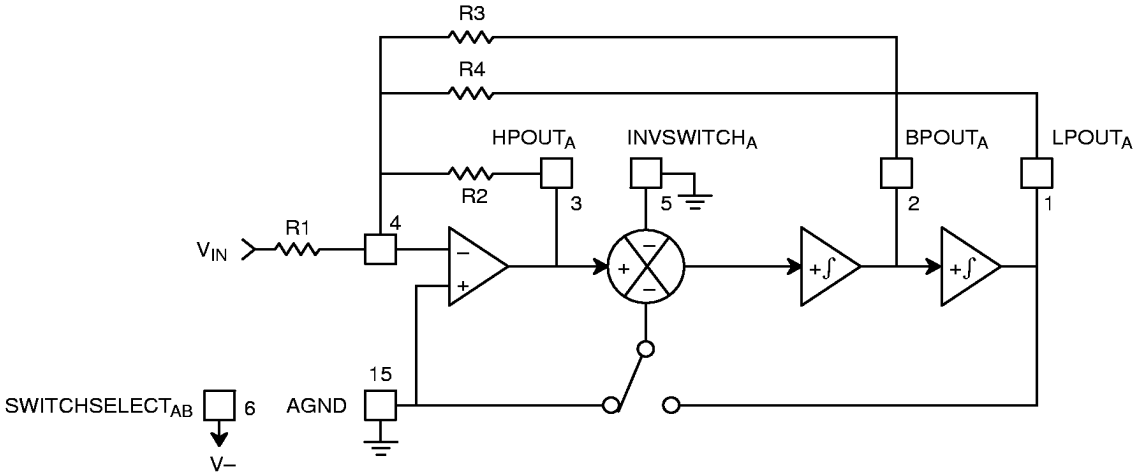


Figure 15. Mode 3

$$H_{bandpass} = (Q \times H_{highpass} \times HI_{owpass})^{1/2}$$

The Q of the filter will have an effect on the gain of band pass filter output. The gain of the high pass and low pass filters will also have some effect on the band pass filter gain.

Mode 3A: High Pass, Band Pass, Low Pass and Notch Filters

With the addition of an external operational amplifier a notch filter can be obtained from the same circuit as Mode 3. The output of the high pass and the low pass filter are summed to obtain a notch filter response. The limitation of the notch depth will be the slope of the rolloff of the high pass and low pass filter responses. An operational amplifier with a large gain bandwidth product is recommended to minimize its effect on the filter response.

Figure 16. gives the details as to the filter configuration.

Design Equations

$$f_o = \frac{f_{clock}}{100}\left(\frac{R2}{R4}\right)^{1/2}$$

The center frequency of the notch or band pass filter or the corner frequency of the low pass can be adjusted to some degree by the ratio of the low pass and high pass filter gain resistors. This formula is used if Pin 12, 50/100/PD is tied to analog ground.

$$f_o = \frac{f_{clock}}{50}\left(\frac{R2}{R4}\right)^{1/2}$$

This formula is used if 50/100/PD is tied to V_{DD}.

$$f_{notch} = \frac{f_{clock}}{50}\left(\frac{R2}{R4}\right)^{1/2} \text{ or } f_{notch} = \frac{f_{clock}}{100}\left(\frac{R2}{R4}\right)^{1/2}$$

The notch filter center frequency at the output of the external operational amplifier.

$$H_{bandpass} = -\frac{R3}{R1}$$

The gain of the band pass filter output is controlled by the ratio between the feedback resistor (R2) and the input resistance (R1).

$$H_{highpass} = -\frac{R2}{R1}$$

The gain of the high pass filter output is controlled by the ratio between the feedback resistor R2 (operational amplifier output to inverting input) and the input resistor R1.

$$H_{lowpass} = -\frac{R4}{R1}$$

The gain of the low pass filter output is adjusted by the ratio between the feedback resistor R4 (integrator 2 output to inverting input of operational amplifier) and resistor R1.

$$H_{notch@0} = \frac{R_{gain}}{R_{lowpass}}\left(\frac{R4}{R1}\right)$$

The gain of the notch filter as the input frequency approaches 0Hz can be calculated using the formula at left. From *Figure 16.*, it can be seen that the gain of the external operational amplifier will affect the gain seen at the notch output. Also, this does allow some adjustment to the gain of the pass band of the notch filter without affecting the gain of the low pass filter output.

The outputs of the XR-1010 can typically drive a 10kΩ load. The parallel combination of R4 and $R_{lowpass}$ should be 10 kΩ or greater.

$$H_{notch@f_{clock}} = \frac{R_{gain}}{R_{lowpass}}\left(\frac{R2}{R1}\right)$$

The gain of the notch filter output as the input frequency approaches f_{clock} is calculated using the equation at left. *Figure 16.* shows how the gain of the high pass filter output can be adjusted independently of the notch filter gain. Care should be taken to ensure that clipping of the signal does not occur, due to excessive gain set at the notch filter output.

It should be considered that the output of the XR-1010 can drive 10 kΩ typically. Care should be taken so that the parallel combination of the feedback resistor R2 and the input resistor $R_{lowpass}$ is not less than 20kΩ.

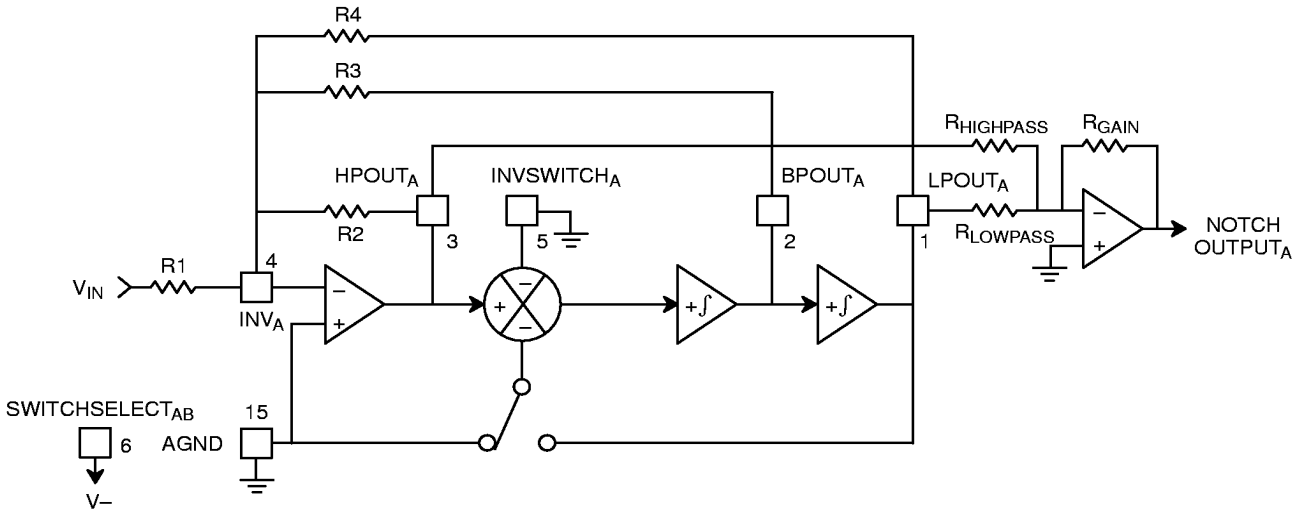


Figure 16. Mode 3A

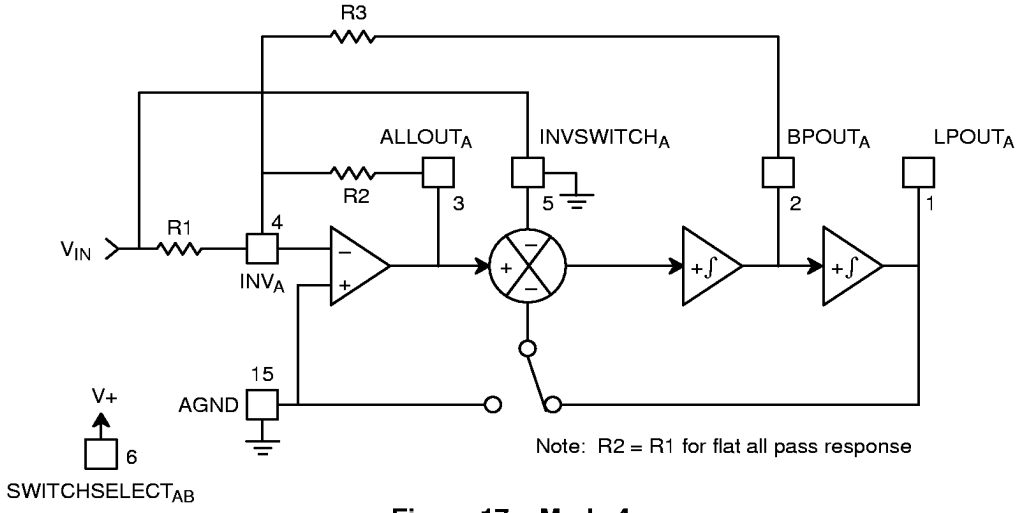


Figure 17. Mode 4

Mode 4: All Pass, Band Pass, and Low Pass Filtering

This mode provides an inverted all pass, band pass, and low pass filter output. Through variation of the f_{clock}, the amount of delay through the all pass filter can be varied. The output gain of the all pass filter is fixed at –1 to reduce the amount of ripple. Unlike other all pass filters, the XR-1010 has typically less than 1dB of ripple in the response of the all pass filter output. This allows the use of Mode 4 in any all pass system. The f_O in this mode is fixed to either 100:1 or 50:1.

Figure 17. shows the external connections for Mode 4. As with the other circuits, it is important that the connections to the inverting input of the operational amplifier should be kept short to prevent noise pickup. *Figure 18. and Figure 19.* show the change in delay for f_{clock} = 500kHz and f_{clock} = 1MHz. From this, it can be determined that for maximum delay, the frequency of the clock should be decreased within the limits of the maximum input frequency.

Design Equations

$$f_o = \frac{f_{clock}}{100}$$

The center or corner frequency of the filter responses does not vary with the adjustment of the resistor values. The formula above is used when Pin 12, 50/100/PD is tied to 0 VDC.

$$f_o = \frac{f_{clock}}{100}$$

The formula above is used when the 50/100/PD pin is tied to V+.

The f_o of the complex zero pair is approximately equal to the f_o of the complex pole.

$$Q = \frac{R3}{R2}$$

The Q of the band pass filter output can be calculated using the equation above. In the case of the large Q, this will have some effect on the gain of the low pass filter outputs at fcorner.

$$Q_{zero} = \frac{R3}{R1}$$

The Q of the complex zero pair which cannot be measured externally.

$$H_{allpass} = -\frac{R2}{R1}$$

The gain of the all pass filter output should be set to –1 (R2 = R1). When R2 is larger than R1, a slope will appear on the all pass output.

$$H_{bandpass} = -2\left(\frac{R3}{R1}\right)$$

The gain of the band pass filter output is controlled by the ratio of R3 to R1.

$$H_{lowpass} = -2\left(\frac{V}{V}\right)$$

The gain of the low pass filter output is fixed at –2 where f_o approaches 0Hz. This can be seen by the two inputs used in this mode (Mode 4). One input is applied directly to the INVSWITCH input. The second is applied through R1 to the inverting input of the operational amplifier. At the switched capacitor summer, the amplitude of the two signals would be equal in amplitude (@ 180°) providing twice the amplitude to be applied to the low pass integrator.

Mode 5: Complex Zero, Band Pass and Low Pass Filter Outputs

This mode provides additional flexibility over Mode 4, in that the complex zero location can be moved separately from the complex pole position. This can reduce the amount of ripple in the all pass response, as well as provide additional control over the position of the corner frequency of the low pass filter and the center frequency of the band pass filter output. Please see *Figure 21.*

Design Equations

$$f_o = \left(1 + \frac{R2}{R4}\right)^{1/2}\left(\frac{f_{clock}}{100}\right)$$

The formula above calculates the corner or center frequency of the XR-1010 filter outputs when Pin 12, 50/100/PD is tied to analog ground.

$$f_o = \left(1 + \frac{R2}{R4}\right)^{1/2}\left(\frac{f_{clock}}{50}\right)$$

When 50/100/PD is tied to V_{DD}, the formula above should be used. This formula shows the advantage that Mode 5 has over Mode 4 in that the corner or center frequency of the filter can be moved relative to the fixed clock-to-corner ratio.

If only a small change to the clock-to-corner (center) ratio is desired, then R4 can be made larger. However, this will have a direct effect on the gain of the low pass filter output. Clipping on the output of the low pass filter could occur, which would affect the other filter outputs.

$$f_{zero} = \left(1 - \frac{R1}{R4}\right)^{1/2}\left(\frac{f_{clock}}{100}\right)$$

The equation above is used for calculating the location of the complex zero pair, when Pin 12, 50/100/PD is tied to ground. With the ability of moving the complex zero to a location of the pole, many different filter shapes can be obtained.

In the case of a large value for R1 and a small value of R4, the location of the zero would be close to 0Hz. The equation is not defined for values of R1/R4 which are greater than or equal to 1.

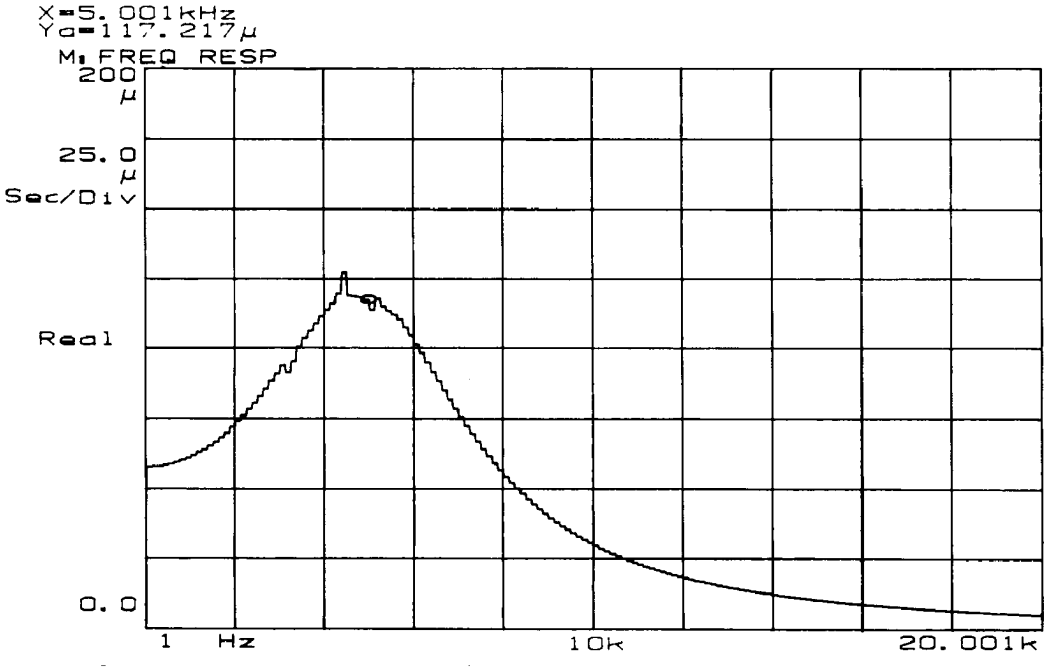


Figure 18. Delay of Mode 4 All Pass Output f_{clock} = 500kHz

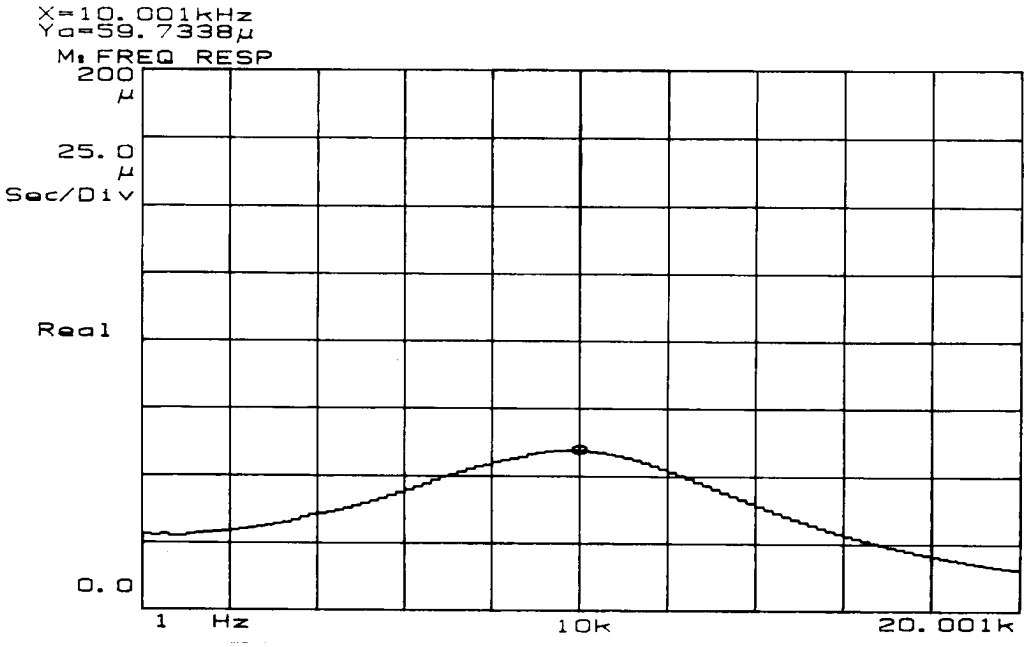


Figure 19. Delay of Mode 4 All Pass Output f_{clock} = 1MHz

$$f_{zero} = \left(1-\frac{R1}{R4}\right)^{1/2} \left(\frac{f_{clock}}{50}\right)$$

This equation is used when Pin 12, 50/100/PD is tied to V_{DD}.

$$Q_{pole} = \left(1+\frac{R2}{R4}\right)^{1/2} \left(\frac{R3}{R2}\right)$$

The equation above calculates the quality of the filter relative to the complex pole pair. With the variation of R3 (band pass feedback) and R4 (inverting low pass filter feedback), the magnitude of the real component can be varied.

$$Q_{zero} = \left(1-\frac{R2}{R4}\right)^{1/2} \left(\frac{R3}{R1}\right)$$

This equation is used to calculate the quality of the complex zero pair. The magnitude of R4 (inverting low pass filter feedback) and R3 (band pass filter feedback) control the location of the zero on the jω, ω axis.

This formula works well with large values (relative to R2) of resistance of R4. When R4 becomes equal to, or smaller than R2, the formula becomes meaningless.

The Q_{zero} in such a case is much less than 1 and does not have any practical use.

$$H_{zero\,@\,0} = \frac{R2(R4-R1)}{R1(R2+R4)}$$

The gain on the output of the complex zero filter as the input frequency approaches 0Hz is calculated by this formula.

$$H_{zero} \,@\, f_{clock}/2 = -\frac{R2}{R1}$$

As the input frequency approaches $f_{clock}/2$, the gain of the output is limited by the gain of the operational amplifier.

$$H_{bandpass} = \left(\frac{R2}{R4}+1\right)\left(\frac{R3}{R2}\right)$$

The gain of the bandpass filter at f_O is calculated using the formula above.

$$H_{lowpass} = \left(\frac{R2+R1}{R2+R4}\right)\left(\frac{R4}{R1}\right)$$

The formula above is used to calculate the gain of the low pass filter as f_O approaches 0 Hz. The response of the filter near the corner frequency is affected by the gain of the band pass filter.

Mode 6a: First Order Clock Controlled High Pass and Low Pass Filter (Inverted)

This mode allows the construction of first order high pass and low pass filters with the f_{corner} adjustable from the clock frequency or by adjusting the resistor ratios. This is far more useful than the continuous time RC version, since the XR-1010 will track any other stage in the system.

The output of the second integrator is not normally used. The output is typically near V_{DD} or V_{SS}.

Design Equations

$$f_o = \left(\frac{f_{clock}}{50}\right)\left(\frac{R2}{R3}\right)$$

This equation is used for calculation of the position of the corner frequency of the low pass filter or the high pass filter when Pin 12, 50/100/PD is tied to V_{DD}.

$$f_o = \left(\frac{f_{clock}}{100}\right)\left(\frac{R2}{R3}\right)$$

This equation is used when Pin 12, 50/100/PD is tied to analog reference. Please note that if the gain of the low pass and high pass filter outputs is not the same, the clock-to-corner ratio will be affected.

$$H_{highpass} = -\frac{R2}{R1}$$

This formula is used to calculate the gain of the high pass filter output.

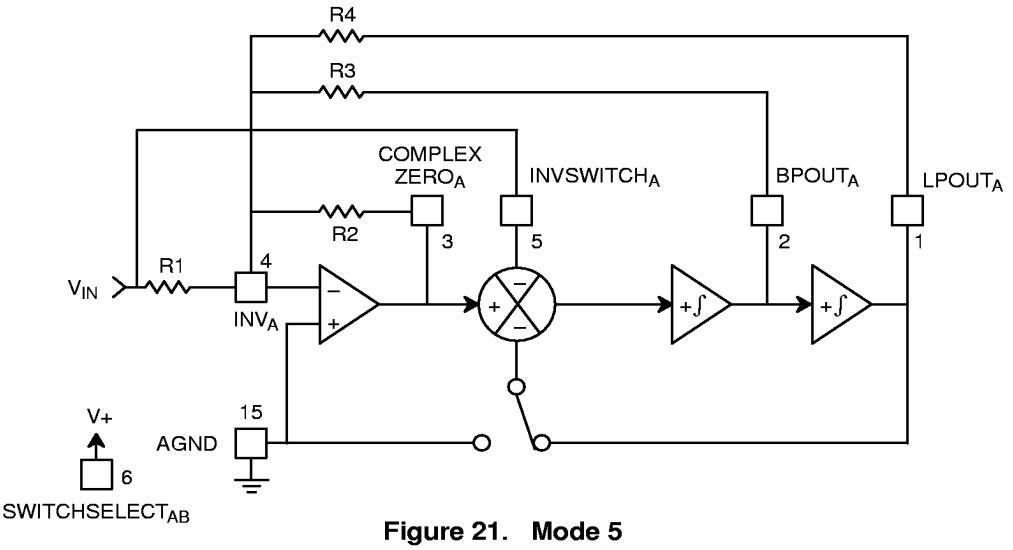


Figure 21. Mode 5

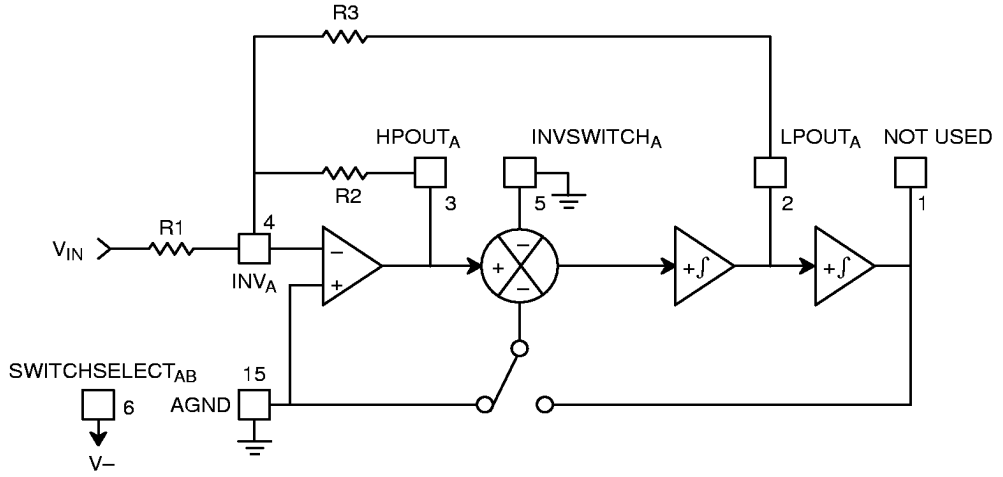


Figure 20. Mode 6A

Mode 6b: Single Pole Low Pass Filter – Inverting and Non-Inverting Output

This mode is used for circuits which only need a single pole, but need the flexibility of clock control for the corner frequency. As with Mode 6, the output at Pin 1 is not used and is normally either near V_{DD} or V_{SS}.

Design Equations

$$f_{corner} = \frac{f_{clock}}{100} \quad \frac{R2}{R3}$$

This equation is used when Pin 12, 50/100/PD is tied to mid-supplies, usually 0 VDC.

$$f_{corner} = \frac{f_{clock}}{50} \quad \frac{R2}{R3}$$

When Pin 12, 50/100/PD is tied to V_{DD}, this formula is used to calculate the position of the corner of the low pass filter.

$$H_{lowpass\ (inverting)} = -\frac{R3}{R2}$$

The gain of the inverting low pass filter output is controlled by the ratio of the feedback resistor R3 to the resistor R2.

$$H_{lowpass\ (noninverting)} = +1\frac{V}{V}$$

The gain of the non-inverting low pass filter output is fixed at +1.

GENERAL APPLICATION CRITERIA

The following aspects of the use of any filter should be considered when the design is started:

1. Prevention of saturation of the first stage or any subsequent stages. If a design is composed of two stages, consideration to the output amplitude of the first stage must be given. The Q of the filter could cause clipping on the first stage, which would be filtered by the second stage back to a sinusoidal signal. This would cause an increase in noise and error in the phase response of the filter.

   Any DC offset of the signal can cause clipping or even rectification of the signal. The offset of the signal should be determined for the first stage and any other stages.

3. The order of the filters may be important to the design. Once again this would be due to the gain or Q of the filters. For example, a low pass filter may be desired before a band pass filter to reduce the chance that out–of–band signals will affect the band pass filter. Also, any clipping at the output of the band pass filter would be apparent. This would not be the case if the band pass filter was the first stage and the low pass filter was second.

4. The signal–to–noise ratio should be maximized. In most designs the limiting factor for the signal to noise ratio is not the filter itself, rather the layout of the board and decoupling of the supplies. Proper use of analog and digital grounds should be observed in any system using a filter. Proper grounds imply that no differential voltage will occur from the INV SWITCH when grounded and AGND. A separate analog V_{DD} and V_{SS} should be provided when possible.

   Also, shielding of the low amplitude signals from large digital signals should be considered.

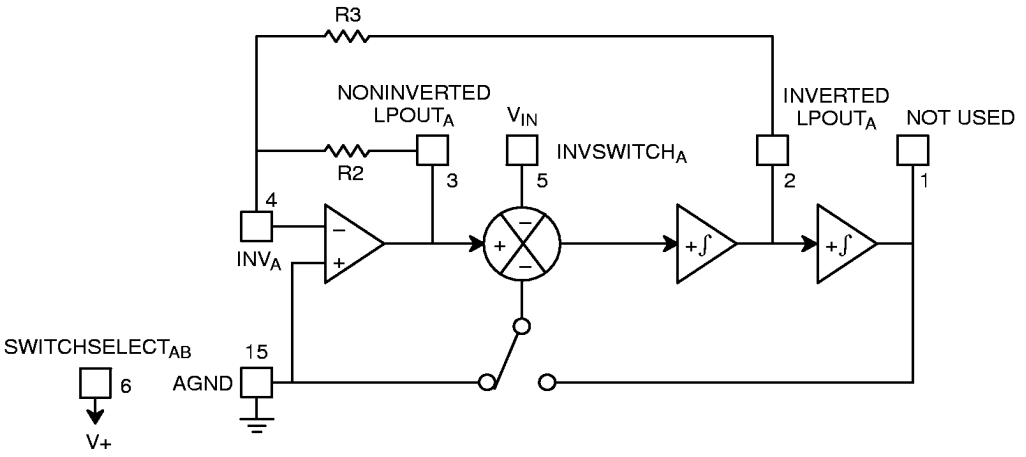


Figure 22. Mode 6B

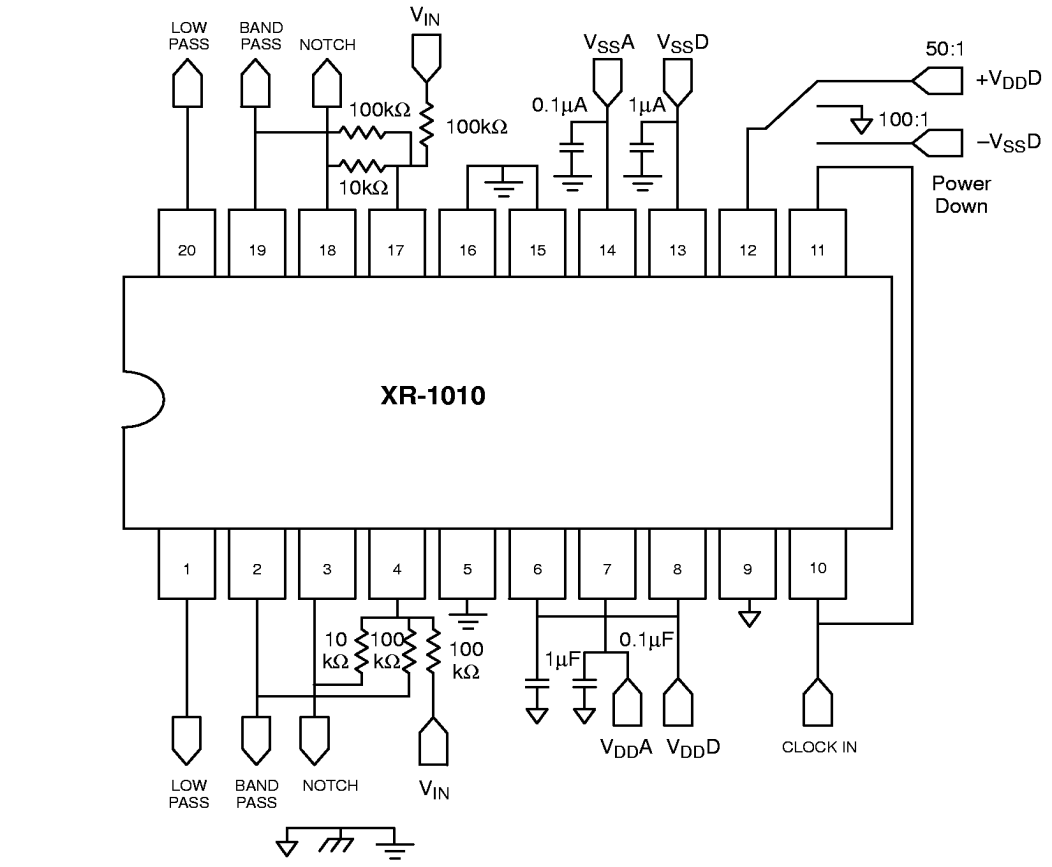
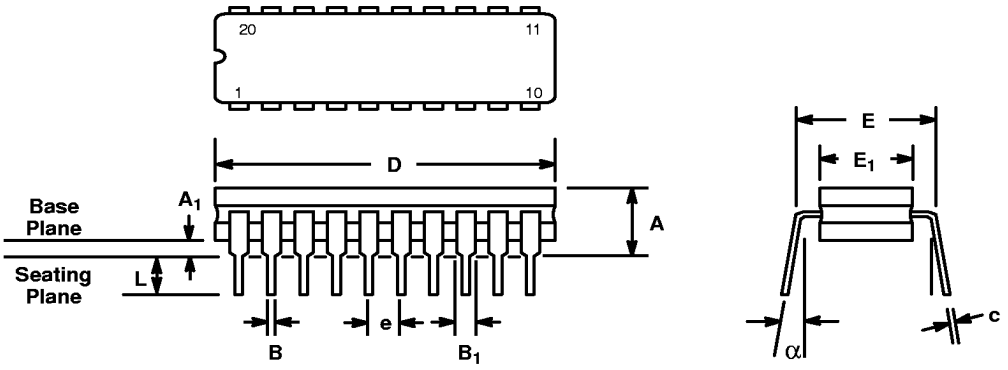


Figure 23. Split Supply Operation Mode 1

20 LEAD CERAMIC DUAL-IN-LINE (300 MIL CDIP)

Rev. 1.00

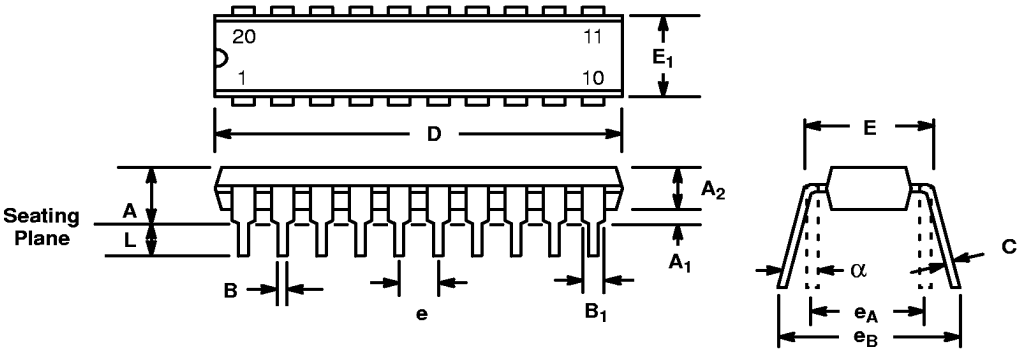


SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.100	0.200	2.54	5.08
A_1	0.015	0.070	0.38	1.78
B	0.014	0.026	0.36	0.66
B_1	0.045	0.065	1.14	1.65
c	0.008	0.018	0.20	0.46
D	0.960	1.060	24.38	26.92
E_1	0.250	0.310	6.35	7.87
E	0.300 BSC		7.62 BSC	
e	0.100 BSC		2.54 BSC	
L	0.125	0.200	3.18	5.08
α	0°	15°	0°	15°

Note: The control dimension is the inch column

20 LEAD PLASTIC DUAL-IN-LINE (300 MIL PDIP)

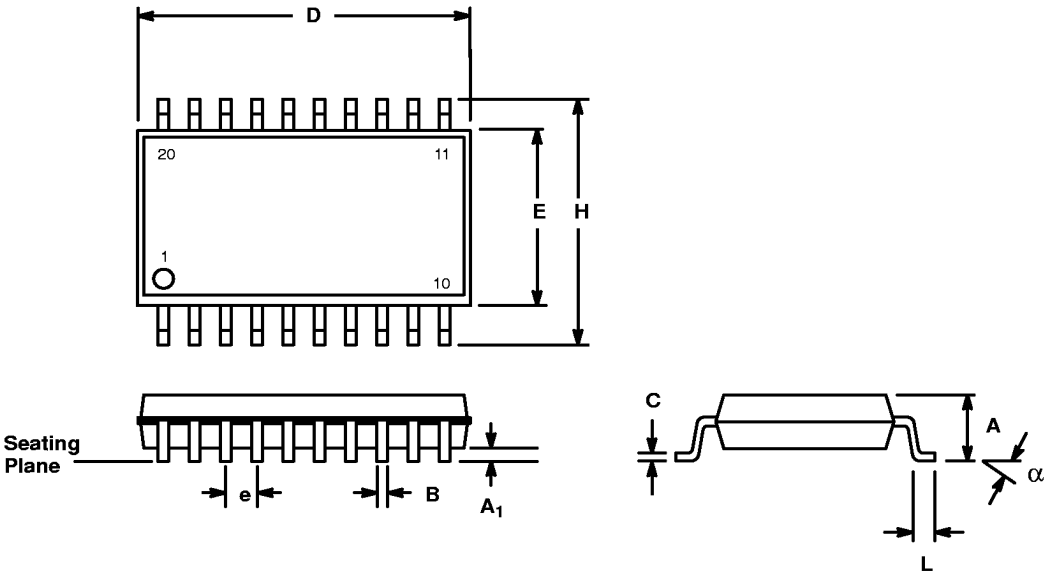
Rev. 1.00



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.145	0.210	3.68	5.33
A_1	0.015	0.070	0.38	1.78
A_2	0.115	0.195	2.92	4.95
B	0.014	0.024	0.36	0.56
B_1	0.030	0.070	0.76	1.78
C	0.008	0.014	0.20	0.38
D	0.925	1.060	23.50	26.92
E	0.300	0.325	7.62	8.26
E_1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
e_A	0.300 BSC		7.62 BSC	
e_B	0.310	0.430	7.87	10.92
L	0.115	0.160	2.92	4.06
α	0°	15°	0°	15°

20 LEAD SMALL OUTLINE (300 MIL JEDEC SOIC)

Rev. 1.00



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A_1	0.004	0.012	0.10	0.30
B	0.013	0.020	0.33	0.51
C	0.009	0.013	0.23	0.32
D	0.496	0.512	12.60	13.00
E	0.291	0.299	7.40	7.60
e	0.050 BSC		1.27 BSC	
H	0.394	0.419	10.00	10.65
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°

Note: The control dimension is the millimeter column