XC2000L Low-Voltage Logic Cell Array Family

Preliminary Product Specification

Features

- Part of the ZERO+ Family of 3.3 V FPGAs

- Low-power, low-supply-voltage FPGA family with two device types
  - JEDEC-compliant 3.3 V version of the XC2000 LCA Family
  - Logic densities from 1,000 to 1,500 gates
  - Up to 74 user-definable I/Os

- Advanced, low power 0.8 μ CMOS static-memory technology
  - Very low quiescent current consumption, ≤20 μA , 25 times less than XC2000
  - Operating power consumption 66% less than previous generation 5 V FPGAs; 56% less than XC2000

- Identical to the basic XC2000 in structure, pin out, design methodology, and software tools
  - 100% compatible with XC2000 bitstreams

- XC2000L-specific features
  - Guaranteed over the 3.0 to 3.6 V V_{CC} range
  - TTL-equivalent input and output levels
  - 4 mA output sink and source current
  - Advanced packaging using thin and very thin quad flat packs

Description

The XC2000L family of FPGAs is optimized for operation from a 3.3 V (nominal) supply. Aside from the electrical and timing parameters listed in this data sheet, the XC2000L family is in all respects identical with the XC2000 family.

The operating power consumption of Xilinx FPGAs is almost exclusively dynamic; it changes with the square of the supply voltage. For a given complexity and clock speed, the XC2000L consumes, therefore, only 44% of the power used by the equivalent XC2000 device. Consistent with its use in battery-powered equipment, the XC2000L family was designed for the lowest possible power-down and quiescent current consumption.

Device	Logic Capacity (gates)	CLBs	User I/O Max	Config. bits
XC2064L	800 - 1,000	64	58	12,038
XC2018L	1,200 - 1,500	100	74	17,878

LCA logic functions and interconnections are determined by data stored in internal static-memory cells. On-chip logic provides for automatic loading of configuration data at power-up. Program data can reside in an EEPROM, EPROM or ROM on the circuit board or on a floppy disk or hard disk. The program can be loaded in a number of modes to accommodate various system requirements.

Xilinx maintains test specifications for each product as controlled documents. To insure the use of the most recently released device performance parameters, please request a copy of the current test-specification revision.

Absolute Maximum Ratings

Symbol	Description		Units
V_{CC}	Supply voltage relative to GND	−0.5 to +7.0	V
V_{IN}	Input voltage with respect to GND	−0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output	−0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)	−65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in.)	+260	°C
T_J	Junction temperature plastic	+125	°C
	Junction temperature ceramic	+150	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Operating Conditions

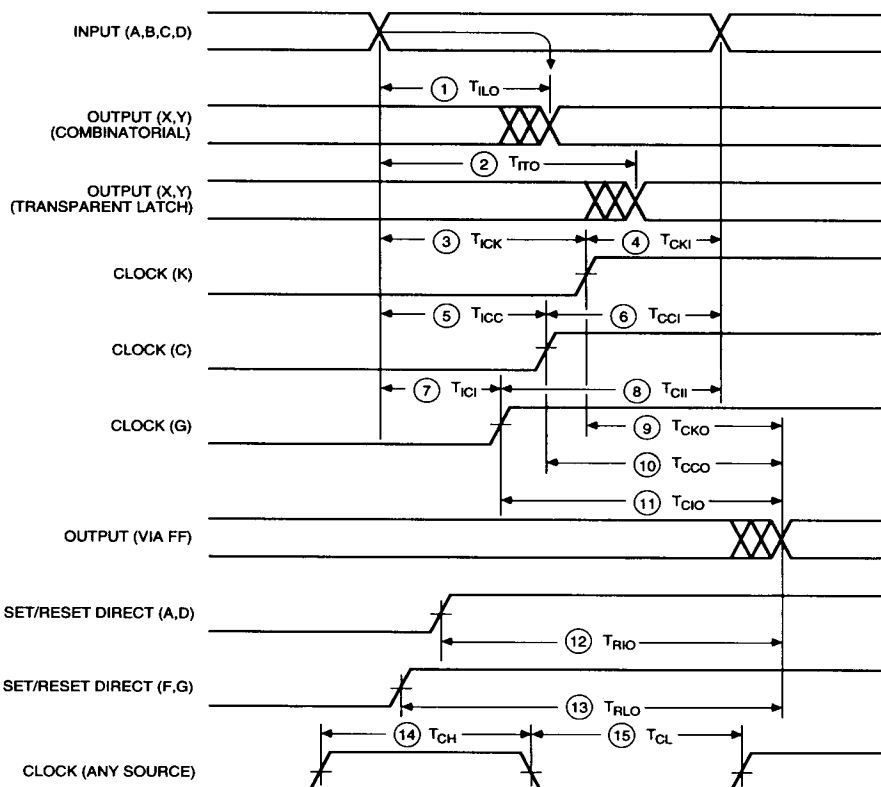| Symbol	Description	Min	Max	Units
V_{CC}	Supply voltage relative to GND (Commercial 0°C to +70°C)	3.0	3.6	V
V_{IH}	High-level input voltage	2.0	V_{CC}+0.3	V
V_{IL}	Low-level input voltage	0.3	0.8	V
T_{IN}	Input signal transition time		250	ns

Although the present (1993) devices operate over the full supply voltage range from 3.0 to 5.25 V, Xilinx reserves the right to restrict operation to the 3.0 to 3.6 V range later, when smaller device geometries might preclude operation at 5 V.

DC Characteristics Over Operating Conditions

Symbol	Description	Min	Max	Units
V_{OH}	High-level output voltage (@ $I_{OH} = -2.0$ mA V_{CC} min)	2.4		V
V_{OL}	Low-level output voltage (@ $I_{OL} = 4.0$ mA V_{CC} max)		0.4	V
V_{OH}	High-level output voltage (@ -100 µA V_{CC} min)	V_{CC} -0.2		V
V_{OL}	Low-level output voltage (@ 100 µA V_{CC} min)		0.2	V
V_{CCPD}	Power-down supply voltage ($\overline{PWRDWN}$ must be Low)	2.3		V
I_{CCO}	Quiescent operating power supply current*		20	µA
I_{CCPD}	Power-down supply current ($V_{CC(MAX)}$ @ T_{MAX})		10	µA
I_{IL}	Input Leakage Current, all I/O pins in parallel	-10	$+10$	µA
C_{IN}	Input capacitance (sample tested) All Pins except XTL1 and XTL2		10	pF
	XTL1 and XTL2		15	pF

* With no output current loads, no active input or Longline pull-up resistors, all package pins at V_{CC} or GND, and the LCA device configured with a MakeBits tie option. I_{CCO} is in addition to I_{CCPD}.

CLB Switching Characteristic Guidelines

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CLB Switching Characteristic Guidelines (Continued)

	Description	Symbol		Speed Grade								Units
Logic Input to Output	Combinatorial	1	T_{ILO}									ns
	Transparent latch	2	T_{ITO}									ns
	Additional for Q through F or G to out		T_{QLO}									ns
K Clock	To output	9	T_{CKO}									ns
	Logic-input setup	3	T_{ICK}									ns
	Logic-input hold	4	T_{CKI}									ns
C Clock	To output	10	T_{CCO}									ns
	Logic-input setup	5	T_{ICC}									ns
	Logic-input hold	6	T_{CCI}									ns
Logic Input to G Clock	To output	11	T_{CIO}									ns
	Logic-input setup	7	T_{ICI}									ns
	Logic-input hold	8	T_{CII}									ns
Set/Reset direct	Input A or D to output x, y	12	T_{RIO}									ns
	Through F or G to output	13	T_{RLO}									ns
	Reset pad to output x, y		T_{MRQ}									ns
	Separation of set/reset		T_{RS}									ns
	Set/Reset pulse-width		T_{RPW}									ns
Flip-flop Toggle rate	Q through F to flip-flop		F_{CLK}									MHz
Clock	Clock High	14	T_{CH}									ns
	Clock Low	15	T_{CL}									ns

Notes: 1. All switching characteristics apply to all valid combinations of process, temperature and supply with a nominal chip power dissipation of 250 mW.

IOB Switching Guidelines
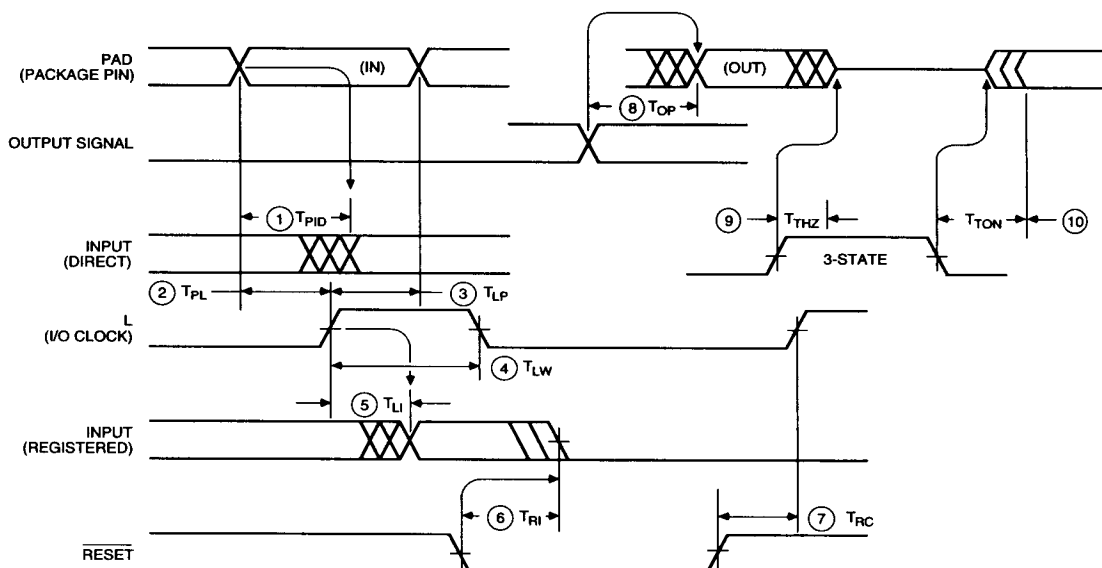
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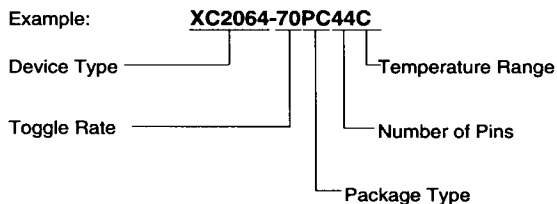| Speed Grade											Units
	Description		**Symbol**								
Pad (package pin)	To input (direct)	1	T_{PID}								ns
I/O Clock	To input (storage)	5	T_{LI}								ns
	To pad-input setup	2	T_{PL}								ns
	To pad-input hold	3	T_{LP}								ns
	Pulse width	4	T_{LW}								ns
	Frequency										MHz
Output	To pad (output enabled)	8	T_{OP}								ns
Three-state	To pad begin hi-Z	9	T_{THZ}								ns
	To pad end hi-Z	10	T_{TON}								ns
$\overline{RESET}$	To input (storage)	6	T_{RI}								ns
	To input clock	7	T_{RC}								ns

Note: Timing is measured at 0.5 Vcc levels with 50 pF output load.

For a detailed description of the device architecture, see pages 2-179 through 2-187.

For a detailed description of the configuration modes and their timing, see pages 2-192 through 2-198.

For package physical dimensions, see Section 4.

Ordering Information

Example: **XC2064-70PC44C**

Device Type ——————┘   └——Temperature Range

Toggle Rate ——————————┘   └—— Number of Pins

└—— Package Type

Component Availability

PINS		44	48	64	68		84		100	
TYPE		PLAST. PLCC	PLAST. DIP	PLAST. VQFP	PLAST. PLCC	CERAM. PGA	PLAST. PLCC	CERAM. PGA	PLAST. TQFP	PLAST. VQFP
CODE		PC44	PD48	VQ64	PC68	PG68	PC84	PG84	TQ100	VQ100
XC2064	-50		C		C I	C I M				
	-70	C I			C I	C I M				
	-100	C			C	C				
XC2018	-33							M B		
	-50				C I		C I	C I M B		
	-70	C I			C I		C I	C I M B		
	-100	C		C	C		C	C	C	
XC2064L				(C I)	C I					
XC2018L				C I			C I			C I

C = Commercial = 0° to +70° C   I = Industrial = -40° to +85° C
M = Mil Temp = -55° to +125° C   B = MIL-STD-883C Class B
Parentheses indicate future product plans