3 Electrical Characteristics

3.1 Absolute Maximum Ratings Over Operating Free-Air Temperature Range (unless otherwise noted)†

Supply voltage, V_{CC} (measured to GND) ..... 7 V
Input voltage range V_I (any digital terminal) ..... GND – 0.5 to V_{CC} + 0.5 V
Analog output short circuit duration to any power supply or common ..... unlimited
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature, T_{stg} ..... –65°C to 150°C
Junction temperature, T_J ..... 150°C
Case temperature for 10 seconds, T_C: FN package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

3.2 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Power supply voltage, V_{CC}	4.75	5	5.25	V
Reference voltage, V_{ref}	1.15	1.235	1.26	V
High-level digital input voltage, including XIN and XOUT, V_{IH}	2		VCC+0.5	V
Low-level digital input voltage, including XIN and XOUT, V_{IL}	GND–0.5		0.8	V
Crystal input frequency, f_I (200 ppm)		14.318		MHz
Crystal loading	parallel	parallel	parallel	
Crystal series resistance		35		Ω
Output load resistance, R_L		37.5		Ω
White level adjust resistor, R_{SET}		147		Ω
Ambient operating temperature, T_A	0		70	°C

NOTE 1: Other crystal frequencies can be used.

3.3 Electrical Characteristics Over Recommended Full Voltage and Temperature Ranges

3.3.1 DC Characteristics, Total Device (see Note 2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level digital output voltage, except OTCLKA and OTCLKB	$I_{OH} = -4$ mA	2.4			V
V_{OL}	Low-level digital output voltage, except OTCLKA and OTCLKB	$I_{OL} = 4$ mA			0.4	V
V_{OH}	High-level digital output voltage, OTCLKA and OTCLKB	$I_{OH} = -12$ mA	2.4			V
V_{OL}	Low-level digital output voltage, OTCLKA and OTCLKB	$I_{OL} = 12$ mA			0.4	V
I_{IH}	High-level digital input current	$V_I = 2.4$ V			1	µA
I_{IL}	Low-level digital input current	$V_I = 0.4$ V			−1	µA
I_{OZ}	Digital high-impedance-state output current				50	µA
C_i	Digital input capacitance	f = 1 MHz, $V_I = 2.4$ V		4		pF

NOTE 2: Test conditions generate RS-343A video signals unless otherwise specified. The recommended operation condition for generating test signals is $R_{SET} = 147\ \Omega$, $V_{ref} = 1.235$ V.

3.3.2 AC Characteristics, Supply Current, and Pipeline Delay (See Notes 3 and 4)

PARAMETER		TVP3409-170			TVP3409-135			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
I_{CC}	V_{CC} supply current		265	285		231	250	mA
$I_{CC(sleep)}$	Sleep current (PCLK = 35 MHz)		55			55		mA

NOTES: 3. The recommended operation condition for generating test signals is $R_{SET} = 147\ \Omega$, $V_{ref} = 1.235$ V. TTL level input values are 0 V to 3 V, with input rise/fall times ≤ 3 ns, measured from 10% to 90% points. Timing reference points are 50% for both inputs and outputs. Analog output load ≤ 10 pF, $\overline{\text{SENSE}}$, D(7–0) output load ≤ 50 pF.

4. Pipeline delay is fixed for each mode (see Table 2–18 for pipeline delay for each mode).

3.4 Operating Characteristics Over Recommended Full Voltage and Temperature Ranges

3.4.1 DC Characteristics, Total Device (see Note 2)

	PARAMETER	MIN	TYP	MAX	UNIT
	Resolution (each DAC)	8	8	8	bits
E_L	Integral linearity error (8-bit, each DAC)			±1	LSB
E_D	Differential linearity error (8-bit, each DAC)			±1	LSB
E_G	Gain error			±1%	
C_O	Digital output capacitance		7		pF
	Coding				binary
	Internal reference output voltage	1.15	1.235	1.26	V
	Sense voltage reference	270	340	410	mV
PSRR	Power supply rejection ratio			−6	dB

3.4.2 DC Characteristics, Analog Outputs (see Note 2)

PARAMETER			MIN	TYP	MAX	UNIT
Output current		Gray scale			20	mA
		White level relative to black	17.69	19.05	20.4	mA
		Black level relative to $\overline{\text{BLANK}}$ (with pedestal)	0.95	1.44	1.9	mA
		Black level relative to $\overline{\text{BLANK}}$ (without pedestal)	0	5	50	µA
		$\overline{\text{BLANK}}$ level	0	5	50	µA
		One LSB		69.9		µA
	DAC-to-DAC matching			2%	5%	
	Output compliance		−0.5		1.2	V
Z_O	Output impedance			50		kΩ
C_O	Output capacitance	f = 1 MHz, I_O = 0 mA		13		pF

NOTE 2: Test conditions generate RS-343A video signals unless otherwise specified. The recommended operation condition for generating test signals is R_{SET} = 147 Ω, V_{ref} = 1.235 V.

3.4.3 AC Characteristics, DAC Performance (see Notes 3 and 5)

PARAMETER	TVP3409-170			TVP3409-135			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	
DAC-to-DAC crosstalk		–20			–20		dB
Clock and data feedthrough (see Note 5)		–20			–20		dB
Glitch impulse		50			50		pV-s

NOTES: 3. The recommended operation condition for generating test signals is R_{SET} = 147 Ω, V_{ref} = 1.235 V. TTL level input values are 0 V to 3 V, with input rise/fall times ≤ 3 ns, measured from 10% to 90% points. Timing reference points are 50% for both inputs and outputs. Analog output load ≤ 10 pF, $\overline{\text{SENSE}}$, and D(7–0) output load ≤ 50 pF.

5. External voltage reference automatically disabled during power down. Test conditions are 25°C to 70°C, pixel and data ports at 0.4 V.

3.4.4 AC Characteristics, Clock Synthesizer (see Notes 6 and 7)

PARAMETER		TVP3409-170			TVP3409-135			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
t_1	Edge jitter, OTCLKA or OTCLKB (6 sigma)		300			300		ps

NOTES: 6. TTL level input values are 0 V to 3 V, with input rise/fall times ≤ 3 ns, measured from 10% to 90% points. Timing reference points are 50% for both inputs and outputs. Digital output load ≤ 15 pF. Crystal or reference frequency = 14.318 MHz, OTCLKA or OTCLKB loading ≤ 15 pF.

7. Output phase and duty cycle jitter excludes the reference clock or crystal oscillator jitter.

3.5 Timing Requirements

3.5.1 Total Device (see Note 3)

PARAMETER			TVP3409-170			TVP3409-135			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
f_{max1}	Internal 2X clock frequency (for reference only)				170			135	MHz
f_{max2}	PCLK frequency	2X clock disabled			110			110	MHz
f_{max2x}	PCLK frequency	2X clock enabled	0		85	0		67.5	MHz
t_{cyc}	PCLK cycle time		9.09			9.09			ns
	PCLK duty cycle		30%	50%	70%	30%	50%	70%	

3.5.2 Pixel and Control Timing (see Note 3)

PARAMETER		TVP3409-170		TVP3409-135		UNIT
		MIN	MAX	MIN	MAX	
t_{su1}	Setup time, P(15–0), $\overline{BLANK}$	2		2		ns
t_{h1}	Hold time, P(15–0), $\overline{BLANK}$	2		2		ns

NOTE 3. The recommended operation condition for generating test signals is R_{SET} = 147 Ω, V_{ref} = 1.235 V. TTL level input values are 0 V to 3 V, with input rise/fall times ≤ 3 ns, measured from 10% to 90% points. Timing reference points are 50% for both inputs and outputs. Analog output load ≤ 10 pF, $\overline{SENSE}$, and D(7–0) output load ≤ 50 pF.

3.5.3 Microprocessor Port (see Note 8)

PARAMETER		TVP3409-170		TVP3409-135		UNIT
		MIN	MAX	MIN	MAX	
t_{su2}	Setup time, RS(1,0)	10		10		ns
t_{h2}	Hold time, RS(1,0)	10		10		ns
t_{su4}	Setup time, Write D(7–0)	10		10		ns
t_{h4}	Hold time, Write D(7–0)	10		10		ns
t_{w1}	Pulse duration, $\overline{RD}$, $\overline{WR}$ low	50		50		ns
t_{w2}	Pulse duration, $\overline{RD}$, $\overline{WR}$ high	3		3		PCLK periods

NOTE 8. TTL level input values are 0 V to 3 V, with input rise/fall times ≤ 3 ns, measured from 10% to 90% points. Timing reference points are 50% for both inputs and outputs.

3.5.4 Clock Synthesizer (see Notes 6)

PARAMETER		TVP3409-170		TVP3409-135		UNIT
		MIN	MAX	MIN	MAX	
f_{max3}	Maximum synthesizer frequency for OTCLKA or OTCLKB (external)		85		85	MHz
	Input duty cycle, Fref, XIN, and XOUT	45%	55%	45%	55%	
	Duty cycle, OTCLKA or OTCLKB	45%	55%	45%	55%	
t_{w3}	Pulse duration, high or low, $\overline{\text{STROBE}}$	20		20		ns
t_{su5}	Setup time, FS(1,0) to $\overline{\text{STROBE}}$	2		2		ns
t_{h5}	Hold time, FS(1,0) to $\overline{\text{STROBE}}$		4		4	ns

NOTE 6. TTL level input values are 0 V to 3 V, with input rise/fall times ≤ 3 ns, measured from 10% to 90% points. Timing reference points are 50% for both inputs and outputs. Digital output load ≤ 15 pF. Crystal or reference frequency = 14.318 MHz, OTCLKA or OTCLKB loading ≤ 15 pF.

3.6 Switching Characteristics

3.6.1 DAC Performance (see Note 3)

PARAMETER		TVP3409-170			TVP3409-135			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
t_{d1}	Delay time, analog output (see Note 11)		9			9		ns
t_{r1}	Rise time, analog output (see Note 9)		3			3		ns
t_s	Settling time, analog output (see Note 10)		6			6		ns
	Delay SENSE output		1			1		µs
	Analog output skew			2			2	ns

NOTES: 3. The recommended operation condition for generating test signals is R_{SET} = 147 Ω, V_{ref} = 1.235 V. TTL level input values are 0 V to 3 V, with input rise/fall times ≤ 3 ns, measured from 10% to 90% points. Timing reference points are 50% for both inputs and outputs. Analog output load ≤ 10 pF, $\overline{\text{SENSE}}$, and D(7–0) output load ≤ 50 pF.

9. Measured between 10% to 90% of the full-scale transition.
10. Measured from the 50% point of the full-scale transition to the point at which the output has settled within ±1 LSB (settling time does not include clock and data feed through).
11. Measured from 90% point of PCLK rising edge to 50% point of full-scale transition.

3.6.2 Microprocessor Port (see Note 8)

PARAMETER		TVP3409-170		TVP3409-135		UNIT
		MIN	MAX	MIN	MAX	
t_{d2}	Delay time, $\overline{\text{RD}}$ asserted to D(7–0) driven	5		5		ns
t_{en}	Enable time, $\overline{\text{RD}}$ asserted to D(7–0) valid		40		40	ns
t_{dis}	Disable time, $\overline{\text{RD}}$ negated to D(7–0) 3-stated		20		20	ns
t_{v1}	Valid time, D(7–0) valid after $\overline{\text{RD}}$ high	5		5		ns

NOTE 8. TTL level input values are 0 V to 3 V, with input rise/fall times ≤ 3 ns, measured from 10% to 90% points. Timing reference points are 50% for both inputs and outputs.

3.6.3 Clock Synthesizer (see Note 6)

PARAMETER		TVP3409-170			TVP3409-135			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
t_{d3}	Delay time, frequency select to OTCLKA or OTCLKB unstable (see Note 12)			0			0	ns
t_{d4}	Delay time, frequency select to OTCLKA or OTCLKB stable (see Note 12)		1	10		1	10	ms
	Delay time, power up to OTCLKA or OTCLKB stable			10			10	ms
t_{r2}, t_{f2}	Rise or fall time, OTCLKA or OTCLKB (see Note 13)			3			3	ns

NOTES: 6. TTL level input values are 0 V to 3 V, with input rise/fall times ≤ 3 ns, measured from 10% to 90% points. Timing reference points are 50% for both inputs and outputs. Digital output load ≤ 15 pF. Crystal or reference frequency = 14.318 MHz, OTCLKA or OTCLKB loading ≤ 15 pF.

12. Frequency select can refer to the FS(1,0) terminals or control register bits CC(5,4) or CC(1,0).

13. Rise and fall time measured from 10% to 90% points using 0 V and 3 V levels.

3.7 Timing Diagrams

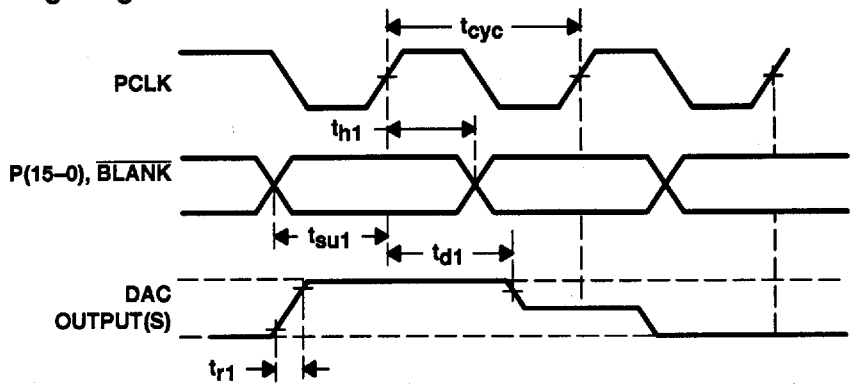

Figure 3–1. Pixel Input and Video Output Timing

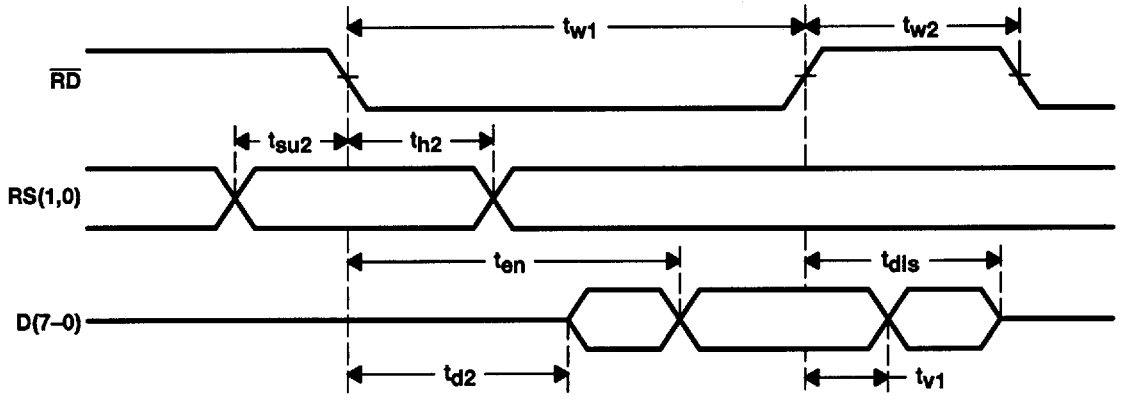

Figure 3–2. Basic Read-Cycle Timing

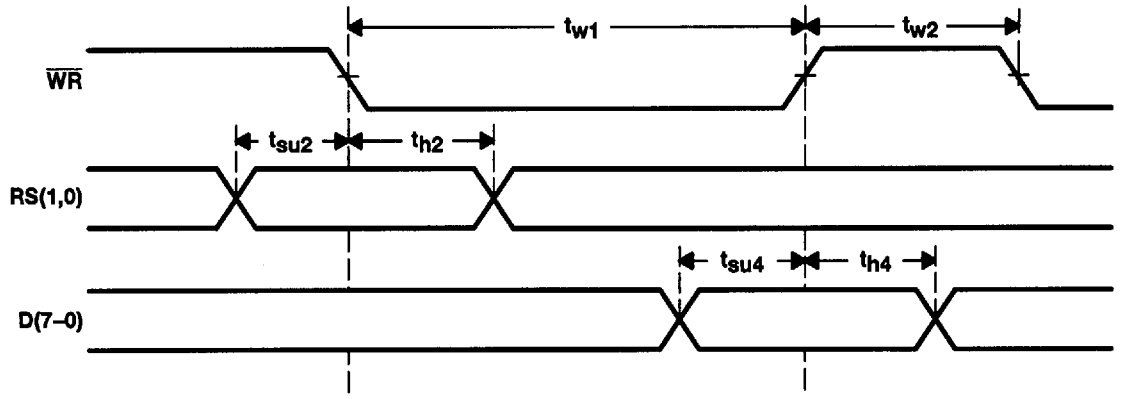

Figure 3–3. Basic Write-Cycle Timing

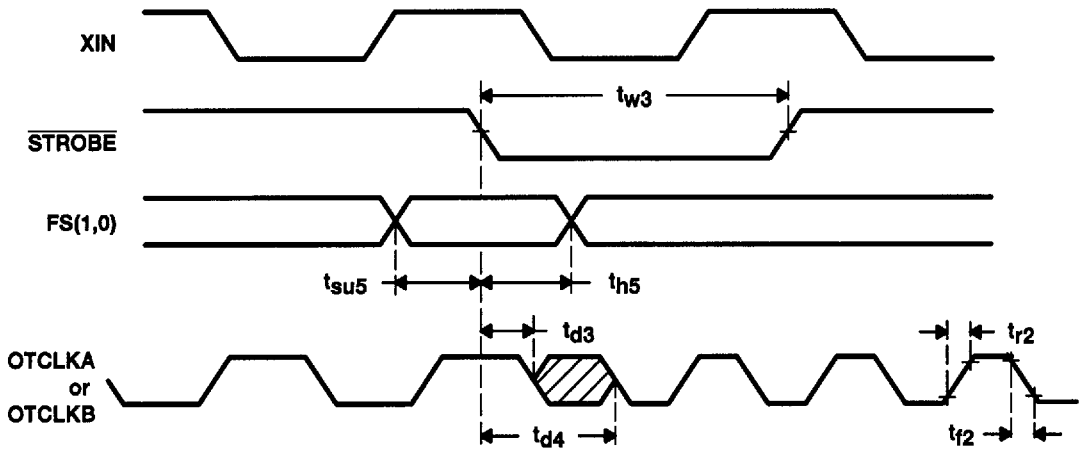

Figure 3–4. Clock Synthesizer (OTCLKA or OTCLKB) Timing

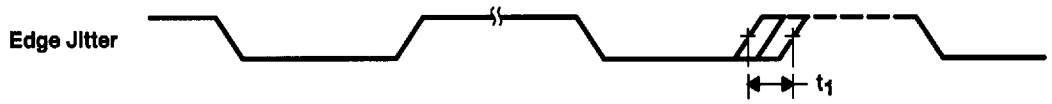

Figure 3–5. Clock Synthesizer Waveform Specifications (OTCLKA or OTCLKB)