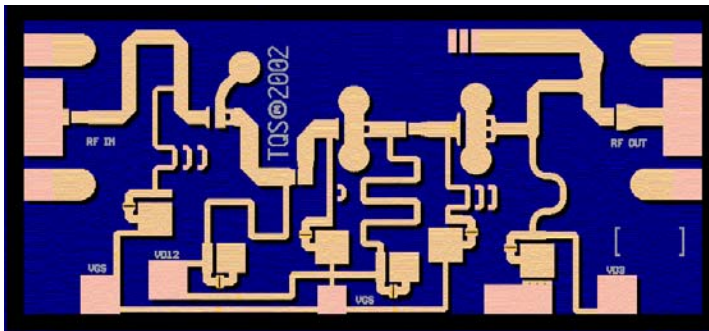


**Ka Band Low Noise Amplifier**

**TGA4507-EPU**



**Key Features**

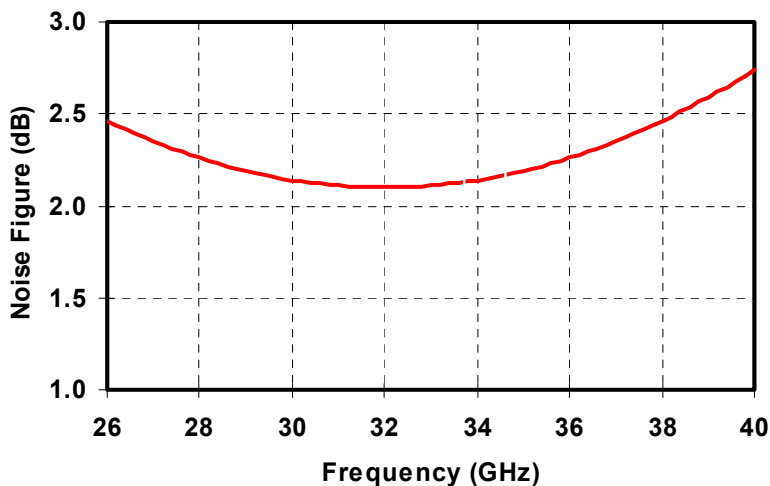
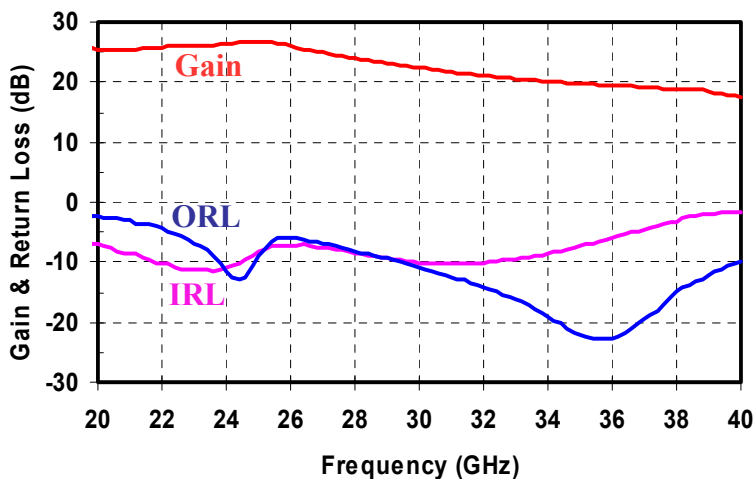
- Typical Frequency Range: 28 - 36 GHz
- 2.3 dB Nominal Noise Figure
- 22 dB Nominal Gain
- 12 dBm Nominal P1dB
- Bias 3.0 V, 60 mA
- 0.15 um 3MI pHEMT Technology
- Chip Dimensions 1.86 x 0.85 x 0.1 mm (0.073 x 0.033 x 0.004 in)

**Primary Applications**

- Point-to-Point Radio
- Point-to-MultiPoint Radio
- Ka Band VSAT

**Preliminary Measured Data**

Bias Conditions: Vd = 3.0 V, Id = 60 mA



Note: Devices designated as EPU are typically early in their characterization process prior to finalizing all electrical and process specifications. Specifications are subject to change without notice

**TABLE I**  
**MAXIMUM RATINGS <sup>1/</sup>**

SYMBOL	PARAMETER	VALUE	NOTES
V <sub>d</sub>	Drain Voltage	5 V	<u>2/</u>
V <sub>g</sub>	Gate Voltage Range	-1 TO +0.5 V	
I <sub>d</sub>	Drain Current	280 mA	<u>2/ 3/</u>
I <sub>g</sub>	Gate Current	6 mA	<u>3/</u>
P <sub>IN</sub>	Input Continuous Wave Power	TBD	
P <sub>D</sub>	Power Dissipation	TBD	<u>2/ 4/</u>
T <sub>CH</sub>	Operating Channel Temperature	150 °C	<u>5/ 6/</u>
T <sub>M</sub>	Mounting Temperature (30 Seconds)	320 °C	
T <sub>STG</sub>	Storage Temperature	-65 to 150 °C	

- 1/ These ratings represent the maximum operable values for this device.
- 2/ Combinations of supply voltage, supply current, input power, and output power shall not exceed P<sub>D</sub>.
- 3/ Total current for the entire MMIC.
- 4/ When operated at this bias condition with a base plate temperature of TBD, the median life is reduced from TBD to TBD hrs.
- 5/ Junction operating temperature will directly affect the device median time to failure (MTTF). For maximum life, it is recommended that junction temperatures be maintained at the lowest possible levels.
- 6/ These ratings apply to each individual FET.

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**TABLE II**  
**DC PROBE TESTS**  
(Ta = 25 °C, Nominal)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
V <sub>BVGD3</sub>	Breakdown Voltage Gate-Source			-5	V
V <sub>P1,2,3</sub>	Pinch-off Voltage		-0.4		V

Q1 is 100 um FET, Q2 is 200 um FET, Q3 is 300 um FET.

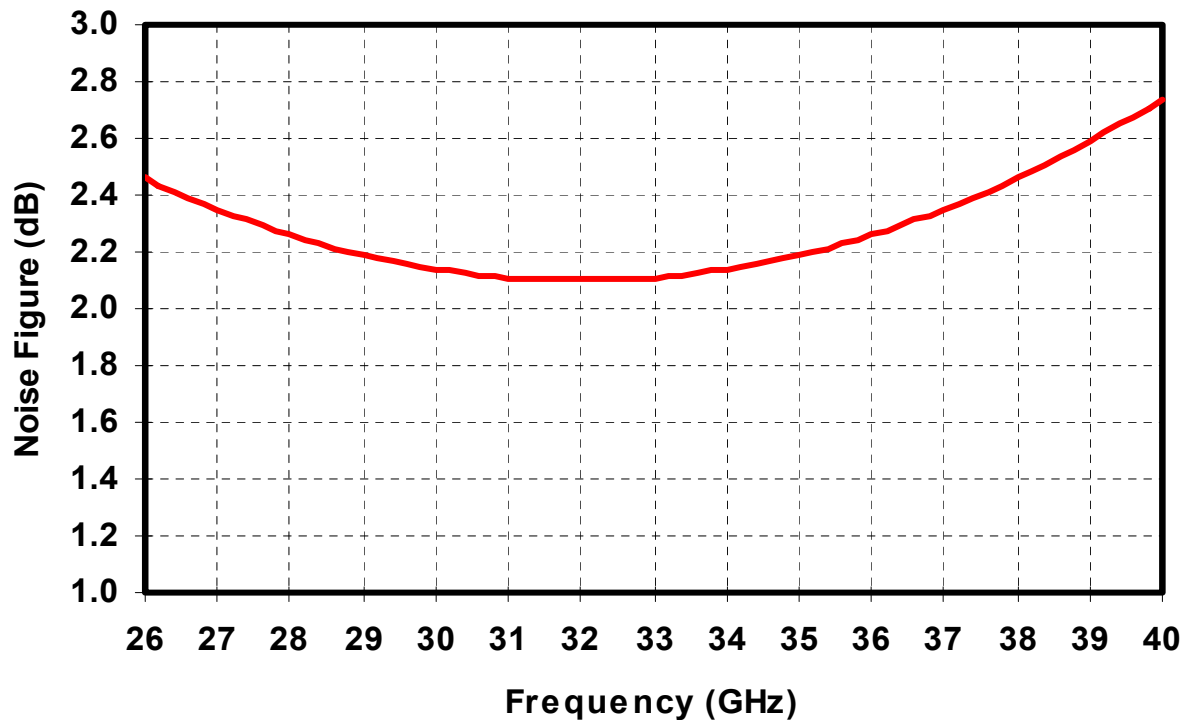
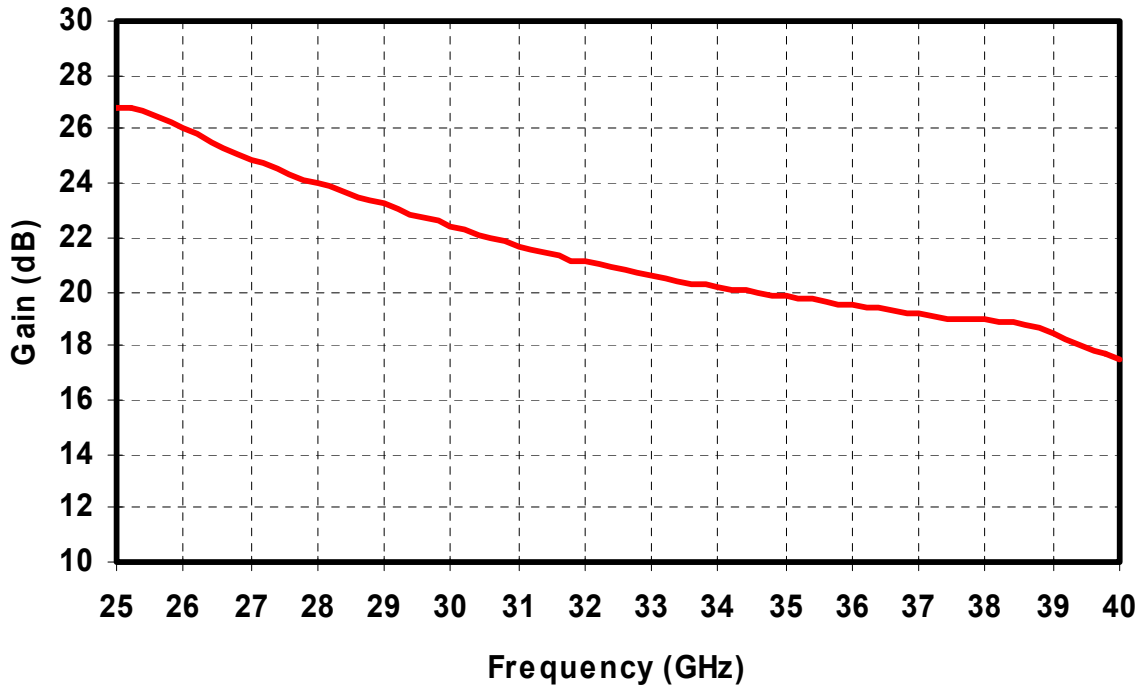
**TABLE III**  
**ELECTRICAL CHARACTERISTICS**  
(Ta = 25 °C Nominal)

PARAMETER	TYPICAL	UNITS
Drain Voltage, Vd	3.0	V
Drain Current, Id	60	mA
Gate Voltage, Vg	-0.5 to 0	V
Small Signal Gain, S21	22	dB
Input Return Loss, S11	8	dB
Output Return Loss, S22	8	dB
Noise Figure, NF	2.3	dB
Output Power @ 1 dB Compression Gain, P1dB	12	dBm

*Note: Devices designated as EPU are typically early in their characterization process prior to finalizing all electrical and process specifications. Specifications are subject to change without notice*

**Preliminary Measured Data**

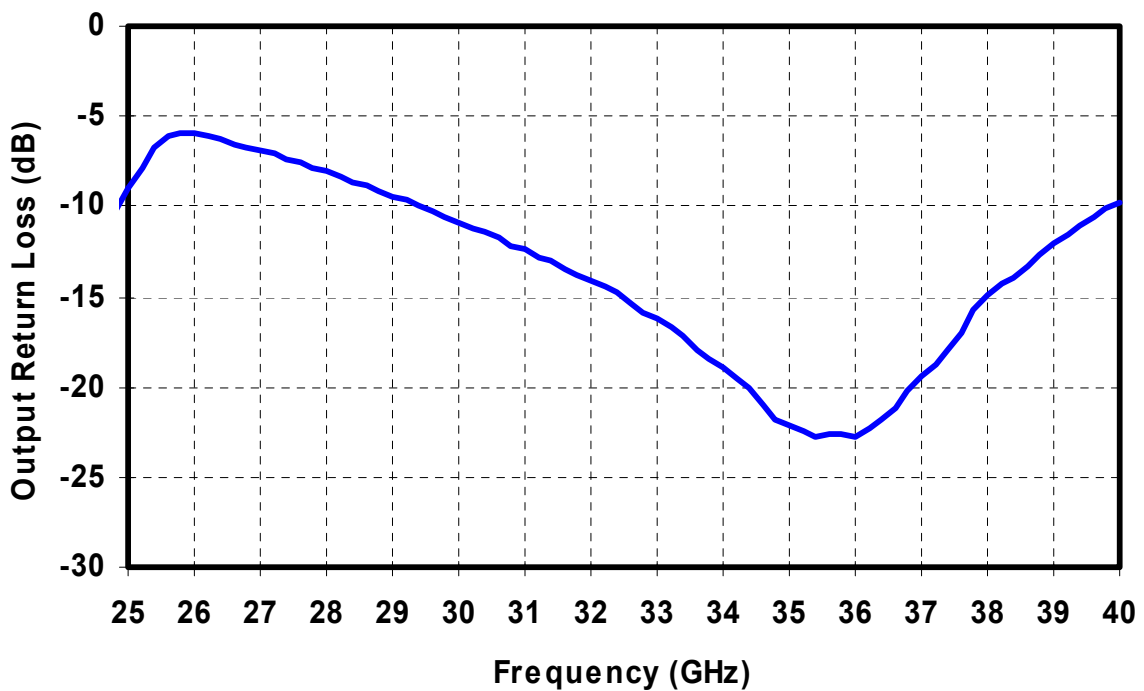
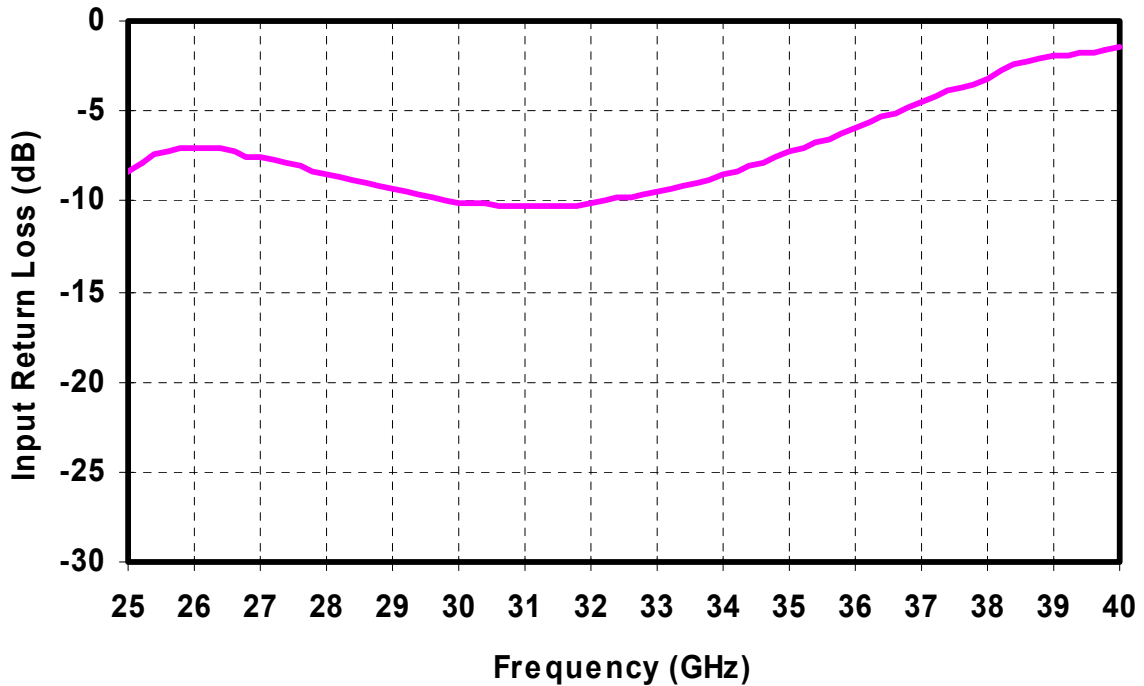
Bias Conditions:  $V_d = 3.0\text{ V}$ ,  $I_d = 60\text{ mA}$



Note: Devices designated as EPU are typically early in their characterization process prior to finalizing all electrical and process specifications. Specifications are subject to change without notice

### Preliminary Measured Data

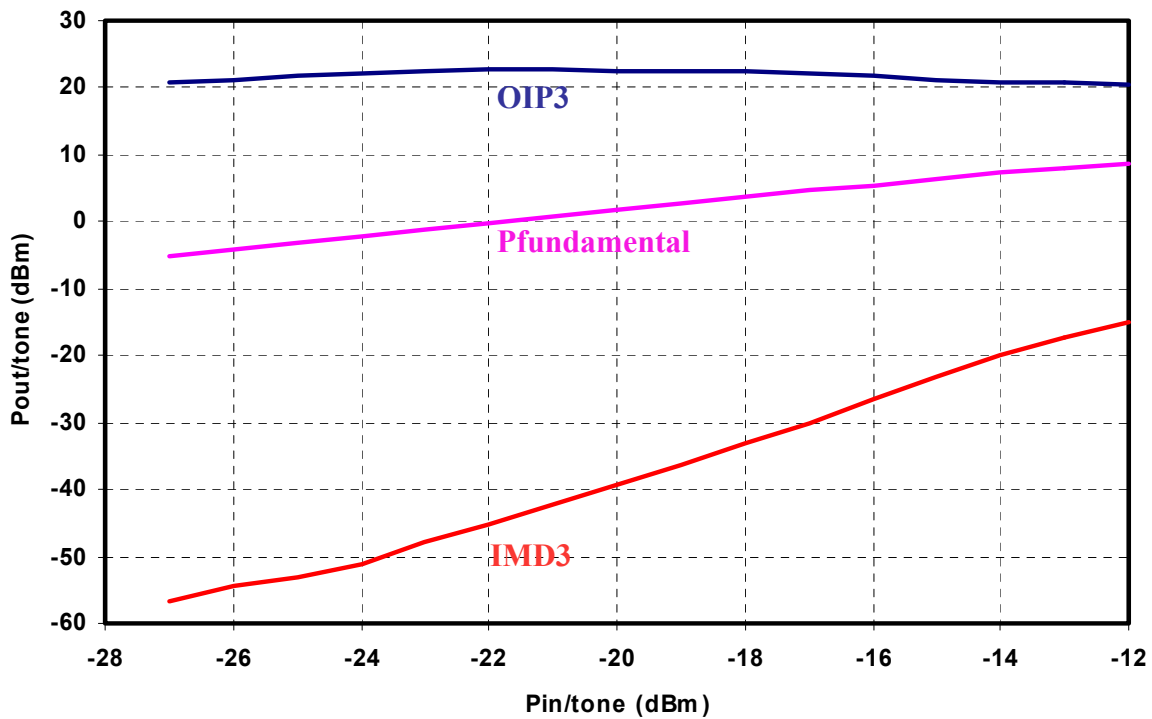
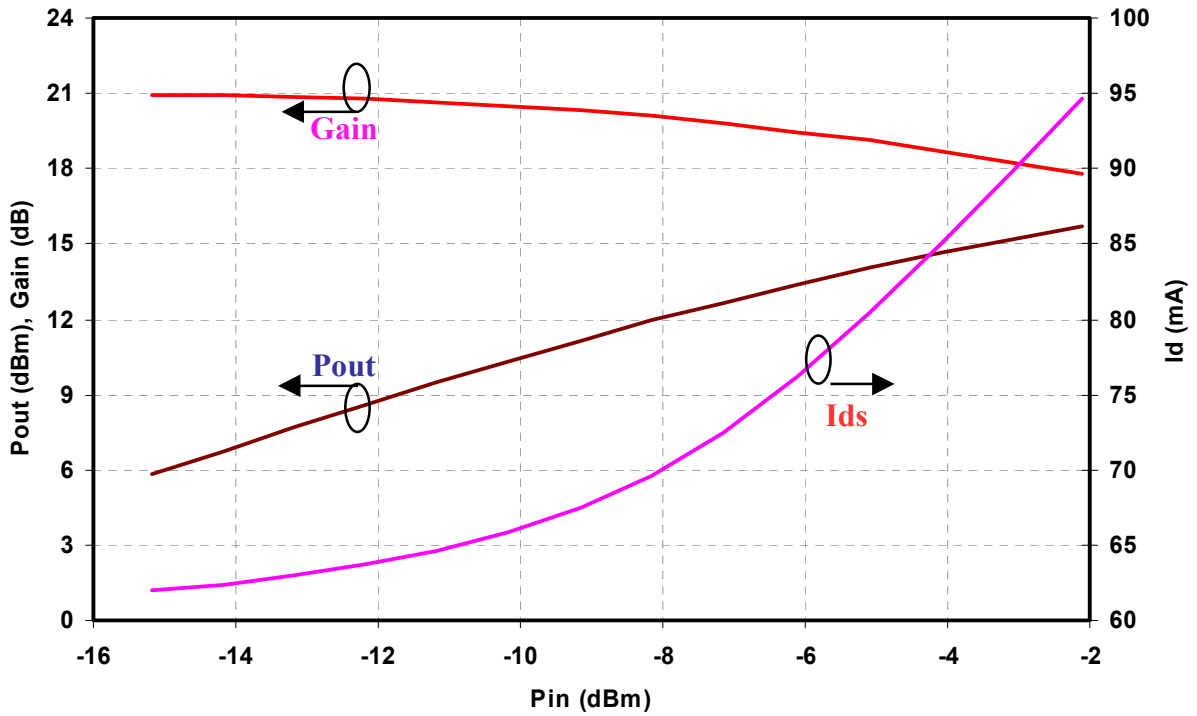
Bias Conditions:  $V_d = 3.0\text{ V}$ ,  $I_d = 60\text{ mA}$



Note: Devices designated as EPU are typically early in their characterization process prior to finalizing all electrical and process specifications. Specifications are subject to change without notice

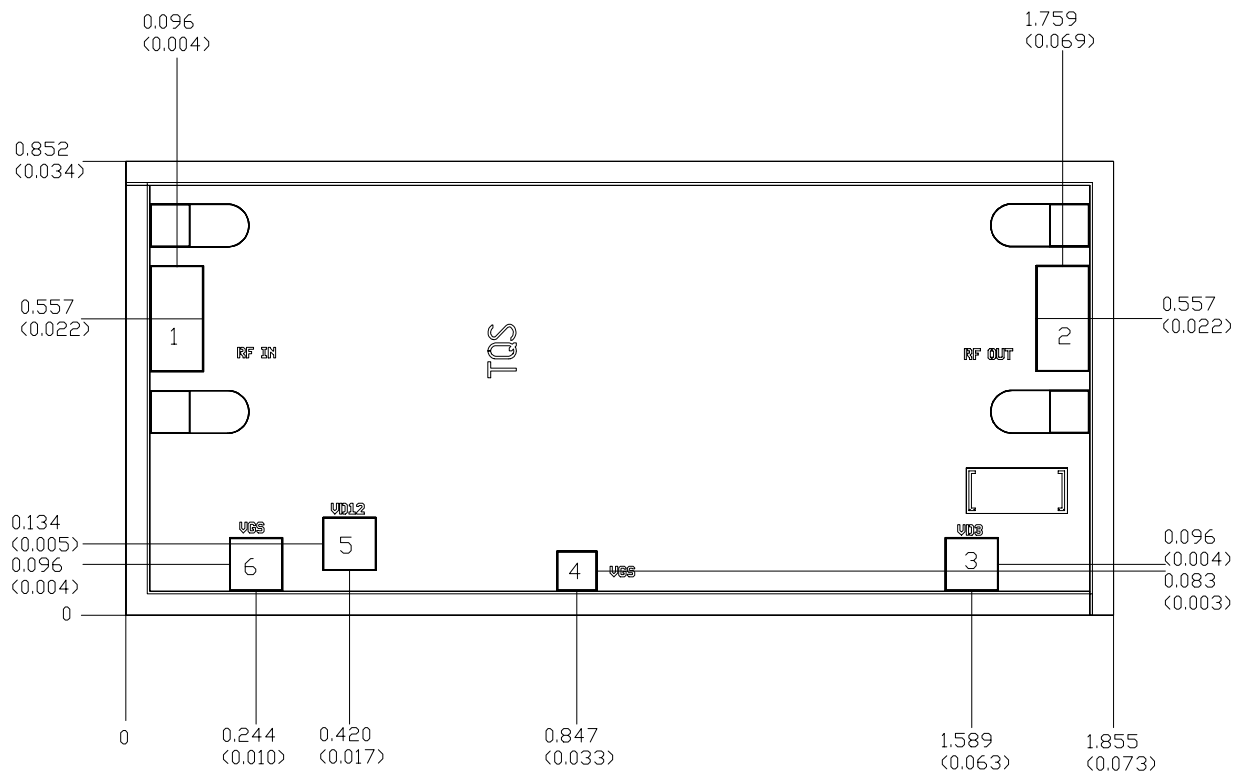
**Preliminary Measured Data**

Bias Conditions:  $V_d = 3.0\text{ V}$ ,  $I_d = 60\text{ mA}$ , Freq @ 30 GHz



Note: Devices designated as EPU are typically early in their characterization process prior to finalizing all electrical and process specifications. Specifications are subject to change without notice

**Mechanical Drawing**



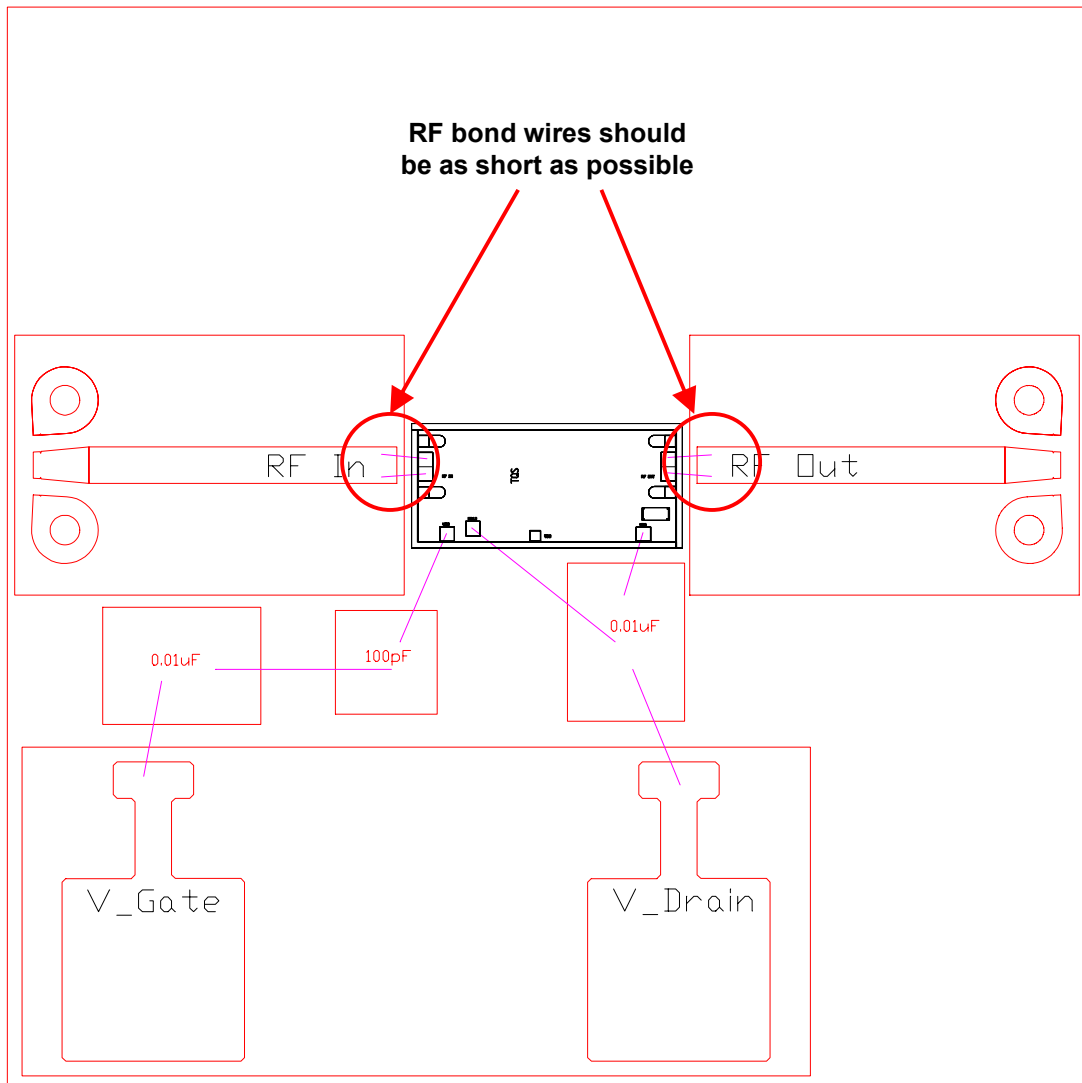
Units: millimeters (inches)  
Thickness: 0.100 (0.004)  
Chip edge to bond pad dimensions are shown to center of bond pad  
Chip size tolerance: +/- 0.051 (0.002)  
GND is back side of MMIC.

Bond pad #1 (RF In)	0.100 x 0.200	(0.004 x 0.008)
Bond pad #2 (RF Out)	0.100 x 0.200	(0.004 x 0.008)
Bond pad #3 (Vd3)	0.100 x 0.100	(0.004 x 0.004)
Bond pad #4 (Vg)	0.075 x 0.075	(0.003 x 0.003)
Bond pad #5 (Vd1,2)	0.100 x 0.100	(0.004 x 0.004)
Bond pad #6 (Vg)	0.100 x 0.100	(0.004 x 0.004)

**GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.**

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### Chip Assembly Diagram



**GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.**

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## **Assembly Process Notes**

Reflow process assembly notes:

- Use AuSn (80/20) solder with limited exposure to temperatures at or above 300°C (30 seconds max).
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- No fluxes should be utilized.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.
- Organic attachment can be used in low-power applications.
- Curing should be done in a convection oven; proper exhaust is a safety concern.
- Microwave or radiant curing should not be used because of differential heating.
- Coefficient of thermal expansion matching is critical.

Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonics are critical parameters.
- Aluminum wire should not be used.
- Maximum stage temperature is 200°C.

***GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.***

*Note: Devices designated as EPU are typically early in their characterization process prior to finalizing all electrical and process specifications. Specifications are subject to change without notice*