128K x 32 FLASH Memory

PUMA 2F4006-70/90/12

Elm Road, West Chirton, NORTH SHIELDS, Tyne & Wear
NE29 8SE, England Tel. +44 (0)191 2930500 Fax. +44 (0) 191 2590997

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General Description

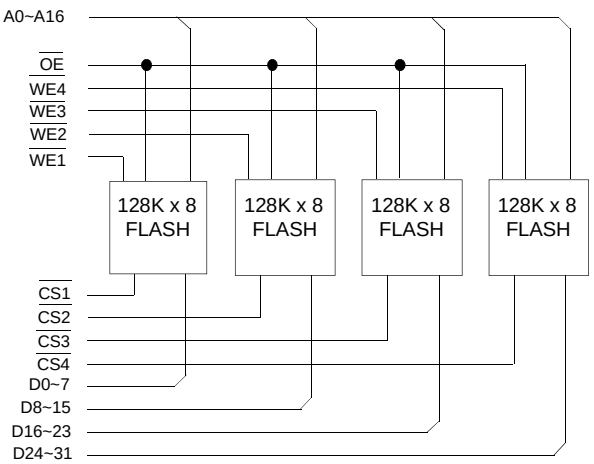
The PUMA 2F4006 is a 4,194,304 bit CMOS 5.0V only FLASH memory in a 66 pin ceramic PGA package, which is configurable as 8, 16, 32 bit wide output using four chip selects.Flash memory combines the functionality of EEPROM with on chip electrical Write/Erase logic, thus simplifying the external control circuitry. The PUMA 2F4006 incorporates Automatic Programming and Erase functions, which allow up to 10,000 Write/Erase cycles (min).

In addition, a Sector Erase function is available which can erase one 16K block of data randomly and more than one block simultaneously. The PUMA 2F4006 also features hardware sector protection, which enables both program and erase operations in any of the 32 sectors on the module.

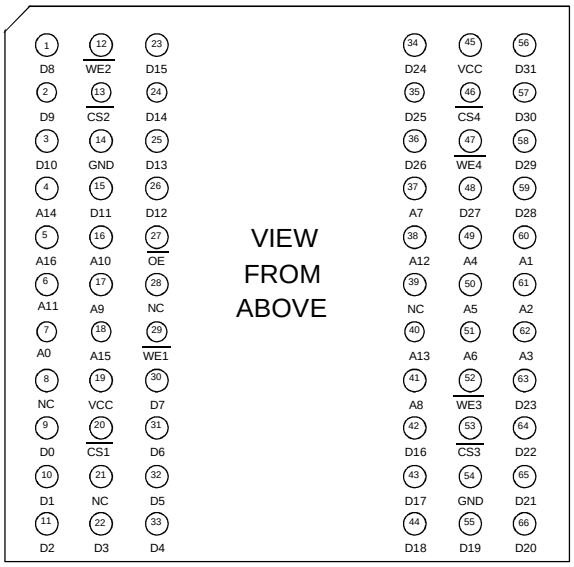
Features

- Very Fast Access Times of 70ns/90ns/120ns.
- Operating Power (Read) 660 mW (Max)
  (Program/Erase) 1100 mW (Max)
  Standby Power 2.2 mW (Max)
  Output Configurable as 32 / 16 / 8 bit wide.
- Automatic Write/Erase by Embedded Algorithm - end of Write/Erase indicated by DATA Polling and Toggle Bit.
- Flexible Sector Erase Architecture - 16K byte sector size, with hardware protection of any number of sectors.
- Single Byte Program of 14µs (typical), Sector Pro gram time of 0.3 sec. (typical).
- Module FLASH Erase of 3 seconds (typical).
- Erase/Write Cycle Endurance 10,000 (minimum)
- Can be screened in accordance with MIL-STD-883.

Block Diagram



Pin Definition



Pin Functions

A0~A16	Address Inputs	**D0~D31**	Data Input/Output
$\overline{CS1~4}$	Chip Select	**$\overline{OE}$**	Output Enable
$\overline{WE1~4}$	Write Enable	**V_{cc}**	Power (+5V)
GND	Ground		

DC OPERATING CONDITIONS

Absolute Maximum Ratings (1)

		unit
Voltage on any pin w.r.t. Gnd(2) (except A9)	-2.0 to +7	V
Supply Voltage(2)	-2.0 to +7	V
Voltage on A_9 w.r.t. Gnd	-2.0 to +14	V
Storage Temperature	-65 to +150	°C

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operationof the device at those or any other conditions above those indicated in the operational sections of this specification is not implied.

(2) Minimum DC voltage on any input or I/O pin is -0.5V. Maximum DC voltage on output and I/O pins is Vcc+0.5V. During transitions voltage may overshoot by +/-2V for up to 20ns

Recommended Operating Conditions

Parameter		*Symbol*	*min*	*typ*	*max*	*unit*	
DC Logic Supply Voltage		V_{CC}	4.5	5.0	5.5	V	
Input High Voltage	TTL	V_{IH}	2.0	-	V_{CC}+0.5	V	
	CMOS	V_{IHC}	0.7V_{CC}	-	V_{CC}+0.5	V	
Input Low Voltage	TTL	V_{IL}	-0.5	-	0.8	V	
	CMOS	V_{ILC}	-0.5	-	0.8	V	
Operating Temperature		T_A	0	-	70	°C	
		T_{AI}	-40	-	85	°C	(-**I** suffix)
		T_{AM}	-55	-	125	°C	(-**M**, **MB** suffix)

DC Electrical Characteristics (T_A= -55°C to +125°C,V_{CC}=5V±10%)

Parameter		*Symbol*	*Test Condition*	*min*	*typ*	*max*	*Unit*
Input Leakage Current		I_{LI}	V_{IN}=0 to V_{CC}, V_{CC} = V_{CC} max.	-	-	±4	µA
Output Leakage Current		I_{LO}	V_{OUT}=0 to V_{CC} ,V_{CC} = V_{CC} max.	-	-	±4	µA
Standby Supply Current	TTL	I_{SB1}	$\overline{CS1\sim4}$=V_{IH} ,V_{CC} = V_{CC} max.	-	-	4	mA
	CMOS	I_{SB2}	CS1~4=V_{CC}+0.5 , V_{CC} = V_{CC} max.	-	-	400	µA
Operating Current	Read	I_{CC1}	$\overline{CS1\sim4}$ = V_{IL}, $\overline{OE}$ = V_{IH}	-		120	mA
	Program/Erase	I_{CC2}	$\overline{CS1\sim4}$ = V_{IL}, $\overline{OE}$ = V_{IH}	-		200	mA
Output LowVoltage		V_{OL}	I_{OL}=12mA , V_{CC} = V_{CC} min.	-	-	0.45	V
Output HighVoltage		V_{OH}	I_{OH}=-2.5mA , V_{CC} = V_{CC} min.	2.4	-	-	V
Low Vcc lock out voltage		V_{LKO}		3.2	-	-	V
A9 voltage for autoselect		V_{ID}	V_{CC} =5.0V	11.5	-	12.5	V

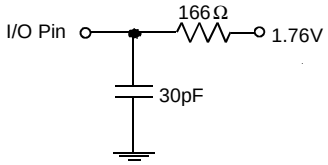
Capacitance (T_A=25°C,f=1MHz)

Parameter	*Symbol*	*Test Condition*	*typ*	*max*	*Unit*
Input Capacitance:	C_{IN}	V_{IN}=0V	34	40	pF
Output Capacitance:	C_{OUT}	V_{OUT}=0V	44	58	pF

Note: Capacitance calculated not measured.

AC Test Conditions

* Input pulse levels : 0.0V to 3.0V
* Input rise and fall times : 5 ns
* Input and output timing reference levels : 1.5V
* V_{CC} = 5V +/- 10%
* Module tested in 32 bit mode



Operating Modes

The following modes are used to control the PUMA 2F4006

OPERATION	$\overline{CS1\sim4}$	$\overline{OE}$	$\overline{WE1\sim4}$	A_0	A_1	A_9	I /O
Auto-Select Manufacturer Code	L	L	H	L	L	VID	Code
Auto Select Device Code	L	L	H	H	L	VID	Code
Read	L	L	H	A0	A1	A9	Dout
Standby	H	X	X	X	X	X	High Z
Output Disable	L	H	H	X	X	X	High Z
Write	L	H	L	A0	A1	A9	Din
Enable Sector Protect	L	VID	L	X	X	VID	X
Verify Sector Protect	L	L	H	L	H	VID	Code

$\overline{CS1\sim4}$ and $\overline{WE1\sim4}$ should be controlled by the user to configure the device for 8,16,or 32 bit operation.

AC OPERATING CONDITIONS

Read

Parameter	Symbol	-70 min	-70 max	-90 min	-90 max	-12 min	-12 max	unit
Read Cycle Time	t_{RC}	70	-	90	-	120	-	ns
Address to output delay	t_{AC}	-	70	-	90	-	120	ns
Chip Select to output	t_{CE}	-	70	-	90	-	120	ns
Output Enable to output	t_{OE}	-	30	-	35	-	50	ns
Chip Select to O/P High Z	t_{DF}	-	20	-	20	-	30	ns
Output Enable to output High Z	t_{DF}	-	20	-	20	-	30	ns
Output hold time (From address, $\overline{CS1}$~4 or $\overline{OE}$ whichever occurs first)	t_{OH}	0	-	0	-	0	-	ns

Write/ Erase/ Program

Parameter	Symbol	-70 min	-70 max	-90 min	-90 max	-12 min	-12 max	unit
Write Cycle time	t_{WC}	70	-	90	-	120	-	ns
Address Setup time	t_{AS}	0	-	0	-	0	-	ns
Address Hold time	t_{AH}	45	-	45	-	50	-	ns
Data Setup Time	t_{DS}	30	-	40	-	50	-	ns
Data hold Time	t_{DH}	0	-	0	-	0	-	ns
Output Enable Setup Time	t_{OES}	0	-	0	-	0	-	ns
Output Enable Hold Time	t_{OEH}	0	-	0	-	0	-	ns
Read Recover before Write	t_{GHWL}	0	-	0	-	0	-	ns
$\overline{CS1}$~4 setup time	t_{CS}	0	-	0	-	0	-	ns
$\overline{CS1}$~4 hold time	t_{CH}	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	35	-	40	-	50	-	ns
Write Pulse Width High	t_{WPH}	20	-	20	-	20	-	ns
Programming operation	t_{WHWH1}	14	-	14	-	14	-	µs
Erase operation(1)	t_{WHWH2}	3	-	3	-	3	-	s
Vcc setup time(4)	t_{VCS}	50	-	50	-	50	-	µs
Voltage Transition Time(2,4)	t_{VLHT}	4	-	4	-	4	-	ns
Write Pulse Width(2)	t_{WPP}	10	-	10	-	10	-	ns
$\overline{OE}$ Setup time to $\overline{WE1}$~4 active(2,4)	t_{OESP}	4	-	4	-	4	-	ns
$\overline{CS1}$~4 Setup time to $\overline{WE1}$~4 active(3,4)	t_{CSP}	4	-	4	-	4	-	ns

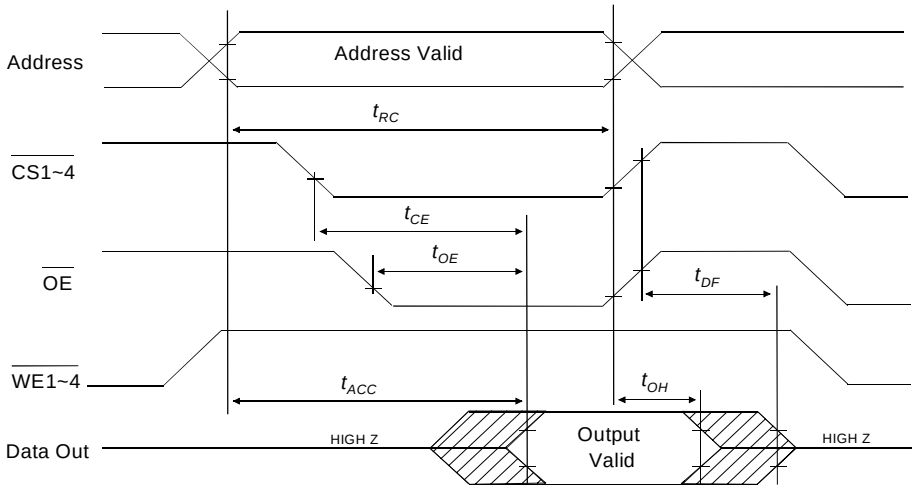
Notes: (1) This also includes the preprogramming time.
(2) These timings are for Sector Protect/Unprotect operations.
(3) This timing is only for Sector Unprotect.
(4) Not 100% tested.

Write/Erase/Program (Alternate $\overline{CS1\sim4}$ controlled Writes)

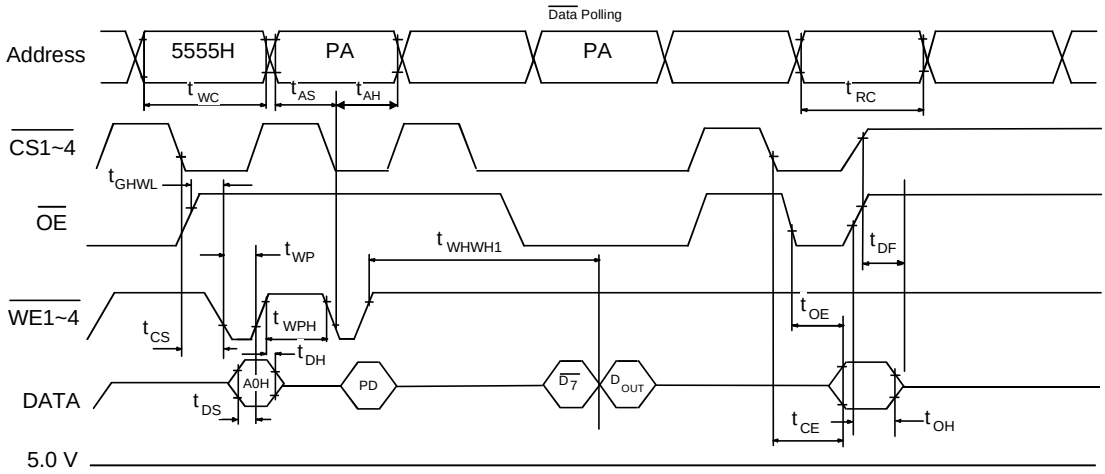
Parameter	Symbol	-70 min	-70 max	-90 min	-90 max	-12 min	-12 max	unit
Write Cycle time	t_{WC}	70	-	90	-	120	-	ns
Address Setup time	t_{AS}	0	-	0	-	0	-	ns
Address Hold time	t_{AH}	45	-	45	-	50	-	ns
Programming operation	t_{DS}	30	-	40	-	50	-	ns
Data hold Time	t_{DH}	0	-	0	-	0	-	ns
Output Enable Setup Time	t_{OES}	0	-	0	-	0	-	ns
Output Enable Hold Time	t_{OEH}	0	-	0	-	0	-	ns
$\overline{\text{Read R}}$ecover before Write	t_{GHEL}	0	-	0	-	0	-	ns
$\overline{\text{WE1}\sim4}$ setup time	t_{WS}	0	-	0	-	0	-	ns
$\overline{\text{WE1}\sim4}$ hold time	t_{WH}	0	-	0	-	0	-	ns
$\overline{\text{CS1}\sim4}$ Pulse Width	t_{CP}	35	-	40	-	50	-	ns
$\overline{\text{CS1}\sim4}$ Pulse Width High	t_{CPH}	20	-	20	-	20	-	ns
Programming operation	t_{WHWH1}	14	-	14	-	14	-	µs
Erase operation(1)	t_{WHWH2}	3	-	3	-	3	-	s
Vcc setup time(2)	t_{VCS}	2	-	2	-	2	-	µs

Notes: (1) This also includes the preprogramming time.
(2) Not 100% tested.

AC Waveforms for Read Operation



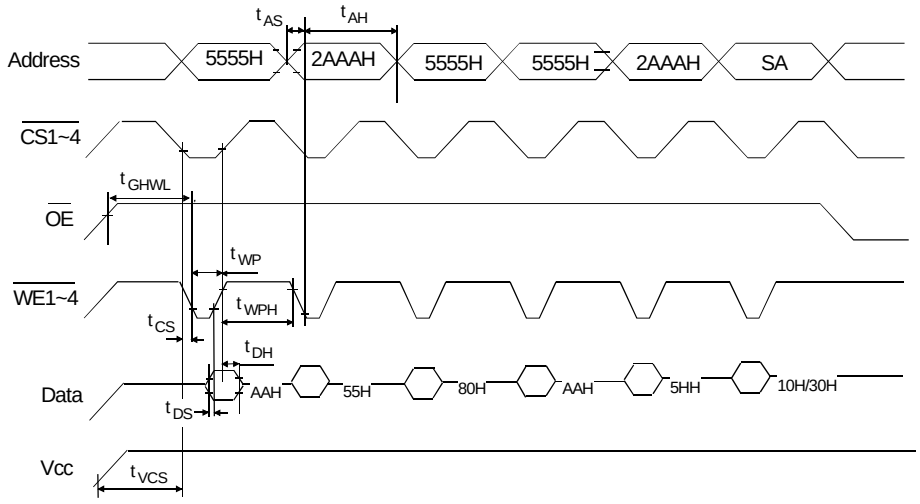
AC Programming Waveforms



Notes:

1. PA is address of the memory location to be programmed.
2. PD is data to be programmed at byte/word address.
3. $\overline{D_7}$ is the output of the complement of the data written to the device. $\overline{D_7}$ and $\overline{D_{15}}$ are used for 16 bit mode, whilst $\overline{D_7}$,$\overline{D_{15}}$,$\overline{D_{23}}$,$\overline{D_{31}}$ are used for 32 bit mode.
4. D_{OUT} is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.

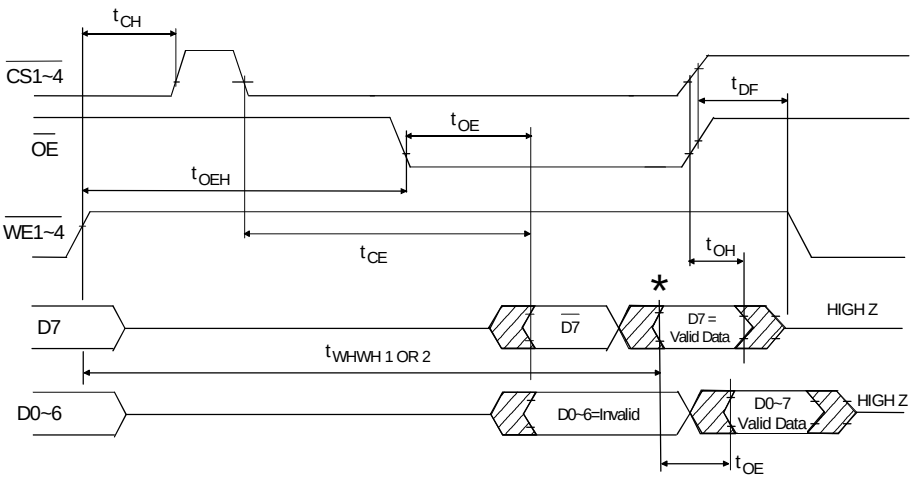
AC Chip / Sector Erase Waveforms



NOTES

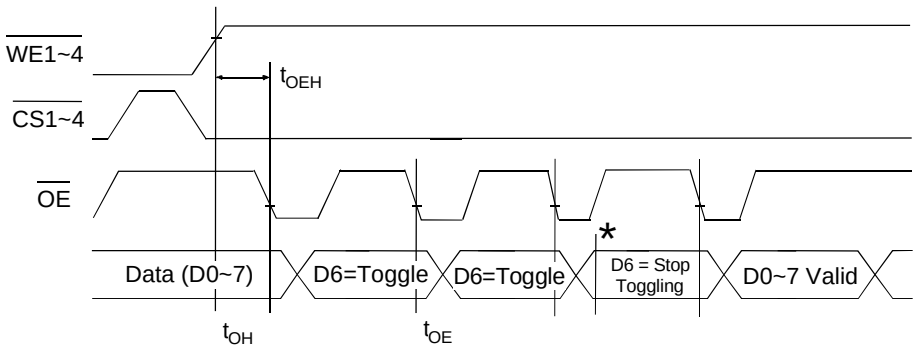
1. SA is the address for Sector Erase. Addresses = don't care for Chip Erase.
2. The data must be repeated on both bytes of the data bus for 16 bit mode and on all four bytes for 32 bit mode.

AC Waveforms for $\overline{\text{Data}}$ Polling During Embedded Algorithm Operations



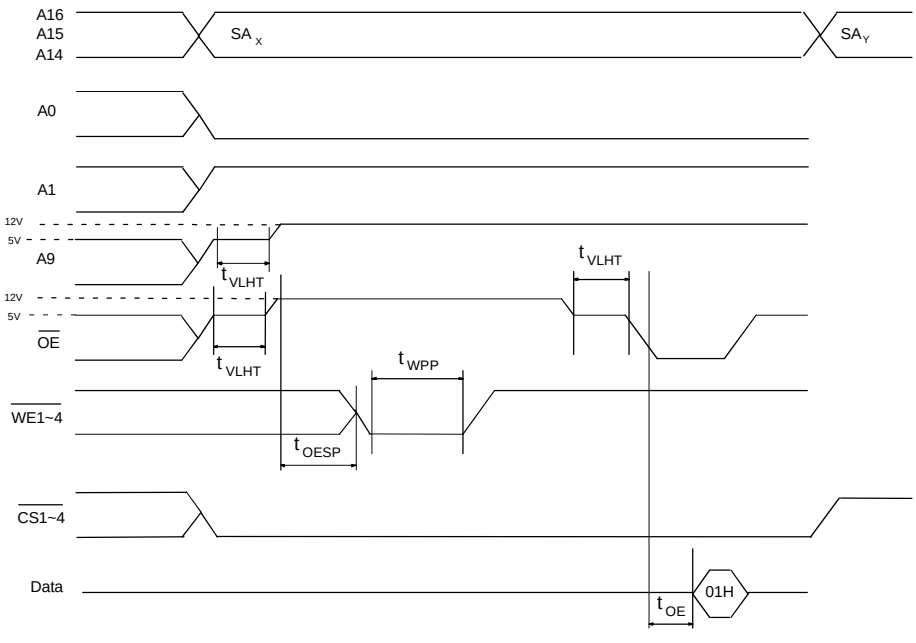
* $\overline{D_7}$ = Valid data(The device has completed the Embeded Operation).For 16 and 32 bit modes $\overline{D_7}$,$\overline{D_{15}}$ and $\overline{D_7}$,$\overline{D_{15}}$,$\overline{D_{23}}$,$\overline{D_{31}}$ are used respectively. 8 bit mode is shown above.

AC Waveforms for Toggle Bit During Embedded Algorithm Operations



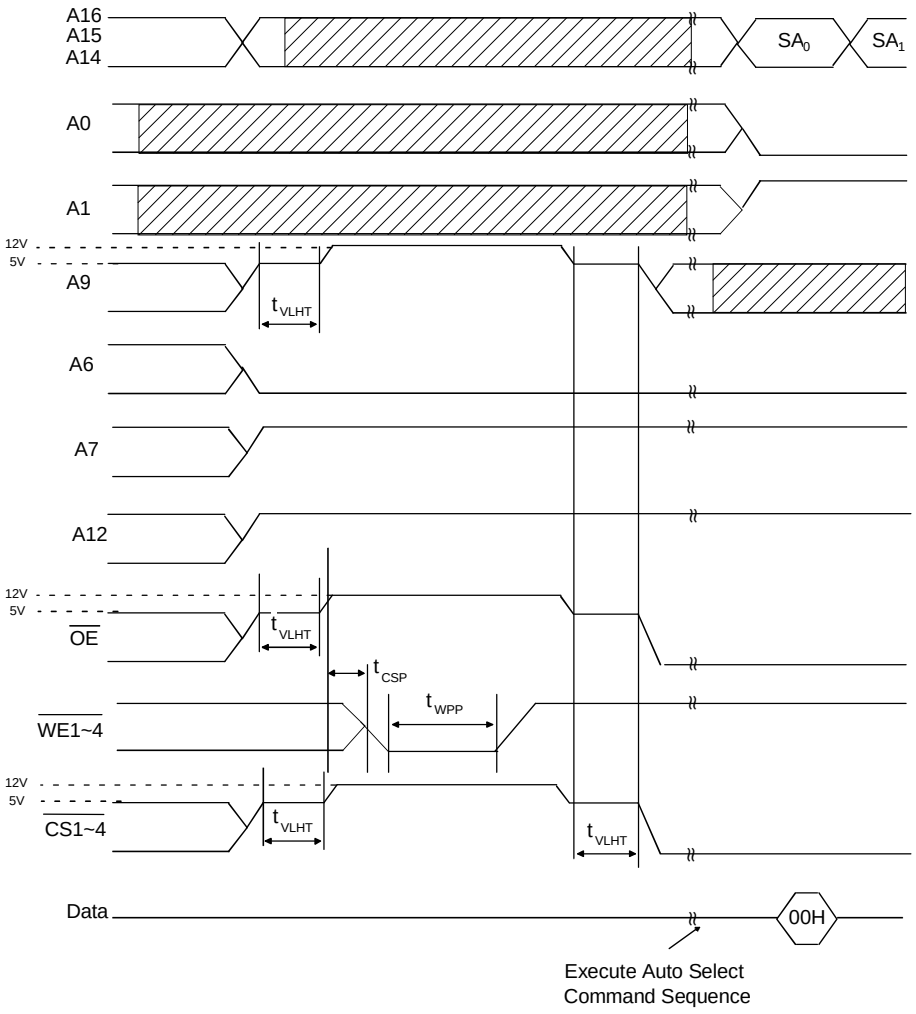
* D_6 stops toggling(The device has completed the Embedded operation). D_6,D_{14} and D_6,D_{14},D_{22},D_{30} are used for 16 bit and 32 bit modes respectively. 8 bit mode shown above.

AC Waveforms For Sector Protection

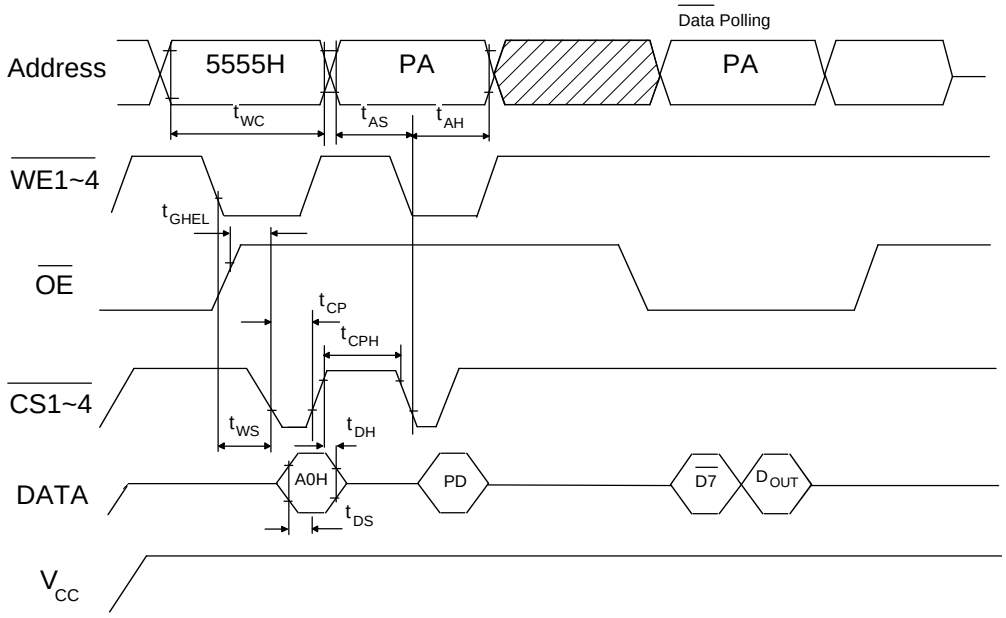


SAX = sector Addr for intial sector
SAY = sector Addr for next sector

AC Waveforms for Sector Unprotect



A.C Waveforms - Alternate $\overline{CS1~4}$ controlled Program operation timings



Notes:

1. PA is address of the memory location to be programmed.
2. PD is data to be programmed at byte/word address.
3. $\overline{D_7}$ is the output of the complement of the data written to the device. $\overline{D_7}$ and $\overline{D_{15}}$ are used for 16 bit mode, whilst $\overline{D_7}$,$\overline{D_{15}}$,$\overline{D_{23}}$,$\overline{D_{31}}$ are used for 32 bit mode.
4. D_{OUT} is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.

Command Definitions

Device operations are selected by writing specific address and data sequences into the command register. The following table defines these register command sequences for 8 bit mode. **For 16 and 32 bit mode, the data values in the table should be repeated on each byte of the data bus, when entering a command sequence. Data to be stored should be entered normally as 16 or 32 bit.**

COMMAND SEQUENCE	Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third bus Write Cycle		Forth bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read/Reset	4	5555H	AAH	2AAAH	55H	5555H	F0H	RA	RD				
Autoselect	4	5555H	AAH	2AAAH	55H	5555H	90H	00H/01H	01H/20H				
Byte Program	4	5555H	AAH	2AAAH	55H	5555H	A0H	PA	PD				
Chip erase	6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Sector erase	6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	SA	30H

NOTES:

1. Address bit A_{15}=X=Don't care. Write Sequences may be initiated with A_{15} in either state.
2. Address bit A_{16}=X=Don't care for all address commands except for Program Address (PA) and Sector Address (SA).
3. RA=Address of the memory location to be read.

   PA=Address of memory location to be programmed. Addresses are latched on the falling edge of the $\overline{WE1\sim4}$ pulse.

   SA=Address of the sector to be erased. The combination of A_{16}, A_{15} and A_{14} will uniquely select any sector in 32 bit mode.
4. RD=Data read from location RA during read operation.

   PD=Data to be programmed at location PA. Data is latched on the falling edge of $\overline{WE1\sim4}$

Read/Reset Command

The read or reset operation is initiated by writing the read/reset command sequence into the command register. Microprocessor read cycles retrieve array data from the memory. The device remains enabled for reads until the command register contents are altered.

The device will automatically power-up in the read/reset state. In this case, a command sequence is not required to read data. Standard microprocessor read cycles will retrieve array data. This default value ensures that no spurious alteration of memory content occurs during the power transition. Refer to the AC Read Characteristics and Waveforms for specific timing parameters.

Read Mode

The PUMA 2F4006 has two control functions which must be satisfied in order to obtain data at the outputs.
$\overline{CS}1{\sim}4$ is the power control and should be used for device selection
$\overline{OE}$ is the output control and should be used to gate data to the output pins if the device is selected.

Standby Mode

Two standby modes are available :
CMOS standby : $\overline{CS}1{\sim}4$ held at Vcc +/- 0.5V
TTL standby : $\overline{CS}1{\sim}4$ held at V_{IH}
In the standby mode the outputs are in a high impedance state independent of the $\overline{OE}$ input. If the device is deselected during erasure or programming the device will draw active current until the operation is completed.

Output Disable

With the $\overline{OE}$ input at a logic high level (V_{IH}), output from the device is disabled. This will cause the output pins to be in a high impedance state.

Autoselect

The autoselect mode allows the reading out of a binary code from the device and will identify the DIE manufacturer and type. This mode is intended for use by programming equipment. This mode is functional over the full military temperature range. The autoselect codes are as follows :

	A_{16}	A_{15}	A_{14}	A_1	A_0	CODE (HEX)	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
DIE Manufacturer code	X	X	X	V_{IL}	V_{IL}	01H	0	0	0	0	0	0	0	1
DIE device code	X	X	X	V_{IL}	V_{IH}	20H	0	0	1	0	0	0	0	0
Sector protection	Sector Address			V_{IH}	V_{IL}	01H*	0	0	0	0	0	0	0	1

* Outputs 01H at protected sector address. Outputs 00H at unprotected sector address.For 16 & 32 bit D0-D7 is repeated on each byte of the data bus.

To activate this mode the programming equipment must force V_{ID} (11.5 to 12.5V) on address A_9. Two identifier bytes may then be sequenced from each DIE device outputs by toggling A_0 from V_{IL} to V_{IH}. All addresses are dont care apart from A_1 & A_0. All identifiers for manufacturer and device will exhibit odd parity with D_7 defined as the parity bit.

The manufacturer and device codes may also be read via the command register, for instances when the PUMA 2F4006 is erased or programmed in a system without access to high voltage on A_9. All identifiers for manufacturers and device will exhibit odd parity with the MSB(D_7/D_{15}/D_{23}/D_{31}) defined as the parity bit. In order to read the proper device codes when executing the Autoselect, A_1 must be V_{IL}.

Write

Device erasure and programming are accomplished via the command register. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. The register is a latch used to store the commands along with the address and data information required to execute the command. The command register is written by bringing $\overline{WE}1{\sim}4$ to V_{IL} while $\overline{CS}1{\sim}4$ is at V_{IL} and $\overline{OE}$ is at V_{IH}.Addresses are latched on the falling edge of $\overline{WE}1{\sim}4$ while data is latched on the rising edge.

Sector Protection

The PUMA 2F4006 features hardware sector protection. This feature will disable both program and erase operations in any number of sectors (0 through 7). The sector protect feature is enabled using programming equipment at the users site. The device is shipped with all sectors unprotected.

To activate this mode, the programming equipment must force V_{ID} on address pin A_9 and control pin $\overline{OE}$. The sector adresses (A_{16}, A_{15} and A_{14}) should be set to the sector to be protected. Programming of the protection circuitry begins on the falling edge of the $\overline{WE1}$~4 pulse and is terminated with the rising edge of the same. Sector addresses must be held constant during the $\overline{WE1}$~4 pulse. (See Sector Address Table)

To verify programming of the protection equipment circuitry, the programming equipment must force V_{ID} on address pin A_9 with $\overline{CS1}$~4 and $\overline{OE}$ at V_{IL} and $\overline{WE1}$~4 at V_{IH}. Reading the device at a particular sector address (A_{16}, A_{15} and A_{14}) will produce 01H at data outputs (D_0-D_7/D_0-D_{15}/D_0-D_{31}) for a protected sector. Otherwise the device will read 00H for unprotected sector. In this mode, the lower order addresses, except for A_0 and A_1, are don't care. Address location 02H is reserved to verify sector protection of the device. Address pin A_1 must be held at V_{IH} and A_0 at V_{IL}. Address location 00H and 01H are reserved for autoselect codes. If a verify of the sector protection circuitry were done at these addresses, the device would output the manufacturer and device codes respectively

It is also possible to determine if a sector is protected in the system by writing the autoselect command. Performing a read operation at particular sector addresses (A_{16}, A_{15} and A_{14}) and with A_1=V_{IH} and A_0=V_{IL} (other addresses are a don't care) will produce 01H data if those sectors are protected. Otherwise the device will read 00H for an unprotected sector. (See Sector Protect/Unprotect Algorithms for more details.)

Sector Address Table

	A_{16}	A_{15}	A_{14}	Address Range
SA_0	0	0	0	00000H-03FFFH
SA_1	0	0	1	04000H-07FFFH
SA_2	0	1	0	08000H-0BFFFH
SA_3	0	1	1	0C000H-0FFFFH
SA_4	1	0	0	10000H-13FFFH
SA_5	1	0	1	14000H-17FFFH
SA_6	1	1	0	18000H-1BFFFH
SA_7	1	1	1	1C000H-1FFFFH

Autoselect Command

Flash memories are intended for use in applications where the local CPU alters memory contents. As such, manufacture and device codes must be accessible while the device resides in the target systems. PROM programmers typically access the signature codes by raising A_9 to a high voltage. However, multiplexing high voltage onto the address lines is not generally a desired system design practice.

The device contains an Autoselect operation to supplement traditional PROM programming methodology. The operation is initiated by writing the Autoselect command sequence into the command register. Following the command Write, a Read cycle from address XXX0H retrieves the manufacture code of 01H. A Read cycle from address XXX1H returns the device code 20H. A Read cycle from address XXX2H returns information as to which sectors are protected. All manufacturer and device codes will exhibit odd paritywith the MSB (D7) defined as the parity bit for 8 bit. D7 and D15 for 16 bit. D7, D15, D23 and D31 are used for 32 bit.

To terminate the operation, it is necessary to write the read/reset command sequence into the register.

Byte Programming

The device is programmed on a byte/word-by-byte/word basis. Programming is a four bus cycle operation. There are two "unlock" write cycle. These are followed by the program set-up command and data write cycles. The addresses are latched on the falling edge of $\overline{CS1{\sim}4}$ or $\overline{WE1{\sim}4}$ (whichever first), the data is latched on the rising edge of $\overline{CS1{\sim}4}$ or $\overline{WE1{\sim}4}$ (whichever first), and then programming begins. Upon executing the Embedded Program Algorithm Command sequence the system is not required to provide further controls or timings. The device will automatically provide adequate internally generated program pulses and verify the programmed cell margin. The automatic programming operation is completed when the data on D_7 is equivalent to data written to this bit (see write Operations Status) at which time the device returns to read mode and addresses are no longer latched. $\overline{Data}$ Polling must be performed at the memory location which is being programmed.

Programming is allowed in any address sequence and across sector boundaries. Beware that data "0" cannot be programmed back to a "1". Attempting to do so will hang up the device, or result in an apparent success according to the data polling algorithm. However, a read from Read/Reset Mode will show data is still "0". **Only an erase operation can convert "0"s to "1"s.**

Chip Erase

Chip erase is a six bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command. Two more "unlock" write cycles are then followed by the chip erase command.

Chip erase doesn't require the user to program the device prior to erase. Upon executing the Embedded Erase Algorithm command sequence the device automatically will program and verify the entire memory for an all zero data pattern prior to electrical erase. The systems is not required to provide any controls or timings during these operations.

The automatic erase begins on the rising edge of the last $\overline{WE1{\sim}4}$ pulse in the command sequence and terminates when the data on D_7,D_{15},D_{23},D_{31} are "1" (See Written Operation Section) at which time the device returns to read the mode.

Sector Erase

For 16 and 32 bit modes, the data values for the sector erase command sequence should be repeated on each byte of the data bus.

Sector erase is a six bus cycle operation. There are two "unlock"write cycles. These are followed by writing the "Set-up" command. Two more "unlock" write cycles are then followed by the sector erase command. The sector address (any address location within the desired sector) is latched on the falling edge of $\overline{WE1\sim4}$, while the command (data) is latched on the rising edge of $\overline{WE1\sim4}$. A time-out of 80µs from the rising edge of the last sector erase command will initiate the sector erase command(s).

Multiple sectors may be erased concurrently by writing the six bus cycle operations as desribed above. This sequence is followed with writes of the sector erase command (30H) to addresses in other sectors required to be concurrently erased. The time between writes must be less than 80µs, otherwise that command will not be accepted. It is recommended that processor interrupts be disabled during this time to guarantee this condition. The interrupts can be re-enabled after the last Sector Erase command(s). If another falling edge of $\overline{WE1\sim4}$ occurs within the 80µs time-out window , the timer is reset.(D_3,D_{11},D_{19},D_{27}, indicate if the timer window is still open on each 128K device on the module). Loading the sector erase buffer may be done in any sequence and with any number of sectors (0 to 7). Any command other than Sector Erase during this period will reset the device to read mode, ignoring the previous.

Sector erase doesn't require the user to program the device prior to erase. The device automatically programs all memory locations in the sector(s) to be erased prior to electrical erase. When erasing a sector or sectors the remaining unselected sectors are not affected. The system is not required to provide any controls or timings during these operations.

The automatic sector erase begins after the 100µs time-out from the rising edge of the $\overline{WE1\sim4}$ pulse for the last sector erase command pulse and terminates when the data on D_7,D_{15},D_{23} and D_{31} are "1" (see Write Operation Status Section) at which time the device returns to read mode. $\overline{Data}$ polling must be preformed at an address within any of the sectors being erased.

Write Operation Status

Hardware Sequence Flags :-

	STATUS	D_7	D_6	D_5	D_3	D_2-D_0
In Progress	Auto-Programming	$\overline{D_7}$	Toggle	0	0	Reserved for future use
	Programming in auto erase	0	Toggle	0	1	
	Erasing in Auto Erase	0	Toggle	0	1	
Exceeded Time limits	Auto-Programming	$\overline{D_7}$	Toggle	1	0	Reserved for future use
	Programming in auto erase	0	Toggle	1	1	
	Erasing in Auto-Erase	0	Toggle	1	1	

$\overline{Data}$ Polling - D_7,D_{15},D_{23},D_{31}

The PUMA 2F4006 features $\overline{Data}$ Polling as a method to indicate to the host system that the Embedded Algorithms are in progress or completed.

During the Embedded Programming Algorithm, an attempt to read the device will produce complement data of the data last written to D_7. Upon completion of the Embedded Programming Algorithm an attempt to read the device will produce the true data last written to D_7. $\overline{Data}$ Polling is valid after the rising edge of the forth $\overline{WE1\sim4}$ pulse in the four write pulse sequence.

During the Embedded Erase Algorithm, D_7 will be "0" until the erase operation is completed. Upon completion data at D_7 is "1". For chip erase, the $\overline{\text{Data}}$ Polling is valid after the rising edge of the sixth $\overline{\text{WE1~4}}$ pulse in the six write pulse sequence. For sector erase, $\overline{\text{Data}}$ Polling is valid after the last rising edge of the sector erase $\overline{\text{WE1~4}}$ pulse.

The $\overline{\text{Data}}$ Polling feature is only active during the Embedded Programming Algorithm, Embedded Erase Algorithm, or sector erase time-out. For 16 and 32 bit modes D_{15},D_{23} and D_{31} behave like D_7.

TOGGLE Bit - D_6,D_{14},D_{22},D_{30}

The PUMA 2F4006 also features the "toggle bit" as a method to indicate to the host system that the Embedded Algorithms are in progress or completed.

During an Embedded Program or Erase Algorithm cycle, successive attempts to read($\overline{\text{OE}}$ Toggling) data from the device will result in D_6 toggling between one and zero. Once the Embedded Program or Erase Algorithm cycle is completed, D_6 will stop toggling and valid data will be read on successive attempts. During programming, the Toggle bit is valid after the rising edge of the forth $\overline{\text{WE1~4}}$ pulse in the four write pulse sequence. For chip erase, the Toggle bit is valid after the sixth $\overline{\text{WE1~4}}$ pulse in the six write pulse sequence.

For sector erase, the Toggle bit is valid after the last rising edge of the sector erase $\overline{\text{WE1~4}}$ pulse. The Toggle Bit is active during the sector time-out. Note: $\overline{\text{CS1~4}}$ or $\overline{\text{OE}}$ toggling will toggle D_6. For 16 and 32 bit modes D_{14},D_{22} and D_{30} behave like D_6.

Exceeding Time Limits - D_5,D_{13},D_{21},D_{29}

D_5 will indicate if the program or erase time has exceeded the specified limits. Under these conditions D_5 will produce "1", indicating the program or erase cycle was not successfully completed . $\overline{\text{Data}}$ Polling is the only operating function of the device under this condition. The $\overline{\text{CS1~4}}$ circuit will partially power down the device under these conditions (to approximately 2mA). The $\overline{\text{OE}}$ and $\overline{\text{WE1~4}}$ pins will control the output disable functions . To reset the device, write reset command sequence to the device. This allows the system to continue to use the other active sectors in the device.

If this failiure condition occurs during the sector erase operation, it specifies that a particular sector is bad and it may not be reused. However, other sectors are still functional and may be used for additional program or erase operations. The device must be reset to use other sectors. Write the Reset command sequence to the device, and then execute the program or erase command sequence.

If this failure condition occurs during the chip erase operation, it specifies that the entire chip is bad or combination of sectors are bad.

If this failure condition occurs during the byte programming operation, it specifies that the entire sector containing that byte is bad and this sector may not be reused(other sectors are still functional and can be reused). The device must be reset to use other sectors.

The D_5 failure condition may also appear if a user tries to program a non blank location without erasing. In this case the system never reads valid data on the D_7 bit and D_6 never stops toggling. Once the device has exceeded timing limits, the D_5 bit will indicate a "1". Please note that this is not a device failure condition since the device was incorrectly used. The device must be reset to continue using the device.For 16 and 32 bit modes D_{13},D_{21} and D_{29} behave like D_5.

Hardware Sequence Flag - D_4 ,D_{12},D_{20},D_{28}

If the device has exceeded the specified erase or program time and D_5 is "1", then D_4 will indicate at which step in the algorithm the device exceeded the limits. A "0" in D_4 indicates in programming, a "1" indicates an erase.

If $\overline{\text{Data}}$ Polling or the Toggle Bit indicates the device has been written with a valid erase command, D_3 may be used to determine if the sector erase timer window is still open. If D_3 is high the internally controlled erase cycle has begun; attempts to write subsequent commands to the device will be ignored until the erase operation is completed as indicated by $\overline{\text{Data}}$ Polling or Toggle Bit. If D_3 is low , the device will accept additional sector erase commands. To insure the command has been accepted, the software should check the status of D_3 prior to and following each subsequent sector erase command. If D_3 were high on the second status check, the command may not have been accepted. For 16 and 32 bit configurations D_3,D_{11} and D_3,D_{11},D_{19},D_{27} are used respectively.

Sector Erase Timer - D_3, D_{11}, D_{19}, D_{27}

After the completion of the initial sector erase command sequence the sector erase time-out will begin. D_3 will remain low until the time-out is complete. $\overline{\text{Data}}$ Polling and Toggle Bit are valid after the initial sector erase command sequence. For 16 and 32 bit configurations D_{11},D_{19} and D_{27} behave like D_3.

Data Protection

The PUMA 2F4006 is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transition. During power up the device automatically resets the internal state machine in the Read mode. Also, with its controls register architecture , alteration of the memory contents only occurs after successful completion of specific multi-bus cycle command sequences. The device also incorporates several features to prevent inadvertent write cycles resulting from Vcc power up and power down transitions or system noise.

Low V_{CC} Write Inhibit

To avoid initiation of a write cycle during V_{CC} power up and power down, a write cycle is locked out for V_{CC} less than 3.2V (typically 3.7V). If $V_{CC}<V_{LKO}$, the command register is disabled and all internal program/erase circuits are disabled. Under this condition the device will reset to read mode. Subsequent writes will be ignored until the V_{CC} level is greater than V_{KLO}. It is usually correct to prevent unintentional writes when V_{CC} is above 3.2V.

Write Pulse "Glitch" Protection

Noise pulses of less than 5ns (typical) on $\overline{\text{OE}}$, $\overline{\text{CS1~4}}$, $\overline{\text{WE1~4}}$ will not initiate a write cycle.

Logical Inhibit

Writing is inhibited by holding any one of $\overline{\text{OE}}=V_{IL}$, $\overline{\text{CS1~4}}=V_{IH}$ or $\overline{\text{WE1~4}}=V_{IH}$. To initiate a write cycle $\overline{\text{CS1~4}}$ and $\overline{\text{WE1~4}}$ must be logical zero while $\overline{\text{OE}}$ is a logical one.

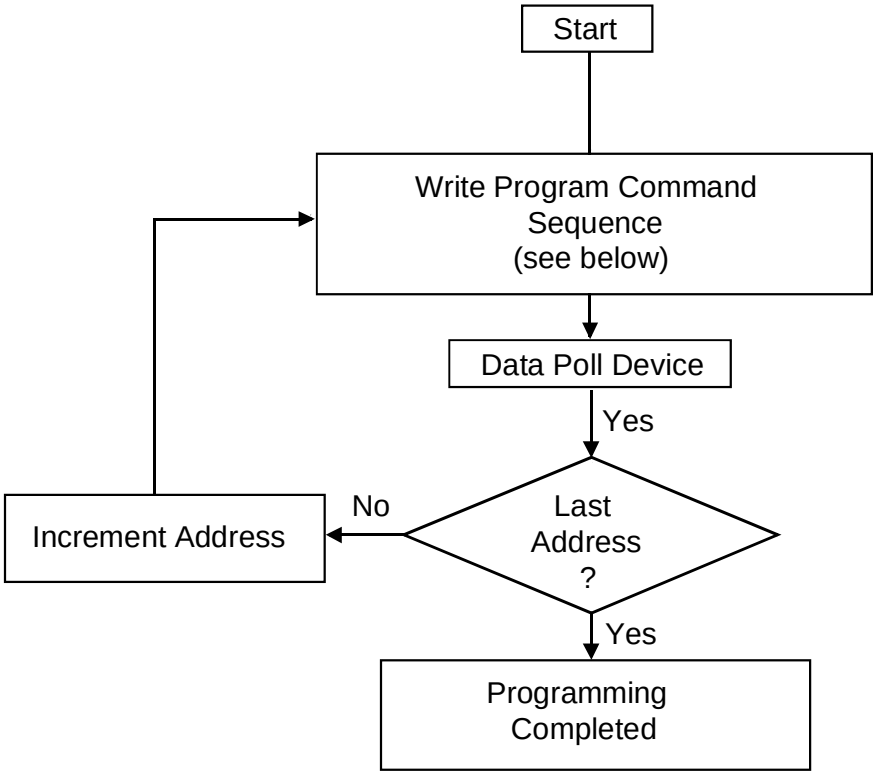
Power-Up Write Inhibit

Power-up of the device with $\overline{\text{WE1~4}}=\overline{\text{CS1~4}}=V_{IL}$ and $\overline{\text{OE}}=V_{IH}$ will not accept commands on the rising edge of $\overline{\text{WE1~4}}$. The internal state machine is automatically reset to the read mode on power-up.

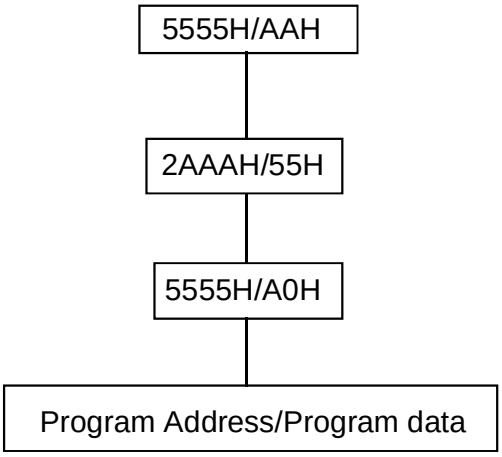
Sector Protect

Sectors of the PUMA 2F4006 may be hardware protected at the users factory. The protection circuitry will disable both program and erase functions for the protected sector(s). Requests to program or erase a protected sector will be ignored by the device.

Embedded Programming Algorithm

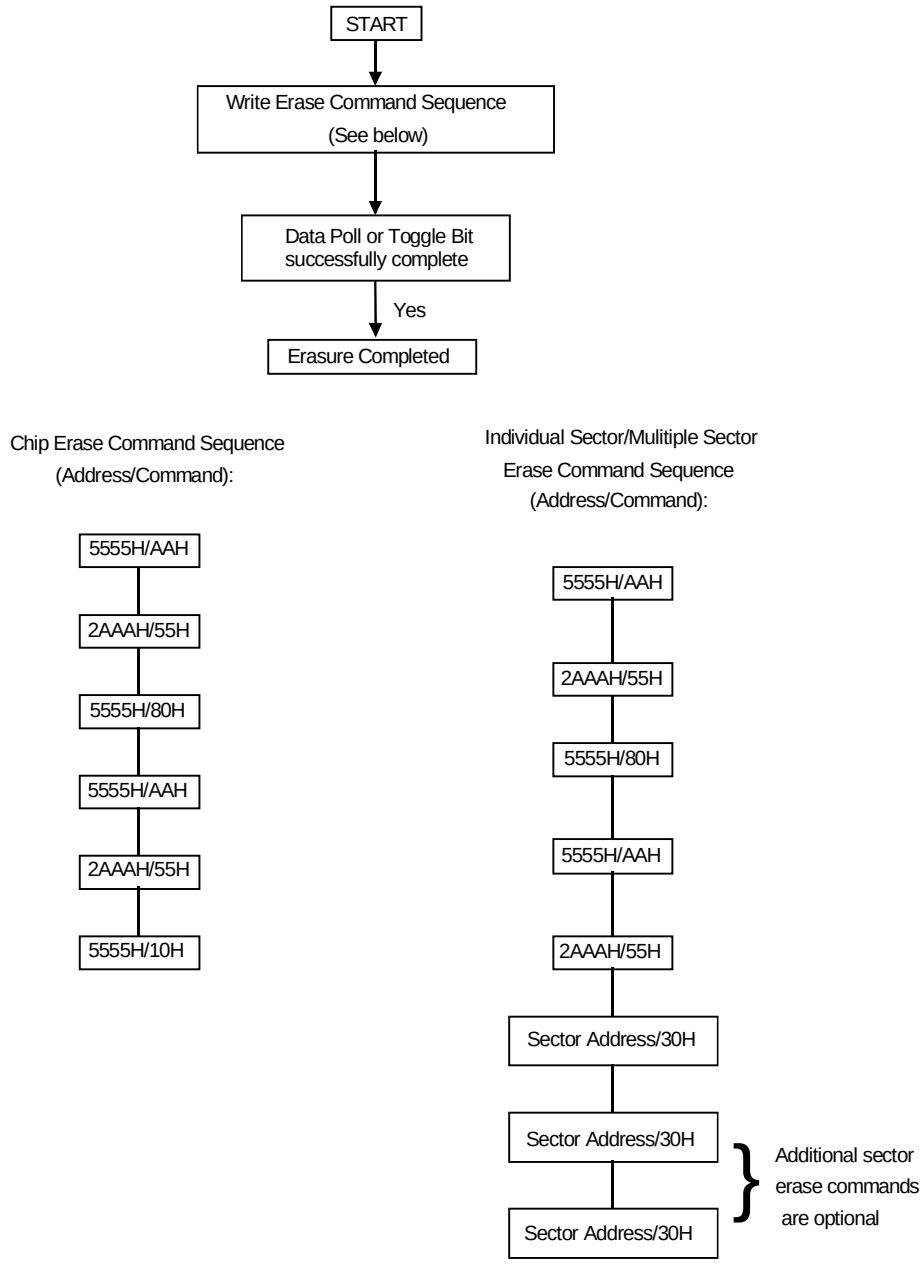


Program Command Sequence (Address /Command)



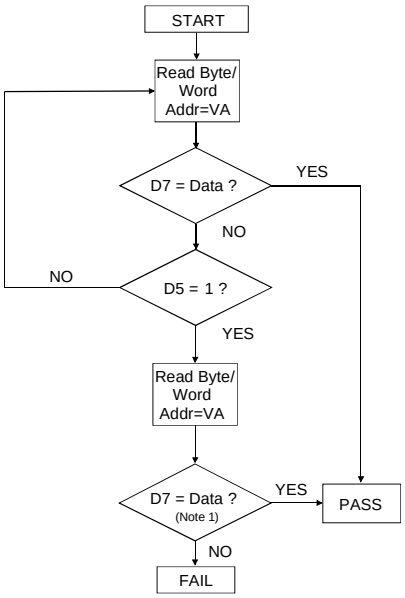
NOTE: AA_H,55_H, and $A0_H$ above should be repeated on each byte of the data bus for 16 and 32 bit configurations, program data should be entered normally in 8,16 or 32 bit form.

Embedded Erase Algorithm



NOTE: All data above should be repeated on each byte of the data bus for 16 and 32 bit configurations.

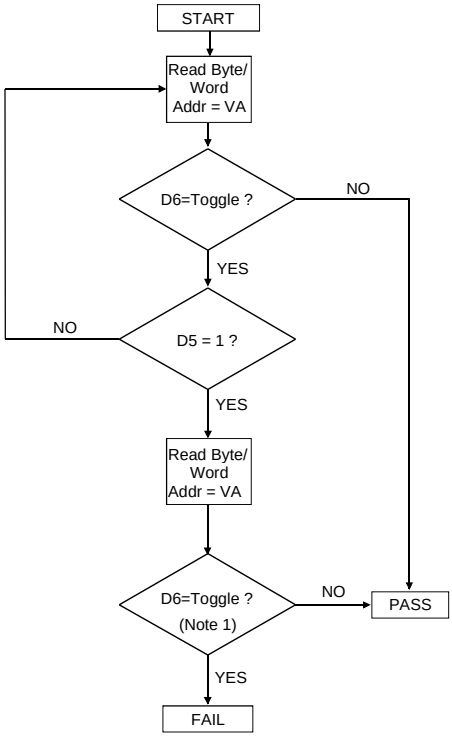
Data Polling Algorithm



VA = Byte/Word Address for programming.
= Any of the sector address within the sector erase during sector erase operation.
= XXXXH during Chip Erase

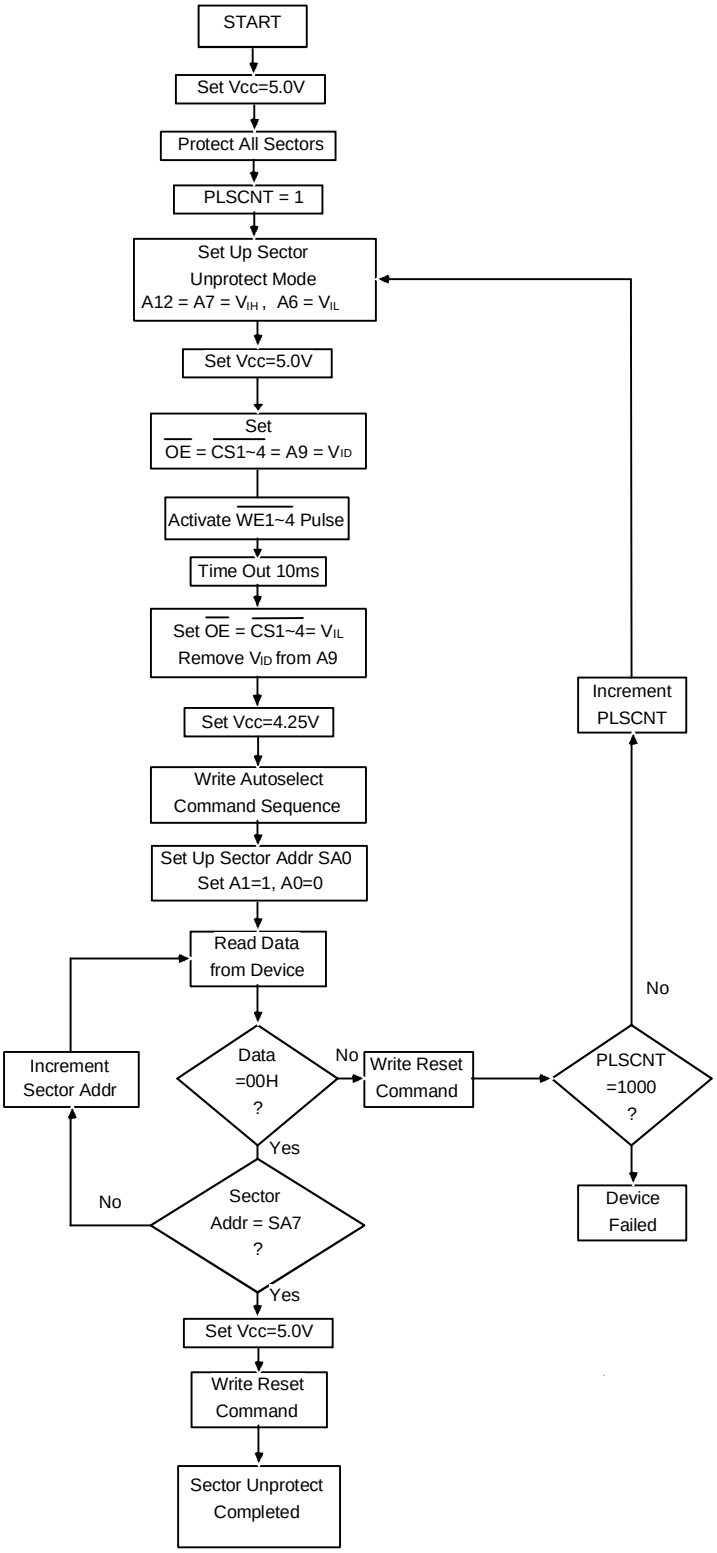
NOTE:
1. D_7 is rechecked even if D_5 = 1 because D_7 may change simultaneously with D_5.
2. For 16 and 32 bit D_5,**D_7**,D_{13},**D_{15}** and D_5,**D_7**,D_{13},**D_{15}**,D_{21},**D_{23}**,D_{29},**D_{31}** are used respectively. **Bold**=data polling bits.

TOGGLE Bit Algorithm



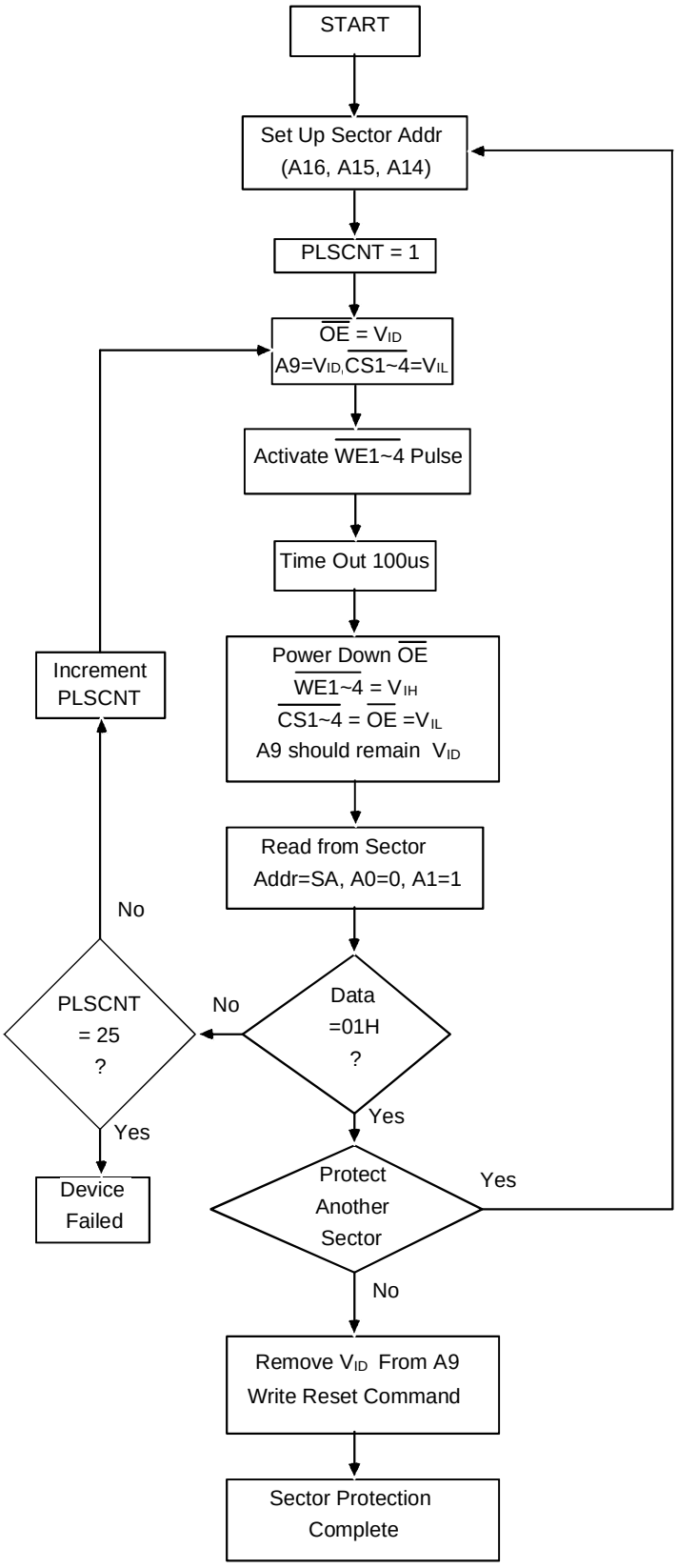
NOTE:
1. D_6 is rechecked even if D_5 = 1 because D_6 may stop toggling at the same time as D_5 changing to "1".
2. For 16 and 32 bit D_5,**D_6**,D_{13},**D_{14}** and D_5,**D_6**,D_{13},**D_{14}**,D_{21},**D_{22}**,D_{29},**D_{30}** are used respectively. **Bold**=Toggle bits.

Sector Unprotect Algorithm



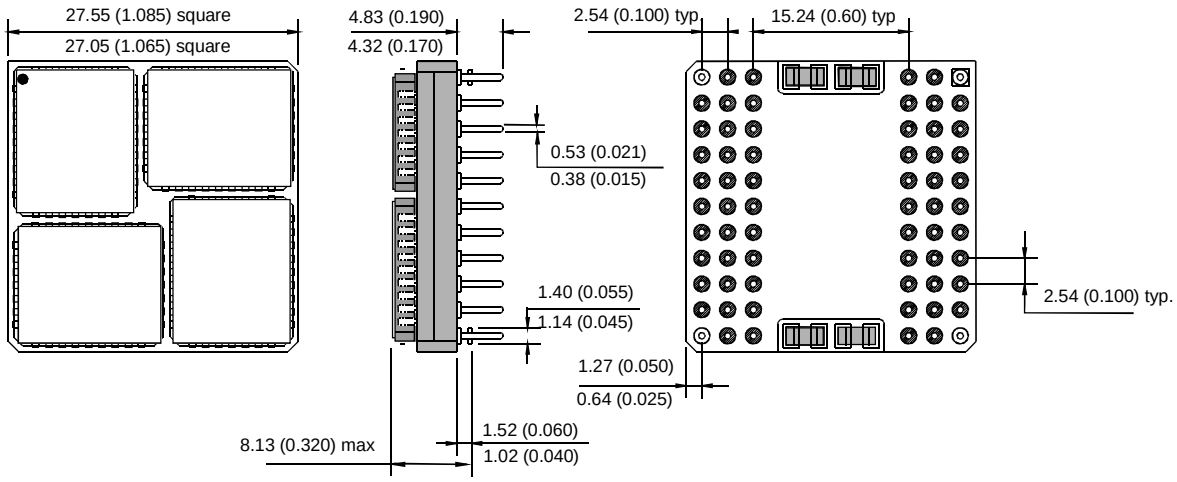
NOTES:
SA0 = Sector Addr for intial sector
SA7 = Sector Addr to last sector

Sector Protection Algorithm



Package Details Dimensions in mm(inches).

PUMA 2 - 66 Pin Ceramic PGA



Military Screening Procedure

Module Screening Flow for high reliability product is in accordance with MIL-STD-883 method 5004 Level B and is detailed below:

MODULE SCREENING FLOW

SCREEN	*TEST METHOD*	*LEVEL*
Visual and Mechanical		
External visual	2017 Condition B or manufacturers equivalent	100%
Temperature cycle	1010 Condition C (10 Cycles,-65°C to +150°C)	100%
Burn-In		
Pre-Burn-in electrical	Per applicable device specifications at T_A=+25°C	100%
Burn-in	T_A=+125°C,160hrs minimum.	100%
Final Electrical Tests	Per applicable Device Specification	
Static (DC)	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Functional	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Switching (AC)	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Percent Defective allowable (PDA)	Calculated at post-burn-in at T_A=+25°C	5%
Quality Conformance	Per applicable Device Specification	Sample
External Visual	2009 Per vendor or customer specification	100%

Ordering Information

PUMA 2F4006MB-70E

	E	=	100,000 W/E Cycles
Speed	70	=	70 ns
	90	=	90 ns
	12	=	120 ns
Temp. range/screening	Blank	=	Commercial Temp.
	I	=	Industrial Temp (-40°C to +85°C)
	M	=	Military Temp (-55°C to 125°C)
	MB	=	Screened in accordance with MIL-STD-883.
Organisation	4006	=	User configurable as 128K x 32, 256K x 16, or 512K x 8.
Technology	F	=	FLASH Memory
Package	PUMA 2	=	66 pin ceramic PGA.