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HYUNDAI SEMICONDUCTOR HY531000

1M×1-Bit CMOS DRAM

M171202B-JAN92

DESCRIPTION

The HY531000 is a high speed, low power 1,048,576×1 bit CMOS dynamic random access memory. Fabricated with the HYUNDAI CMOS process, the HY531000 offers a fast page mode for high bandwidth operation, fast usable speed, CMOS standby current, and inherently high CMOS reliability.

All inputs and output are TTL compatible. Fast page mode operation allows random or sequential access of up to 1,024 bits within a row with cycle times as fast as 40ns.

The HY531000 design is optimized for cache based mainframe and minicomputers, graphics, digital signal processing, and high performance microprocessor systems.

FEATURES

- **Low power dissipation**
  - **Operating Current, 100ns : 55mA(max.)**
  - **TTL Standby Current : 2mA(max.)**
  - **CMOS Standby Current : 1mA(max.)**
- **Read-Modify-Write Capability**
- **$\overline{RAS}$-only, Hidden, $\overline{CAS}$-before-$\overline{RAS}$ Refresh Capability**
- **Common I/O capability**
- **Fast Page mode operation for a sustained data rate up to 25 MHz**
- **512 refresh cycles/8 ms**
- **High reliability 300 mil 18 pin P-DIP and 20/26 pin SOJ**
- **Fast access time and cycle time (ns)**

	HY531000-60	HY531000-70	HY531000-80	HY531000-10
Max $\overline{RAS}$ Access Time, t_{RAC}	60	70	80	100
Max $\overline{CAS}$ Access Time, t_{CAC}	20	20	20	25
Min Fast Page Mode Cycle Time, t_{PC}	40	40	45	55
Min Cycle Time, t_{RC}	120	130	150	180

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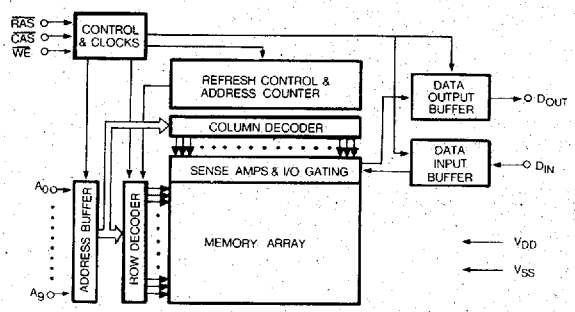
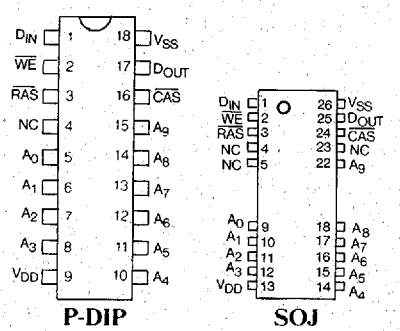
BLOCK DIAGRAM



PIN CONNECTIONS



PIN NAMES

$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{WE}$	WRITE ENABLE
A_0-A_9	ADDRESS INPUT
D_{IN}	DATA INPUT
D_{OUT}	DATA OUTPUT
V_{DD}	POWER(+5V)
V_{SS}	GROUND

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ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	°C
T_{STG}	Storage Temperature	−55 to 150	°C
V_{TERM}	Voltage on Any Pin Relative to V_{SS}	−1.0 to 7.0	V
V_{DD}	Voltage on V_{DD} Relative to V_{SS}	−1.0 to 7.0	V
I_{OUT}	Short Circuit Output Current	50	mA
P_T	Power Dissipation	0.6	W

NOTE : Stress above those listed under "Absolute Maximum Rating" might cause permanent damage to the device.

DC CHARACTERISTICS

(T_A=0 °C to 70 °C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED	HY531000 MIN.	HY531000 MAX.	UNIT	NOTE
$\|I_{LI}\|$	Input Leakage Current(any input pin)	$V_{SS} \le V_{IN} \le V_{DD}$			10	μA	
$\|I_{LO}\|$	Output Leakage Current for High Impedance State	$V_{SS} \le D_{OUT} \le V_{DD}$ $\overline{RAS}$, $\overline{CAS}$ at V_{IH}		–	10	μA	
I_{DD1}	V_{DD} Supply Current, Operating	$t_{RC}=t_{RC}$(min.)	−60	–	85	mA	1, 2
			−70	–	75		
			−80	–	65		
			−10	–	55		
I_{DD2}	V_{DD} Supply Current, TTL Standby	$\overline{RAS}$, $\overline{CAS}$ at V_{IH} other inputs ≥ V_{SS}		–	2	mA	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-only Refresh	$t_{RC}=t_{RC}$(min.)	−60	–	85	mA	2
			−70	–	75		
			−80	–	65		
			−10	–	55		
I_{DD4}	V_{DD} Supply Current, Fast page mode	Minimum Cycle	−60	–	65	mA	1, 2
			−70	–	55		
			−80	–	45		
			−10	–	35		
I_{DD5}	V_{DD} Supply Current, CMOS Standby	$\overline{RAS} \ge V_{DD}-0.2V$, $\overline{CAS}=V_{IH}$, other inputs≥V_{SS}		–	1	mA	
I_{DD6}	V_{DD} Supply Current, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh	$t_{RC}=t_{RC}$(min.)	−60	–	85	mA	2
			−70	–	75		
			−80	–	65		
			−10	–	55		
V_{IL}	Input Low Voltage(all inputs)			−1	0.8	V	
V_{IH}	Input High Voltage(all inputs)			2.4	V_{DD}+1	V	
V_{OL}	Output Low Voltage	I_{OL}=4.2mA		–	0.4	V	
V_{OH}	Output High Voltage	I_{OH}=−5mA		2.4	–	V	

NOTES:
1. I_{DD} is dependent on output loading when the device output is selected. Specified I_{DD}(max.) is measured with output open.
2. I_{DD} is dependent upon the number of address transitions, Specified I_{DD}(max.) is measured with a maximum of two transitions per address cycle in Fast page mode.

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AC CHARACTERISTICS

(T_A=0 ℃ to 70 ℃, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

#	SYMBOL	PARAMETER	HY531000								UNIT	NOTE
			60		70		80		10			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	t_{RAS}	$\overline{RAS}$ Pulse Width	60	10K	70	10K	80	10K	100	10K	ns	
2	t_{RC}	Random Read or Write Cycle Time	120	–	130	–	150	–	180	–	ns	
3	t_{RP}	$\overline{RAS}$ Precharge Time	50	–	50	–	60	–	70	–	ns	
4	t_{ASR}	Row Address Set-up Time	0	–	0	–	0	–	0	–	ns	
5	t_{RAH}	Row Address Hold Time	10	–	10	–	10	–	15	–	ns	
6	t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	–	35	–	40	–	50	–	ns	
7	t_{RAD}	$\overline{RAS}$ to Column Address Delay Tme	15	30	15	35	15	40	20	50	ns	1
8	t_{ASC}	Column Address Set-up Time	0	–	0	–	0	–	0	–	ns	
9	t_{CAH}	Column Address Hold Time	15	–	15	–	15	–	20	–	ns	
10	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	20	40	20	50	20	60	25	75	ns	2
11	t_{RAC}	Access Time From $\overline{RAS}$	–	60	–	70	–	80	–	100	ns	3,4,5
12	t_{AA}	Access Time From Column Address	–	30	–	35	–	40	–	50	ns	5,7
13	t_{CAC}	Access Time From $\overline{CAS}$	–	20	–	20	–	20	–	25	ns	5,6
14	t_{CAS}	$\overline{CAS}$ Pulse Width	20	10K	20	10K	20	10K	25	10K	ns	
15	t_{RSH}	$\overline{RAS}$ Hold Time	20	–	20	–	20	–	25	–	ns	
16	t_{RCS}	Read Command Set-up Time	0	–	0	–	0	–	0	–	ns	
17	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	0	–	0	–	0	–	0	–	ns	8
18	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0	–	0	–	0	–	0	–	ns	8
19	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	5	–	5	–	5	–	ns	
20	t_{OFF}	Output Buffer Turn Off Delay	0	20	0	20	0	20	0	20	ns	9
21	t_{OH}	Output Data Hold Time From $\overline{CAS}$	0	–	0	–	0	–	0	–	ns	9
22	t_{WP}	Write Pulse Width	15	–	15	–	15	–	20	–	ns	
23	t_{CP}	$\overline{CAS}$ Precharge Time	10	–	10	–	10	–	10	–	ns	
24	t_{AR}	Column Address Hold Time From $\overline{RAS}$	50	–	55	–	60	–	75	–	ns	
25	t_{WCR}	Write Command Hold Time From $\overline{RAS}$	50	–	55	–	60	–	75	–	ns	
26	t_{WCS}	Write Command Set-up Time	0	–	0	–	0	–	0	–	ns	10
27	t_{WCH}	Write Command Hold Time	15	–	15	–	15	–	20	–	ns	
28	t_{DS}	Data-In Set-up Time	0	–	0	–	0	–	0	–	ns	11
29	t_{DH}	Data-In Hold Time	15	–	15	–	15	–	20	–	ns	11
30	t_{DHR}	Data-In Hold Time Reference to $\overline{RAS}$	50	–	55	–	60	–	75	–	ns	
31	t_{RWC}	RMW Cycle Time	145	–	155	–	175	–	210	–	ns	
32	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay in RMW Cycle	60	–	70	–	80	–	100	–	ns	10
33	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	20	–	20	–	20	–	25	–	ns	10
34	t_{AWD}	Column Address to $\overline{WE}$ Delay	30	–	35	–	40	–	50	–	ns	10
35	t_{CPA}	Access Time From $\overline{CAS}$ precharge	–	35	–	35	–	40	–	50	ns	5,12

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#	SYMBOL	PARAMETER	HY531000								UNIT	NOTE
			60		70		80		10			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
36	t_{PC}	Fast page mode Read or Write Cycle time	40	–	40	–	45	–	55	–	ns	
37	t_{PCM}	Fast page mode Read-Modify-Write Cycle	65	–	65	–	70	–	85	–	ns	
38	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	20	–	20	–	25	–	ns	
39	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	20	–	20	–	25	–	ns	
40	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	0	–	0	–	0	–	ns	
41	t_{CSR}	$\overline{CAS}$ Set-up Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	5	–	5	–	5	–	5	–	ns	
42	t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	15	–	15	–	15	–	20	–	ns	
43	t_{CSH}	$\overline{CAS}$ Hold Time	60	–	70	–	80	–	100	–	ns	
44	t_T	Transition Time(Rise and Fall)	3	50	3	50	3	50	3	50	ns	13,14
45	t_{CLZ}	$\overline{CAS}$ to output in Low-Z	0	–	0	–	0	–	0	–	ns	5
46	t_{REF}	Refresh Interval(512 Cycle)	–	8	–	8	–	8	–	8	ms	15
47	t_{RASP}	$\overline{RAS}$ Pulse Width Fast Page Mode	60	100K	70	100K	80	100K	100	100K	ns	
48	t_{CPT}	$\overline{CAS}$ Precharge Time (CBR Counter Test Cycle)	40	–	40	–	40	–	50	–	ns	

NOTES :

1. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a referenced point only. If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then the access time is controlled by t_{AA}.
2. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a referenced point only. If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then the access time is controlled by t_{CAC}.
3. Assume $t_{RAD} \leq t_{RAD}$(max.). If t_{RAD} is greater than t_{RAD}(max.) then t_{RAC} will increase by the amount that t_{RAD} exceeds t_{RAD}(max.).
4. Assume $t_{RCD} \leq t_{RCD}$(max.). If t_{RCD} is greater than t_{RCD}(max.) then t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD}(max.).
5. Measured with a load equivalent to two TTL loads and 100 pF.
6. Assumes that $t_{RCD} \geq t_{RCD}$ (max.), $t_{RAD} \leq t_{RAD}$ (max.)
7. Assumes that $t_{RCD} \leq t_{RCD}$(max.) and $t_{RAD} \geq t_{RAD}$(max.)
8. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
9. t_{OFF} and t_{OH} define the time at which the data output achieves the open circuit condition and is not referenced to the output voltage levels.
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only : If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle ; if $t_{RWD} \geq t_{RWD}$(min), $t_{CWD} \geq t_{CWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), the cycle is a read/write and the data output will contain data from the selected cell ; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time)is indeterminate.
11. t_{DS} and t_{DH} are referenced to the latter occurence of $\overline{CAS}$ or $\overline{WE}$
12. Access time is determined by the longer of t_{AA}, t_{CAC}, or t_{CPA}.
13. t_T is measured between V_{IH}(min.) and V_{IL}(max.).
14. AC measurements assume t_T=5ns.
15. An initial pause of 200μs is required after power-up and followed by a minimum of 8 initialization cycles(any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh). 8 initialization cycles are required after extended period of bias without clocks.

CAPACITANCE

(T_A=25 °C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Address, Data In	–	5	pF
C_{IN2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	–	7	pF
C_{OUT}	Data Out	–	7	pF

NOTE : Capacitance is measured at worst case of voltage levels with a programmable capacitance meter.

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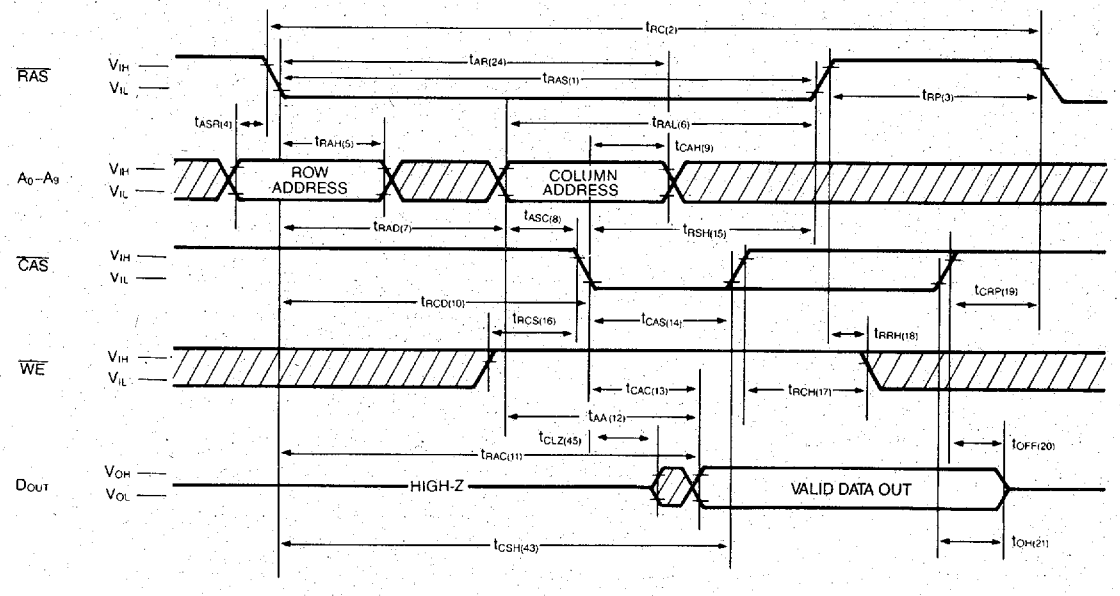
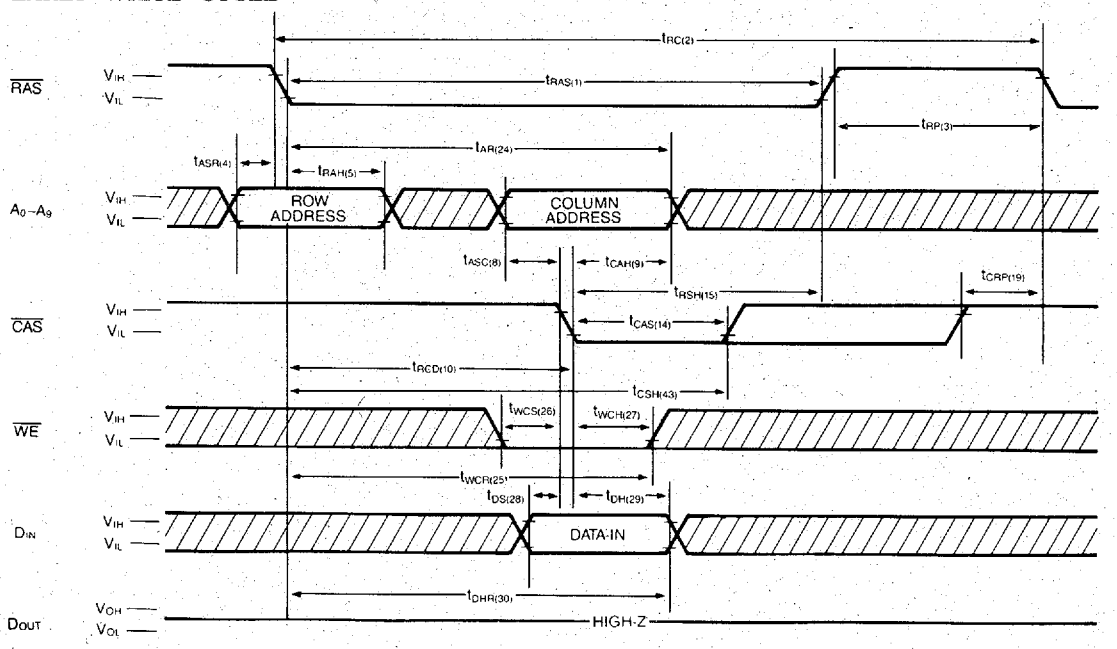
TIMING DIAGRAM

READ CYCLE



EARLY WRITE CYCLE



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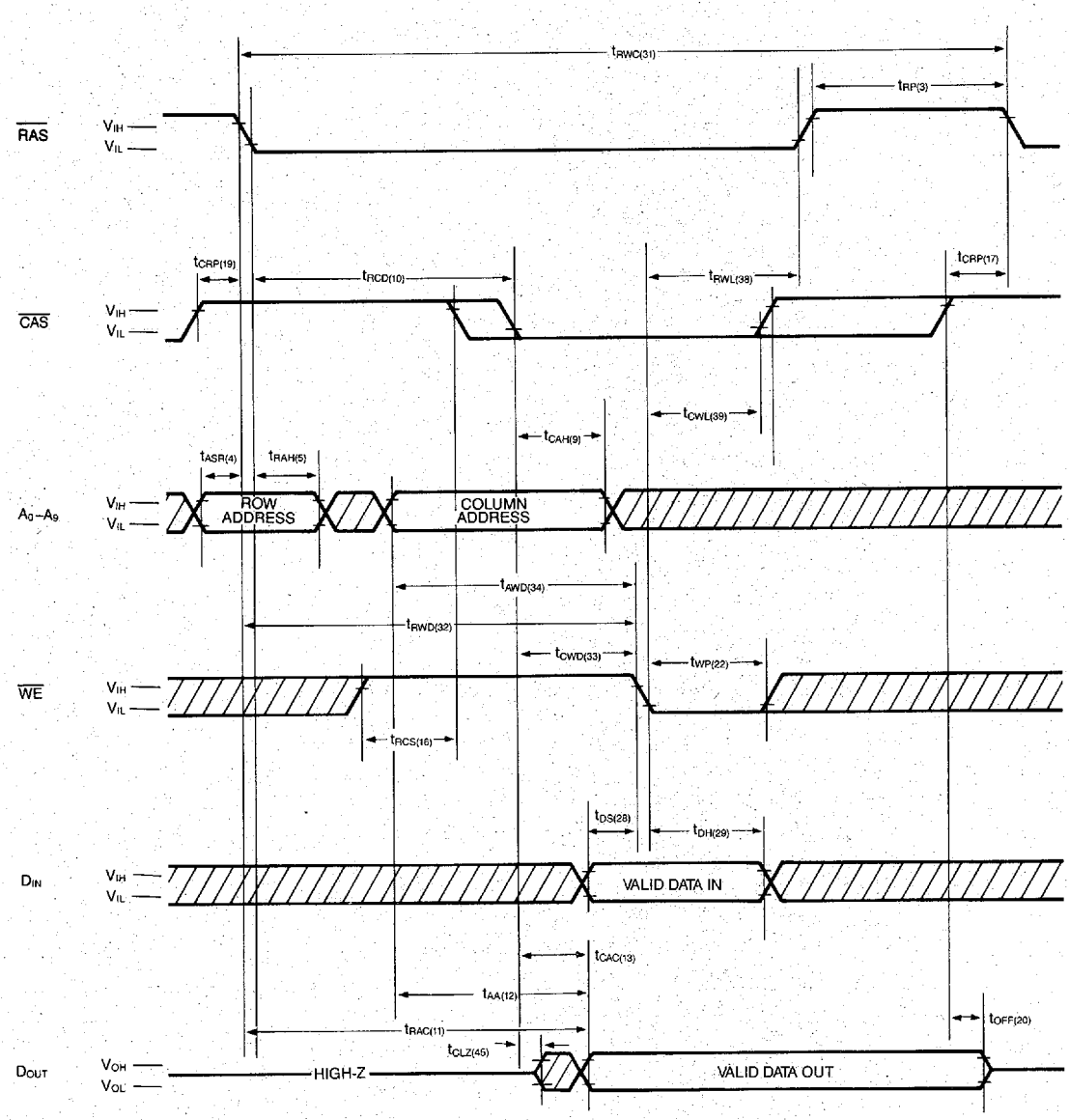
READ-MODIFY-WRITE CYCLE



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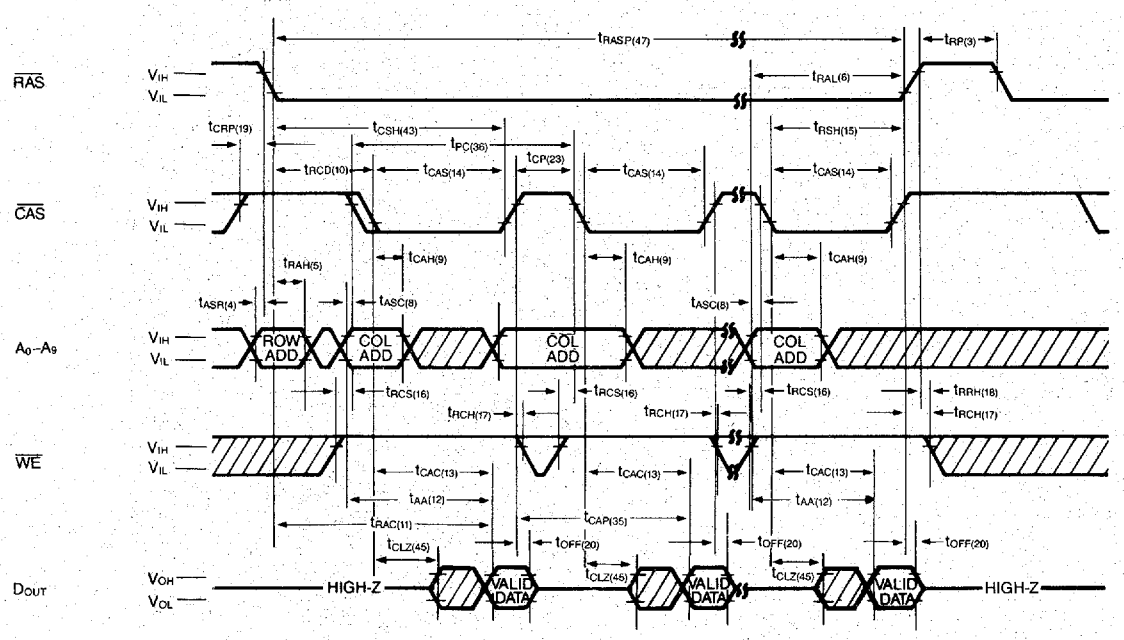
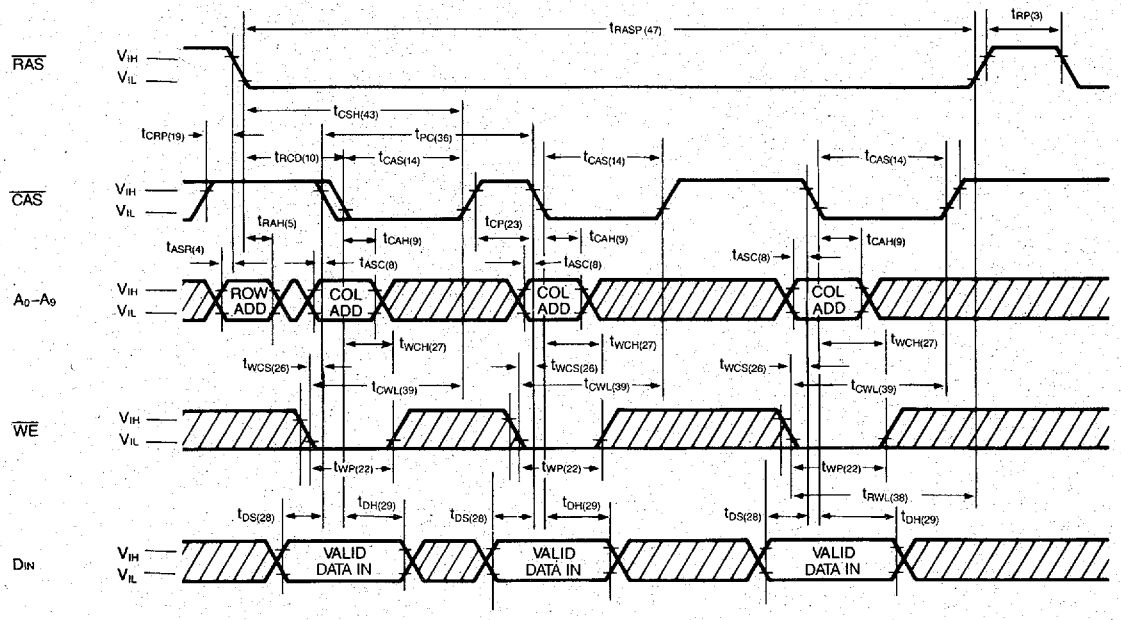
FAST PAGE MODE READ CYCLE



FAST PAGE MODE EARLY WRITE CYCLE



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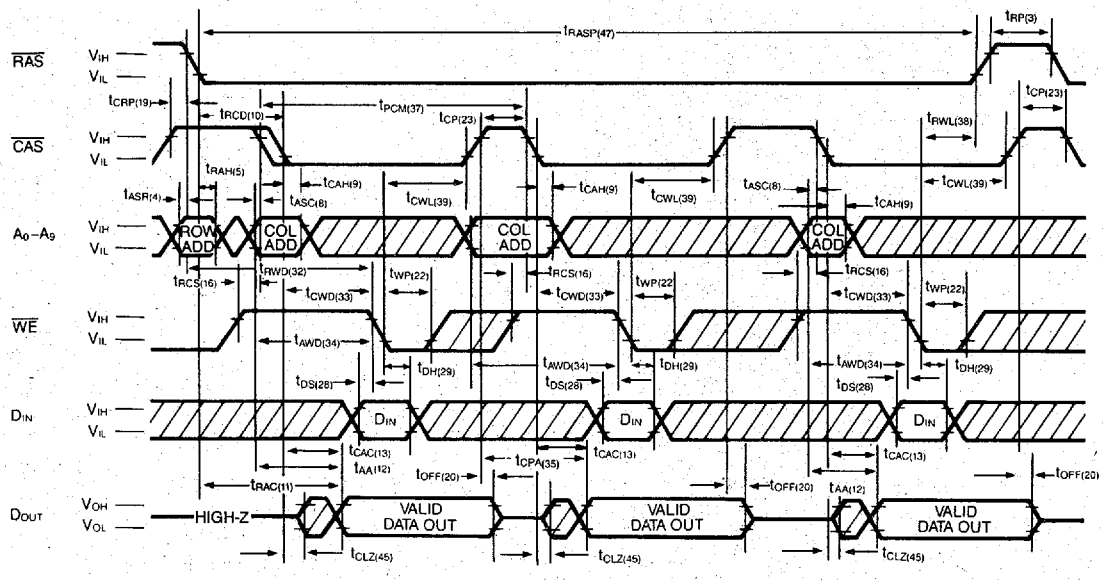
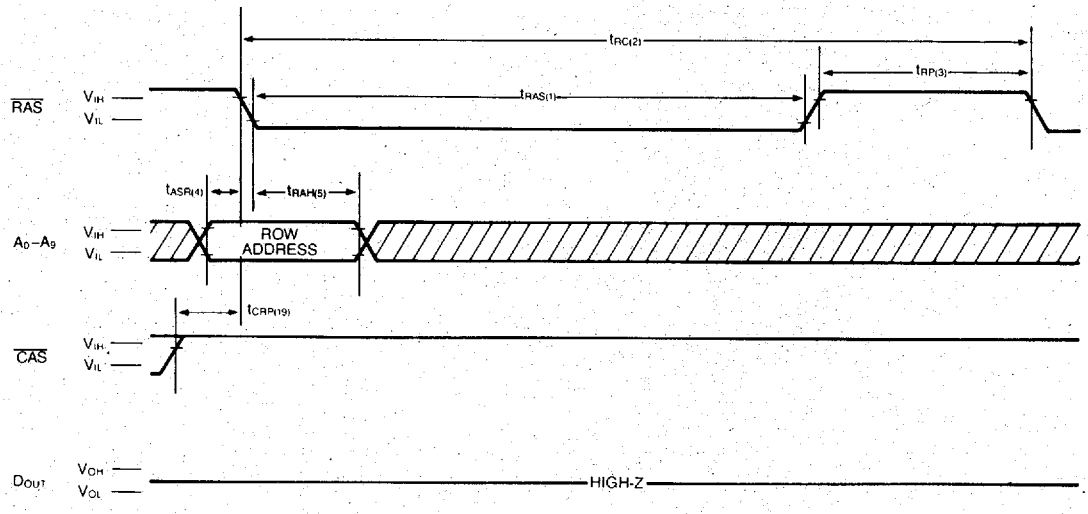
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



RAS-ONLY REFRESH CYCLE



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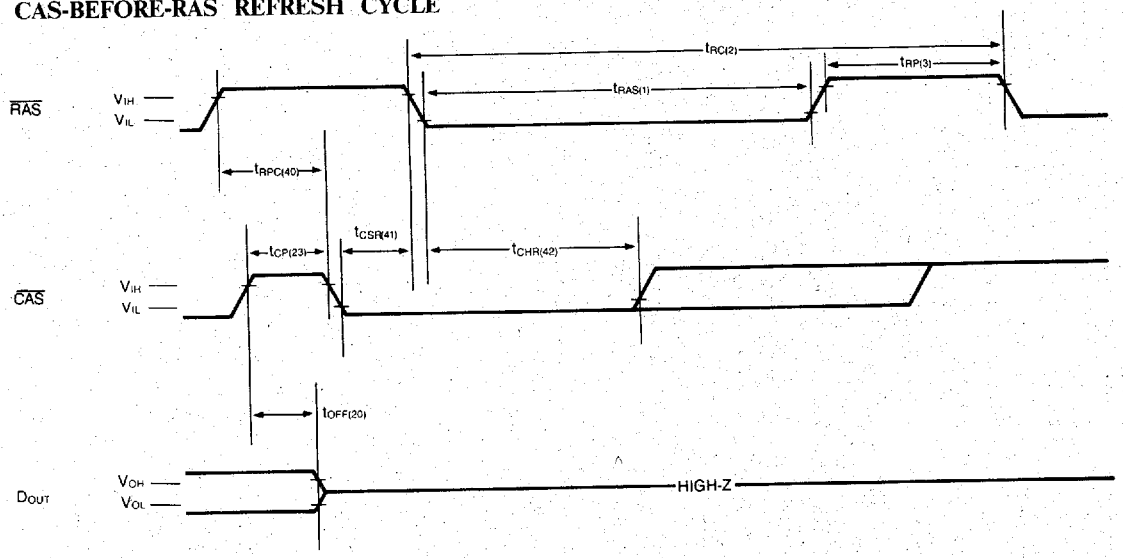
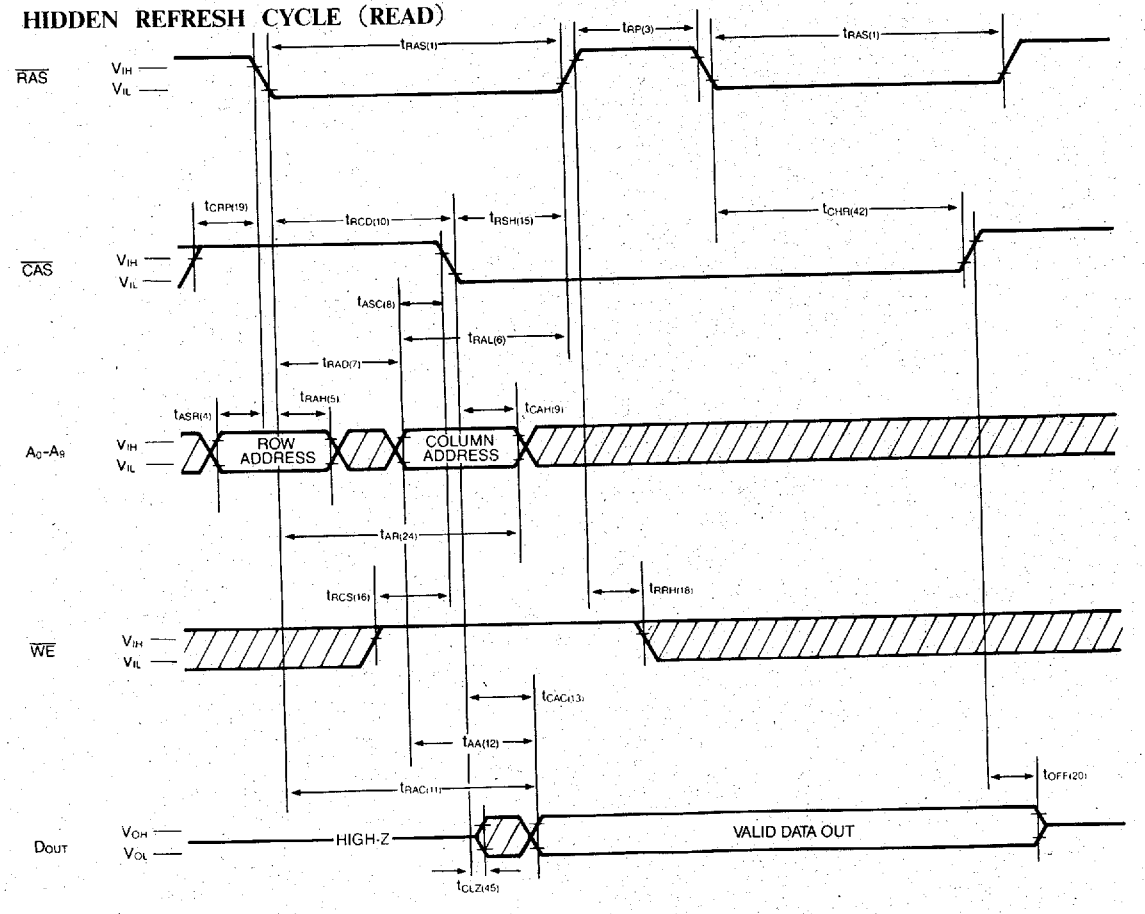
CAS-BEFORE-RAS REFRESH CYCLE



Note: $\overline{WE}$, A_0–A_8 = Don't care

HIDDEN REFRESH CYCLE (READ)



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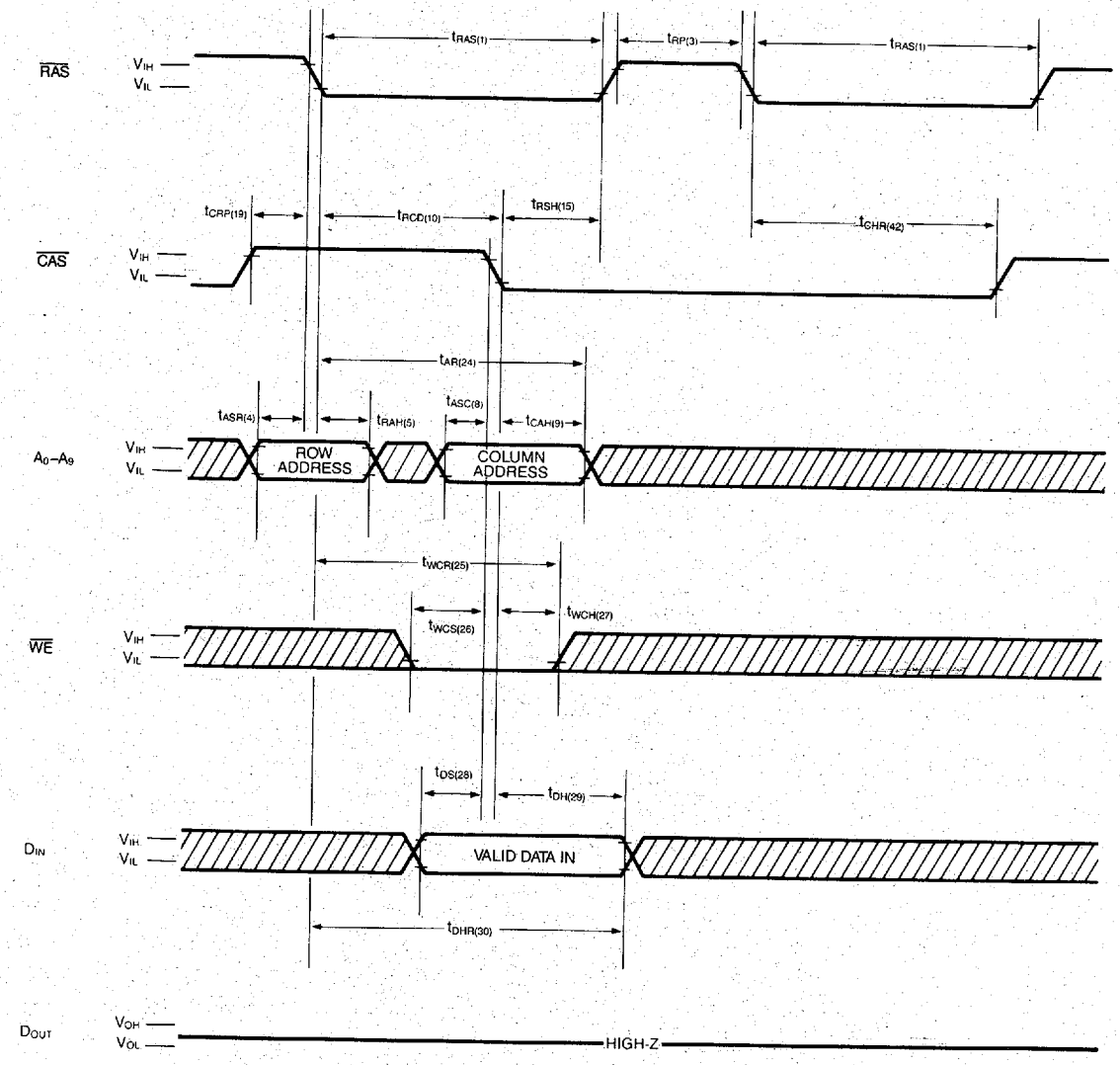
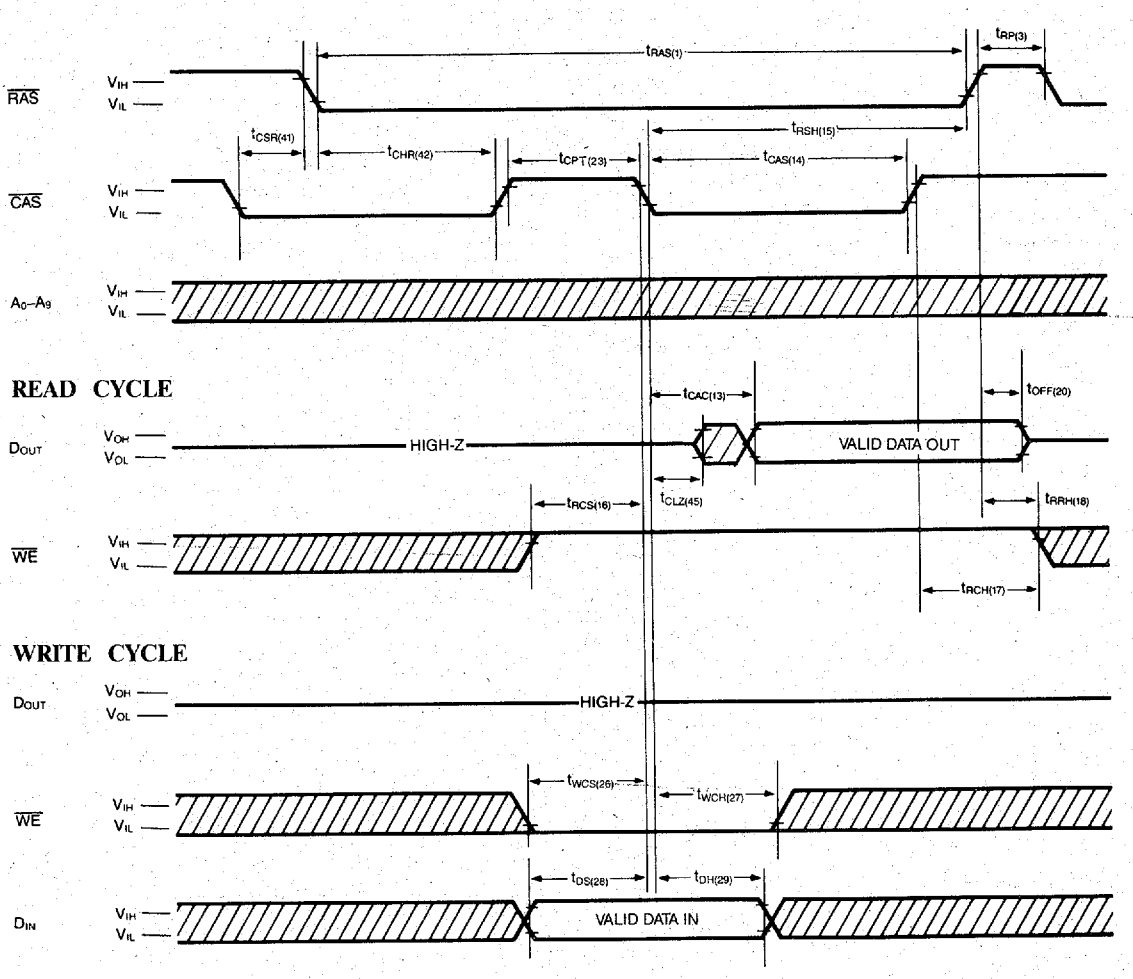
HIDDEN REFRESH CYCLE (WRITE)



CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



FUNCTIONAL DESCRIPTION

The HY531000 is a CMOS dynamic RAM optimized for high data bandwidth and low power applications. The functionality is similar to a traditional dynamic RAM. The HY531000 reads and writes data by multiplexing 20 bit address into 10 bit row and 10 bit column address. The row address is latched by Row Address Strobe ($\overline{RAS}$). The column address, however, flows through the internal address buffer and is latched by the Column Address Strobe ($\overline{CAS}$). Because access time is primarily dependent on a valid column address, the delay time between $\overline{RAS}$ and $\overline{CAS}$ can be long without affecting the access time.

MEMORY CYCLE

The memory cycle is initiated by bringing $\overline{RAS}$ low. Any memory cycle once initiated must not be ended or aborted prior to fulfilling the minimum t_{RAS} timing specification. This ensures proper device operation and data integrity. Additionally, a new cycle can not be initiated until the minimum precharge time t_{RP}/t_{CP} has elapsed.

READ CYCLE

A read cycle is performed by holding the Write Enable($\overline{WE}$) signal high during a $\overline{RAS}$ /$\overline{CAS}$ operation. The column address must be held for a minimum time specified by t_{AR}. Data output becomes valid only when t_{RAC}, t_{CAC}, and t_{AA} are all satisfied. Consequently, the access time is dependent upon the timing relationship among the t_{RAC}, t_{CAC} and t_{AA}. For example, the access time is limited by t_{AA} when t_{RAC} and t_{CAC} are both satisfied.

WRITE CYCLE

A write cycle is performed by taking $\overline{WE}$ and $\overline{CAS}$ low during a $\overline{RAS}$ operation. The column address is latched by $\overline{CAS}$. The write can be $\overline{WE}$ controlled or $\overline{CAS}$ controlled depending upon the latter of $\overline{WE}$ or $\overline{CAS}$ low transition. Consequently, the input data must be valid at or before the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. In a $\overline{CAS}$ controlled write cycle (the leading edge of $\overline{WE}$ occurs priors to or coincident with the $\overline{CAS}$ low transition)the output(D_{OUT}) pin will be in the high impedance state at the beginning of the write function.

Terminating the write action with $\overline{RAS}$ or $\overline{CAS}$ going high will maintain the data output (D_{OUT}) in the high impedance state.

REFRESH CYCLE

To retain data, 512 $\overline{RAS}$ refresh cycles are required in an 8 ms period. The refresh operation can be performed two ways :

1. Clocking each of 512 row address(A_0 through A_8) with $\overline{RAS}$ at least every 8 ms period. Any combination of $\overline{RAS}$ cycle such as read, write, read-modify-write, or $\overline{RAS}$-only refresh cycle will perform a refresh on the selected row.
2. $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle : If $\overline{CAS}$ go low prior to $\overline{RAS}$ go low, the chip enters a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle. In $\overline{CAS}$ -before-$\overline{RAS}$ refresh cycle the HY531000 will use an internal nine-bit counter output as the source of the row address and will ignore the external address input.

This $\overline{CAS}$-before-$\overline{RAS}$ refresh mode is a refresh only mode and no data access is allowed. Also, The $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle does not cause device selection and the state of the data output pin will remain in a high impedance state.

In order to guarantee the reliable operation of the $\overline{CAS}$-before-$\overline{RAS}$ refresh mode, a internal counter test mode is provided. The user can use the counter test mode to write in a data pattern consecutively(512 write cycles) and then verify the data which has been written by 512 consecutive read cycles.

The HY531000 offers a CMOS standby mode that is entered by causing the $\overline{RAS}$ clock to swing between a valid V_{IL} and an "extra high" V_{IH} within 0.2V of V_{DD}. While the $\overline{RAS}$ clock is at the "extra high" level, the HY531000 power consumption is reduced to the low I_{DDS} level. Overall I_{DD} consumption when operating

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in this mode can be calculated as follows :

$$I = \frac{(t_{RC}) \times (I \text{ active}) + (t_{RX} - t_{RC}) \times (I_{DDS})}{t_{RX}}$$

Where t_{RC} = Refresh Cycle Time
t_{RX} = Refresh Interval/512

FAST PAGE MODE OPERATION

Fast page mode operation permits all 1024 columns within a selected row of the device to be randomly accessed at a high data rate. Maintaining $\overline{RAS}$ low while sucessive $\overline{CAS}$ cycles are performed retains the row address internally, eliminating the need to reapply it. The column address buffer acts as a transparent or flow through latch while $\overline{CAS}$ is high. Access begins from the valid column address rather than from $\overline{CAS}$, eliminating t_{ASC} and t_T from the critical timing path. $\overline{CAS}$ latch the address into column address buffer and acts as an output enable.

During this operation, read, write, and read-modify-write, or read-write-read cycles are possible at random or sequential address within a row. Following the entry cycle into fast page mode, access time is t_{AA} or t_{CAP} dependent. If the column address is valid prior to or coincident by t_{CAP} as shown in figure 1. If the column address is valid after the rising edge of $\overline{CAS}$, then the access time is determined by the valid column address specified by t_{AA}. For both cases, the falling edge of $\overline{CAS}$ latches the address and enable the output.

Fast page mode provides a sustained data rate over 25 MHz for applications that require high data rates, such as bit mapped graphics or high speed signal processing. The following equation can be used to calculate the data rate :

$$\text{Data Rate} = \frac{1024}{t_{RC} + 1023 \times t_{PC}}$$

DATA RETENTION MODE

The HY531000 data output (D_{OUT}), which has tri-state capability, is controlled by $\overline{CAS}$. During a $\overline{CAS}$ the high state ($\overline{CAS}$ at V_{IH}), the data output is in the high impedance state. The following table summarize the D_{OUT} state for various types of cycles.

CYCLE	D_{OUT} STATE
Read Cycle	Data from Addressed Memory Cell
$\overline{CAS}$ Controlled Write Cycle (Early Write)	High Impedance
$\overline{WE}$ Controlled Write Cycle (Late Write)	Active, Not Valid
Read-Modify-Write Cycle	Data from Addressed Memory Cell
Fast Page Mode Read Cycle	Data from Addressed Memory Cell
Fast Page Mode Write Cycle (Early Write)	High Impedance
Fast Page Mode Read-Modify-Write Cycle	Data from Addressed Memory Cell
$\overline{RAS}$-Only Refresh Cycle	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle	Data remain the previous cycle's state (high impedance or low impedance)
$\overline{CAS}$-Only Cycle	High Impedance

POWER ON

An initial pause of 200 μs is required after the application of V_{DD} power supply, followed by a minimum of eight initialization cycles(any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh cycle). Eight initialization cycles are required after extended periods of bias without clocks(greater than the refresh interval).

The V_{DD} current (I_{DD}) requirement of the HY531000 during power on is dependent upon the input levels of $\overline{RAS}$ and $\overline{CAS}$. If $\overline{RAS} = V_{SS}$ during power on, the device will go into an active and I_{DD} will exhibit large current transients. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{DD} or be held at a valid V_{IH} level during power on.

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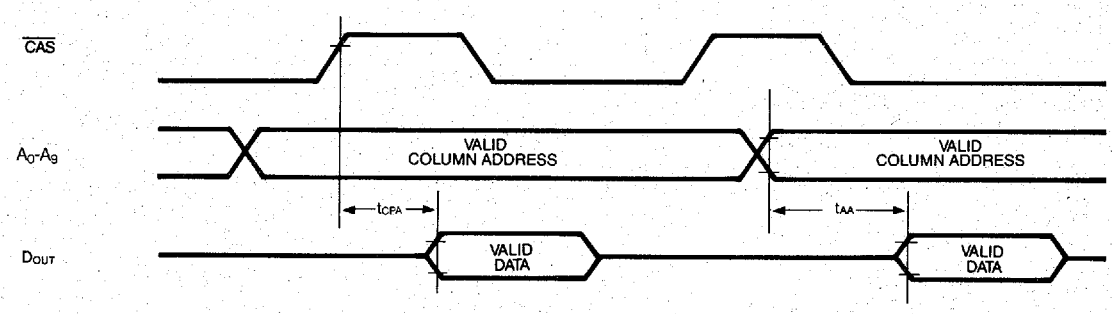
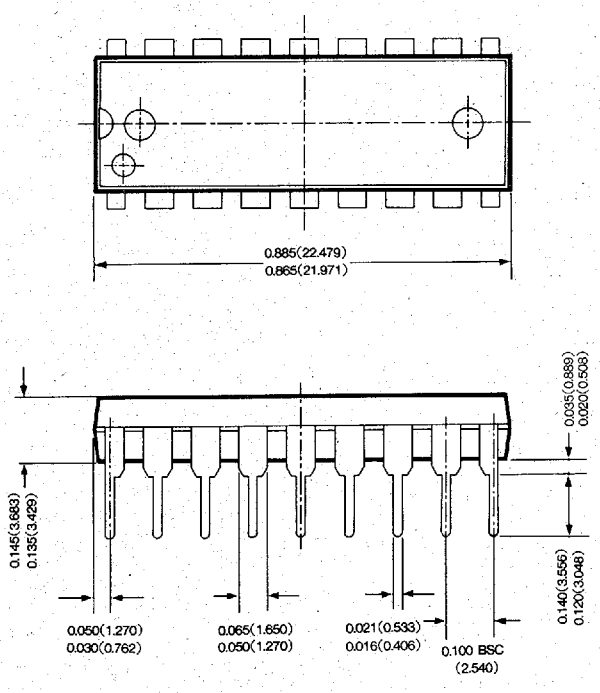
FIGURE 1. FAST PAGE MODE ACCESS TIME DETERMINATION

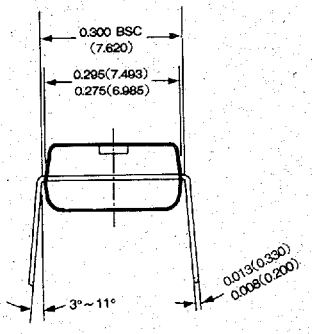


T-46-23-15

PACKAGE INFORMATION

- 18 PIN PLASTIC DUAL IN LINE PACKAGE – 300 MIL





- 20/26 PIN SMALL OUTLINE J-FORM PACKAGE –330 MIL