DESCRIPTION

The HY29F040 is a 4 Megabit, 5.0 Volts only Flash memory device organized as a 512k X 8 bits each. The HY29F040 is offered in an industry standard 32 pin package which is backward compatible to 1 Megabit and also pin compatible to EEPROMs. The device is offered in PDIP and TSOP packages. The device is designed to be programmed and erased in system with the standard system 5.0 Volt Vcc supply. 12.0 Volts Vpp is not required for program and erase operation. The device can also be reprogrammed in standard EPROM programmers.

The HY29F040 offers access times between 70 to 150 ns, allowing operation of high-speed microprocessors without wait-state. The device has separate chip enable ($\overline{CE}$), write enable ($\overline{WE}$) and output enable ($\overline{OE}$) controls to eliminate bus contention.

HEI flash memory technology reliably stores memory information even after 100,000 erase and program cycles. The HEI proprietary cell technology enhances the programming speeds and eliminates over erase problems seen in the classical ETOX^{TM} type of Flash cell technology and internal circuit design techniques give reduced internal electric fields and this gives improved reliability and endurance.

The HY29F040 is entirely pin and command set compatible to the JEDEC standard 4 Megabit EEPROM. The commands are written to the Command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from 12.0 V Flash or EPROM devices.

The HY29F040 is programmed by executing the program command sequence. This will start the internal programming algorithm that automatically times the program pulse width and also verifies the proper cell margin. Erase is accomplished by executing the erase command sequence. This will start the internal erasing algorithm that automatically times the erase pulse width and also verifies the proper cell margin. No preprogramming is necessary in HEI flash technology.

The device also features a sector erase architecture. The HY29F040 is divided into 8 sectors of 64k bytes each. The sectors can be erased individually without affecting the data in other sectors or they can be erased in a random combination of groups. This multiple sector erase capability or full chip erase makes it very flexible to alter the data in HY29F040. To protect the data from accidental program and erase the device also has sector protect or multiple sector protect function.

The device features single 5 Volt power supply for read, program and erase operation. Internally generated and well regulated voltages are provided for the program and erase operation. A low Vcc detector inhibits write operations on the loss of power . The end of program or erase is detected by $\overline{Data}$ Polling of DQ7 or by the Toggle Bit feature on DQ6. Once the program or erase cycle has been successfully completed, the device internally resets to Read mode.

The HY29F040 memory electrically erases the entire chip or all bits within a sector simultaneously via Fowler-Nordheim tunneling. The bytes are programmed one byte at a time using hot electron injection mechanism.

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FEATURE

- **5.0 V ± 10% Write and Erase**
  - minimizes system level power requirement

- **Compatible with JEDEC-Standard Command**
  - uses same software commands as EEPROMs

- **Compatible with JEDEC-Standard Byte-Wide Pinouts**
  - 32 - pin PDIP
  - 32 - pin TSOP

- **Minimum 100,000 Write / Erase Cycles**

- **High Performance**
  - 70 ns maximum access time

- **Sector Erase Architecture**
  - 8 equal size sectors of 64K bytes each
  - any combination of sectors can be concurrently erased, also supports full chip erase

- **Internal Erase Algorithms**
  - automatically erases the chip or any sector

- **Internal Program Algorithms**
  - automatically writes and verifies data at specified address

- **Data Polling and Toggle Bit Feature for Detection of Program or Erase Cycle Completion**

- **Low Power Consumption**
  - 20 mA typical active read current
  - 30 mA typical write / erase current
  - 25 uA typical standby current

- **Low V_{CC} Write Inhibit ≤ 3.2 V**

- **Sector Protection**
  - hardware method disables any combination of sectors from write or erase operations

- **Suspend Erase / Resume**
  - Suspend the erase operation to allow a read data in another sector within the same device

PIN CONNECTION

TSOP

PDIP
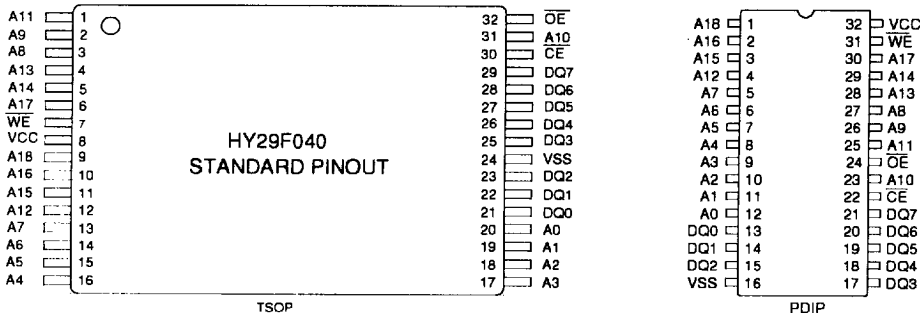
PIN DESCRIPTION

Pin	Function
A0 - A18	Address Inputs
DQ0 - DQ7	Data Input / Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{SS}	Device Ground
V_{CC}	Device Power Supply (5.0 V ± 10% or ± 5%)

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BLOCK DIAGRAM
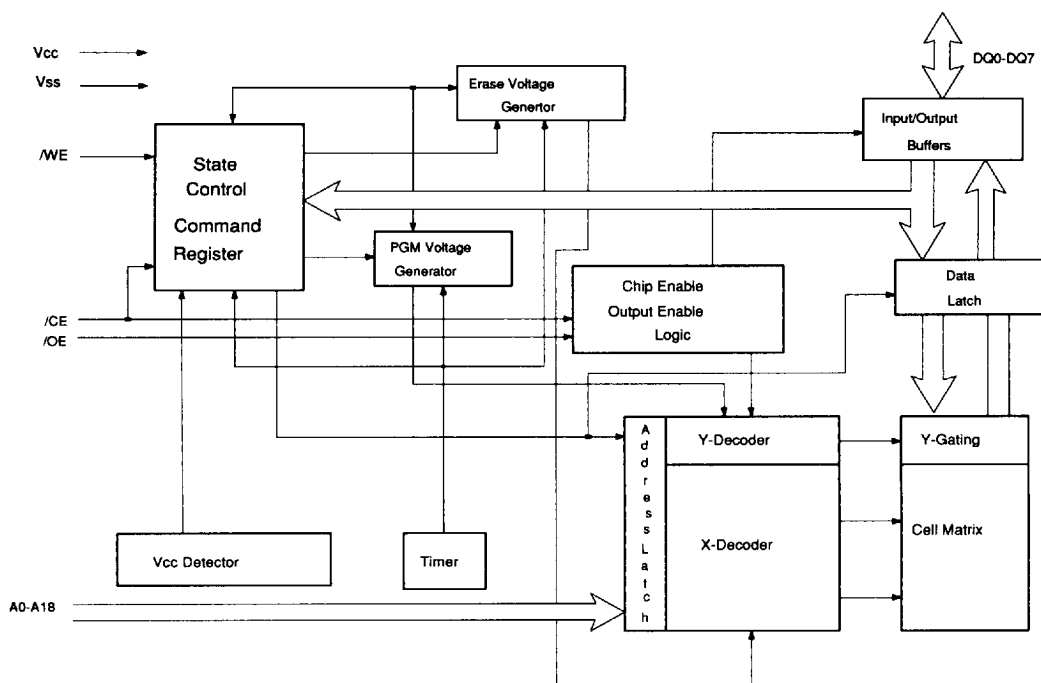
Table 1. Bus Operations

Operation	CE	OE	WE	A0	A1	A6	A9	I / O
Auto-select Manufacturer Code[1]	L	L	H	L	L	L	V_{ID}	Code
Auto-select Device Code[1]	L	L	H	H	L	L	V_{ID}	Code
Read[4]	L	L	H	A0	A1	A6	A9	D_{OUT}
Standby	H	x	x	x	x	x	x	High Z
Output Disable	L	H	H	x	x	x	x	High Z
Write	L	H	L	A0	A1	A6	A9	D_{IN}(2)
Enable Sector Protect	L	V_{ID}	L	x	x	x	V_{ID}	x
Verify Sector Protect[3]	L	L	H	L	H	L	V_{ID}	Code

$L = V_{IL}$, $H = V_{IH}$, x = Don't Care. See DC Characteristics for voltage levels.

Notes:
1. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Tables 2.
2. Refer to Table 4 for valid D_{IN} during a write operation.
3. Refer to the section on Sector Protection.
4. WE can be V_{IL} if CE is V_{IL}, OE at V_{IH} initiates the write operations.

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Table 2. Sector Protection Verify Autoselect Codes

Type	A18	A17	A16	A6	A1	A0	Code (HEX)	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Manufacturer Code	x	x	x	V_{IL}	V_{IL}	V_{IL}	ADH	1	0	1	0	1	1	0	1
HY29F040 Device Code	x	x	x	V_{IL}	V_{IL}	V_{IH}	40H	0	1	0	0	0	0	0	0
Sector Protection	Sector Addresses			V_{IL}	V_{IH}	V_{IL}	01H*	0	0	0	0	0	0	0	1

*Outputs 01H at Protected Sector addresses

Table 3. Sector Address Tables

	A18	A17	A16	Address Range
SA0	0	0	0	00000h - 0FFFFh
SA1	0	0	1	10000h - 1FFFFh
SA2	0	1	0	20000h - 2FFFFh
SA3	0	1	1	30000h - 3FFFFh
SA4	1	0	0	40000h - 4FFFFh
SA5	1	0	1	50000h - 5FFFFh
SA6	1	1	0	60000h - 6FFFFh
SA7	1	1	1	70000h - 7FFFFh

READ MODE

The HY29F040 has two control functions which must be satisfied in order to obtain data at the outputs. $\overline{CE}$ is the power control and should be used for device selection. $\overline{OE}$ is the output control and should be used to gate data to the output pins if a device is selected.

Address access time (t_{ACC}) is equal to the delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is the delay from stable addresses and stable $\overline{CE}$ to valid data at the output pins. The output enable access time is the delay from the falling edge of $\overline{OE}$ to valid data at the output pins (assuming the addresses have been stable for at least t_{ACC}-t_{OE} time).

Standby Mode

The HY29F040 has two standby modes, a CMOS standby mode ($\overline{CE}$ input held at $V_{CC} \pm 0.5$ V), when the current consumed is less than 100 µA ; and a TTL standby mode ($\overline{CE}$ is held at V_{IH}) when the current required is reduced to approximately 1 mA. In the standby mode the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

If the device is deselected during erasure or programming, the device will draw active current until the operation is completed.

Output Disable

With the $\overline{OE}$ input at a logic high level (V_{IH}), output from the device is disabled. This will cause the output pins to be in a high impedance state.

Autoselect

The autoselect mode allows the reading out of a binary code from the device and will identify its manufacturer and device type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the device.

To activate this mode, the programming equipment must force V_{ID} (11.5 V to 13.0 V) on address pin A9. Two identifier bytes may then be sequenced from the device outputs by toggling address A0 from V_{IL} to V_{IH}. All addresses are don't cares except A0, A1, and A6.

The manufacturer and device codes may also be read via the command register, for instances when the HY29F040 is erased or programmed in a system without access to high voltage on the A9 pin. The command sequence is illustrated in Table 4 (refer to Autoselect Command section).

Byte 0 (A0 = V_{IL}) represents the manufacturer's code (ADH for HEI) and byte 1 (A0 = V_{IH}) the device identifier code (40H for HY29F040). These two bytes are given in the Table 2. All identifiers for manufacturer and device will exhibit odd parity with the MSB (DQ7) defined as the parity bit, in order to read the proper device codes when executing the autoselect. A1 must be V_{IL} (see Table 2).

Table 4. Command Definitions

Command Sequence	Bus Write Cycles	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
Read / Reset	Req'd	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read / Reset	1	xxxH	F0H										
Read / Reset	4	5555H	AAH	2AAAH	55H	5555H	F0H	RA	RD				
Autoselect	4	5555H	AAH	2AAAH	55H	5555H	90H						
Byte program	4	5555H	AAH	2AAAH	55H	5555H	A0H	PA	Data				
Chip Erase	6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Sector Erase	6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	SA	30H
Sector Erase Suspend	Erase can be suspended during sector erase with Addr (don't care). Data(B0H)												
Sector Erase Resume	Erase can be resumed after suspend with Addr (don't care). Data(30H)												

Notes:
1. Address bits A15, A17, and A18 = x = Don't care. Write Sequences may be initiated with A15, A17, and A18 in either state.
2. Address bits A16, A17, and A18 = x = Don't care for all address commands except for Program Address(PA) and Sector Address(SA).
3. Bus Operations are defined in Table 1.
4. RA = Address of the memory location to be read.
   PA = Address of the memory location to be programmed. Addresses are latched on the falling edge of the $\overline{WE}$ pulse.
   SA = Address of the sector to be erased. The combination of A18, A17 ,A16 will uniquely select any sector.
5. RD = Data read from location RA during read operation.

WRITE MODE

Device erasure and programming are accomplished via the command register. The contents of the register serve as inputs to the internal state machine. Outputs of the state machine dictate the function of the device.

The command register itself does not occupy any addressable memory locations. The register is a latch used to

store the commands along with the addresses and data information needed to execute the command. The command register is written by bringing $\overline{WE}$ to V_{IL}, while $\overline{CE}$ is at V_{IL} and $\overline{OE}$ is at V_{IH}. Addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever happens later : while data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever happens first. Standard microprocessor write timings are used. Refer to AC Write Characteristics and the Erase / Programming Waveforms for specific timing parameters.

Command Definitions

Device operations are selected by writing specific address and data sequences into the Command register. Writing incorrect addresses and data values or writing them in the improper sequence will reset the device to read mode. Table 5 defines the valid register command sequences. Note that the Erase Suspend (B0) and Erase Resume (30) commands are valid only while the Sector Erase operation is in progress. Either of the two reset commands will reset the device (when applicable).

Read / Reset Command

The read or reset operation is initiated by writing the read / reset command sequence in to the command register. Processor read cycles retrieve the data from the memory. The device remains enable for reads until the command register contents are changed.

The device will automatically power-up in the read / reset mode. In this case, a command sequence is not needed to read the memory data. This default power-up to read mode ensures that no spurious changes of the data can take place during the power transitions. Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

Auto Select Command

Flash memories are intended for use in applications where the local CPU alters memory contents. As such, manufacture and device codes must be accessible while the device resides in the target system. PROM programmers typically access the signature codes by raising A9 to a high voltage. However, multiplexing high voltage on to the address lines is not generally desired system design practice.

The HY29F040 contains a command autoselect operation to supplement traditional PROM programming methodology. The operation is inititated by writing the autoselect command sequence into the command register. Following the command write, a read cycle from address XX00H retrieves manufacture code of ADH. A read cycle from address XX01H returns the device code 40H (see Table 2). All manufacturer and device codes will exhibit odd parity with the MSB (DQ7) defined as the parity bit.

Scanning the sector addresses (A16, A17, A18) while (A6, A1, A0)= (0, 1, 0) will produce a logical "1" at device output DQ0 for a protected sector. To terminate the operation, it is necessary to write the read / reset command sequence into the register.

Byte Write or Byte Program

The HY29F040 is programmed one byte at a time. Programming is a four bus cycle operation. There are two "unlock" write cycles. These are followed by program set-up command and data write cycles. Addresses are latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever happens later and data is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever happens first. The rising edge of $\overline{CE}$ or $\overline{WE}$ (whichever happens first) begins programming. Upon executing the Internal Program Algorithm command sequence the system is not required to provide further controls or timings. The device will automatically provide adequate internally generated program pulses and verify the programmed cell margin. The automatic programming operation is completed when the data on DQ7 is equivalent to data written to this bit (see Write Operation Status section) at which time the device returns to the read mode and addresses are no longer latched. Therefore, the device requires that a valid address to the device be supplied by the system at this particular instance of time. Hence, $\overline{Data}$ Polling must be performed at the memory location which is being programmed. Any commands written to the chip during this period will be ignored.

Programming is allowed in any sequence and across sector boundaries. Beware that a data "0" cannot be

4675088 0003848 538

programmed back to a "1". Attempting to do so will probably hang up the device, or perhaps result in an apparent success according to the data polling algorithm but a read from reset / read mode will show that the data is still "0". Only erase operations can convert "0"s to "1"s. Figure 1 illustrates the Internal Programming Algorithm using typical command strings and bus operations.

Chip Erase

Chip erase is a six bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command. Two more "unlock" write cycles are then followed by the chip erase command.

Chip erase does not require the user to program the device prior to erase.

The automatic erase begins on the rising edge of the last $\overline{WE}$ pulse in the command sequence and terminates when the data on DQ7 is "1" (see Write Operation Status section) at which time the device returns to read mode. Figure 2 illustrates the Internal Erase Algorithm using typical command strings and bus operations.

Sector Erase

Sector erase is a six bus cycle operation. There are two "unlock" write cycles followed by writing the sector erase set-up command. Two more "unlock" write cycles are then followed by the sector erase command. The sector address (any address location within the desired sector) is latched on the falling edge of $\overline{WE}$, while the command data is latched on the rising edge of $\overline{WE}$. A 100 uS time-out from the rising edge of the last sector erase command will initiate the sector erase commands. note : *Do not attempt to write an invalid command sequence during the sector erase operation. Otherwise, it will terminate the sector erase operation and the device will reset back into the read mode.*

Multiple sectors can be erased simultaneously by writing the six bus cycle operations as described above. This sequence is followed with writes of the Sector Erase command to addresses in other sectors desired to be simultaneously erased. The time between writes must be less than 100 uS (± 20%), otherwise that command will not be accepted. It is recommanded that processor interrupts be disabled during this time to guarantee this condition. The interrupts can be re-enabled after the last Sector Erase command is written. A time-out of 100 uS from the rising edge of the last $\overline{WE}$ will initiate the execution of the Sector Erase commands. If another falling edge of the $\overline{WE}$ occurs within the 100uS time-out window the timer is reset. Any command other than Sector Erase or Erase Suspend during this period and afterwards will reset the device to read mode ignoring the previous command string. Reseting the device after it has begun execution will result in the data of the operated sectors being undefined (messed up). In that case, restart the erase on those sectors and allow them to complete. (Refer to the Write Operation Status section for Sector Erase Timer operation.) Loading the sector erase buffer may be done in any sequence and with any number of sectors (1 to 8).

Sector erase does not require the user to program the sector before erase. When erasing a sector or multiple sectors the data in the unselected sectors remains unaffected. The system is not required to provide any controls or timings during these operations.

The automatic sector erase begins after the 100 uS time out from the rising edge of the $\overline{WE}$ pulse for the last sector erase command pulse and terminates when the data on DQ7 is " 1" (see Write Operation Status section) at which time the device returns to read mode. *During the execution of the Sector Erase command, only the Erase Suspend and Erase Resume commands are allowed. All other commands will reset the device to read mode.* $\overline{Data}$ Polling must be performed at an address within any of the sectors being erased. Figure 2 illustrates the Internal Erase Algorithm using typical command strings and bus operations.

Erase Suspend

Erase suspend command allows the user to interrupt the chip and then do data reads (not program) from a non-busy sector while it is in the middle of a Sector Erase operation (which may take up to several seconds). This command is applicable ONLY during the Sector Erase operation and will be ignored if written during the Chip Erase or Programming operation. The Erase Suspend command (B0) will be allowed only during the Sector Erase operation that will include the sector erase time-out period after the Sector Erase commands (30). Writing this

command during the time-out will result in immediate termination of the time-out period. Any subsequent writes of the Sector Erase command will be ignored as such, but instead will be taken as the Erase Resume command. Note that any other commands during the time-out will reset the device to the read mode. The addresses are don't-cares in writing the Erase Suspend or Erase Resume commands.

When the Erase Suspend command is written during a Sector Erase operation, the chip will take between 100 µS to 3 mS to suspend the erase operation and go into erase suspended read mode (pseudo-read mode), during which the user can read from a sector that is NOT being erased. A read from a sector being erased may result in invalid data. The user must monitor the toggle bit to determine if the chip has entered the pseudo-read mode, at which time the toggle bit stops toggling. An address of a sector NOT being erased must be used to read the toggle bit, otherwise the user may encounter information problems. Note that the user must keep track of what state the chip is in since there is no external indication of whether the chip is in pseudo-read mode or actual read mode. After the user writes the Erase Suspend command and waites until the toggle bit stops toggling, data reads from the device may then be performed. Any further writes of the Erase Suspend command at this time will be ignored.

Every time an Erase Suspend command followed by an Erase Resume command is written, the internal pulse counters are reset. These counters are used to count the number of high voltage pulses the memory cell requires to program or erase. If the count exceeds a certain limit, then the DQ5 bit will be set (Exceeded Time Limit flag). This reseting of the counters is necessary since the Erase Suspend command can potentially interrupt or disrupt the high voltage pulses.

To resume the operation of Sector Erase, the Resume command (30) should be written. Any further writes of the Resume command at this point will be ignored. Another Erase Suspend command can be written after the chip has resumed.

Sector Protection

The HY29F040 has a hardware sector protection. This feature will disable both Program and Erase operation to the protected sector. There are total 8 sectors in this device of 64K bytes each. The sector protect feature is enabled using programming equipment at the user's site. The device is shipped with all sectors unprotected.

To activate this mode, the user must force V_{ID} (suggest V_{ID}= 11V)on address pin A9 and control pin $\overline{OE}$, and $\overline{CE}$= V_{IH}. The sector addresses (A16, A17 and A18) should be set to the sector to be protected. Table 3 defines the sector address for each of the eight individual sectors. Programming of the protection circuitry starts on the falling edge of $\overline{WE}$ pulse and is terminated with the rising edge of the same. Sector addresses must be held fixed during the $\overline{WE}$ pulse.

To verify programming of the protection circuitry, the programming equipment must force V_{ID} on the address pin A9 with $\overline{CE}$ and $\overline{OE}$ at V_{IL} and $\overline{WE}$ at V_{IH} . Scanning the sector addresses (A16, A17 and A18) while (A6, A1 and A0) = (0, 1, 0) will produce a logical "1" code at device output DQ0 for a protected sector. Otherwise the device will read 00H for unprotected sector. In this mode, the lower order addresses, except for A0, A1 and A6 are don't care. Address locations with A1 = V_{IL} are reserved for Autoselect manufacturer and device codes.

It is also possible to determine if a sector is protected in the system by writing the Autoselect command. Performing a read operation at the address location XX02H, where the higher order addresses (A16, A17 and A18) are the sector address will produce a logical "1" at DQ0 for a protected sector. See Table 2 for Autoselect codes.

DATA FLAGS

Table 5. Hardware Sequence Flags

	Status	DQ7	DQ6	DQ5	DQ3	DQ2-DQ0
In Progress	Auto-Programming	DQ7	Toggle	0	0	
	Erasing in Auto-Erase	0	Toggle	0	1	(D̄)
Exceeded Time Limits	Auto-Programming	DQ7	Toggle	1	0	
	Erasing in Auto-Erase	0	Toggle	1	1	(D̄)

Notes : DQ0, DQ1, DQ2, DQ4 are reserve pins for future use.

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DQ7 Data Polling

The HY29F040 device features Data Polling as a method to indicate to the host that the Internal Algorithms are in progress or completed. During the Internal Program Algorithm an attempt to read the device will produce the compliment of the data last written to DQ7. Upon completion of the Internal Program Algorithm an attempt to read the device will produce the true data last written to DQ7. During the Internal Erase Algorithm, an attempt to read the device will produce a "0" at the DQ7 output. Upon completion of the Internal Erase Algorithm an attempt to read the device will produce a "1" at the DQ7 output. The flowchart for Data Polling (DQ7) is shown in Figure 3.

For chip erase, the Data Polling is valid after the rising edge of the sixth $\overline{WE}$ pulse in the six write pulse sequence. For sector erase, the Data Polling is valid after the last rising edge of the sector erase $\overline{WE}$ pulse. Data Polling must be performed at sector address within any of the sectors being erased and not a protected sector. Otherwise, the status may not be valid. Once the Internal Algorithm operation is close to being completed, the HY29F040 data pins (DQ7) may change asynchronously while the output enable ($\overline{OE}$) is asserted low. This means that the device is driving status information on DQ7 at one instant of time and then that byte's valid data at the next instant of time. Depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device has completed the Internal Algorithm operation and DQ7 has a valid data, the data outputs on DQ0 - DQ6 may be still invalid. The valid data on DQ0 - DQ7 will be read on the successive read attempts.

The Data Polling feature is only active during the Internal Programming Algorithm, Internal Erase Algorithm or sector erase time-out (see Table 6).

DQ6 Toggle Bit

The HY29F040 also features the "Toggle Bit" as a method to indicate to the host system that the Internal Algorithms are in progress or completed.

During an Internal Program or Erase Algorithm cycle, successive attempts to read ($\overline{OE}$ toggling) data from the device will result in DQ6 toggling between one and zero. Once the Internal Program or Erase Algorithm cycle is completed, DQ6 will stop toggling and valid data will be read on the next successive attempts. During programming, the Toggle Bit is valid after the rising edge of the fourth $\overline{WE}$ pulse in the four write pulse sequence. For chip erase, the Toggle Bit is valid after the rising edge of the sixth $\overline{WE}$ pulse in the six write pulse sequence. For Sector erase, the Toggle Bit is valid after the last rising edge of the sector erase $\overline{WE}$ pulse. The Toggle Bit is active during the sector time-out.

In programming, if the sector being written to is protected, the toggle bit will toggle for about 20 μS and then stop toggling without the data having changed. In erase, the device will erase all the selected sectors except for the ones that are protected. If all selected sectors are protected, the chip will toggle the toggle bit for about 3 mS and then drop back into read mode, having changed none of the data. Either $\overline{CE}$ or $\overline{OE}$ toggling will cause the DQ6 to toggle. The flowchart for Toggle Bit (DQ6) is shown in Figure 4.

DQ5 Exceeded Timing Limits

DQ5 will indicate if the program or erase time has exceeded the specified limits (internal pulse count). Under these conditions DQ5 will produce a "1". This is a failure condition which indicates that the program or erase cycle was not successfully completed. Data Polling is the only operating function of the device under this condition. The $\overline{CE}$ circuit will partially power down the device under these conditions (to approximately 2 mA). The $\overline{OE}$ and $\overline{WE}$ pins will control the output disable functions as described in Table 2.

If this failure condition occurs during sector erase operation, it specifies that a particular sector is bad and it may not be reused, however, other sectors are still fucntional and may not be used for the program or erase operation. The device must be reset to use other sectors. Write the Reset command sequence to the device, and then execute the program or erase command sequence. This allows the system to continue to use the other active sectors in the device.

If this failure condition occurs during the chip erase operation, it specifies that the entire chip is bad or combination of sectors are bad. In which case, the chip should not be reused.

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If this failure condition occurs during the byte programming operation, it specifies that the entire sector containing that byte is bad and this sector may not be reused (other sectors are still functional and can be reused).

The DQ5 failure condition may also appear if a user tries to program a non blank location without erasing. In this case the device locks out and never completes the Internal Algorithm operation. Hence, the system never reads a valid data on DQ7 bit and DQ6 never stops toggling. Once the device has exceeded timing limits, the DQ5 bit will indicate a "1". Please note that this is not a device failure condition since the device was incorrectly used.

DQ3 Sector Erase Timer

After the completion of the initial sector erase command sequence the sector erase time-out will begin. DQ3 will remain low until the time-out is complete. Data Polling and Toggle Bit are valid after the initial sector erase command sequence.

If Data Polling or the Toggle Bit indicates the device has been written with a valid erase command. DQ3 may be used to determine if the sector erase timer window is still open. If DQ3 is high ("1") the internally controlled erase cycle has begun : Attempts to write subsequent command to the device will be ignored until the erase operation is completed as indicated by Data Polling or Toggle Bit. If DQ3 is low ("0"), the device will accept additional sector erase commands. To insure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 were high on the second status check, the command may not have been accepted. Refer to Table 5 : Hardware Sequence Flags.

Data Protection

The HY29F040 is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transitions. During power up the device automatically resets the internal status machine in the Read mode. Also, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific multi-bus cycle command sequences. The device also incorporates several features to prevent inadvertent write cycles resulting from Vcc power-up and power-down transitions or system noise. ·

Low Vcc Write Inhibit

To avoid initiation of a write cycle during Vcc power-up and power-down, a write cycle is locked out for Vcc less than 3.2 V (typically 3.7 V). If Vcc < V$_{LKO}$, the command register is disabled and all internal program / erase circuits are disabled. Under this condition the device will reset to the read mode. Subsequent writes will be ignored until the Vcc level is greater than V$_{LKO}$. It is the users responsibility to insure that the control pins are logically correct to prevent unintentional writes when Vcc is above 3.2 V.

Write Pulse "Glitch" Protection

Noise pulses of less than 5 ns (typical) on $\overline{OE}$, $\overline{CE}$ or $\overline{WE}$ will not initiate a write cycle.

Logical Inhibit

Writing is inhibited by holding any one of $\overline{OE}$ = V$_{IL}$, $\overline{CE}$ = V$_{IH}$ or $\overline{WE}$ = V$_{IH}$. To initiate a write cycle $\overline{CE}$ and $\overline{WE}$ must be a logical zero while $\overline{OE}$ is a logical one.

Power -Up Write Inhibit

Power-up of the device with $\overline{WE}$ = $\overline{CE}$ = V$_{IL}$ and $\overline{OE}$ = V$_{IH}$ will not accept commands on the rising edge of $\overline{WE}$. The internal state machine is automatically reset to the read mode on power-up.

Sector Protect

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Sectors of the HY29F040 may be hardware protected at the users factory. The protection circuitry will disable both program and erase functions for the protected sectors. Requests to program or erase a protected sector will be ignored by the device.

SECTOR PROTECTION ALGORITHMS

Sector Protection

The HY29F040 features hardware sector protection which will disable both program and erase operations to an individual sector or any group of sectors. To activate this mode, the programming equipment must force V_{ID} on control pin $\overline{OE}$ and address pin A9. The sector addresses should be set using higher address lines A18, A17 and A16. The protection mechanism begins on the falling edge of the $\overline{WE}$ pulse and is terminated with the rising edge of the same.

It is also possible to verify if a sector is protected during the sector protection operation. This is done by setting A6 = $\overline{CE}$ = $\overline{OE}$ = V_{IL} and $\overline{WE}$ = V_{IH} (A9 remains high at V_{ID}). Reading the device at address location XXX2H, where the higher order addresses (A18, A17, and A16) define a particular sector, will produce 01H at data outputs (DQ0 - DQ7) for a protected sector.

Sector Unprotect

The HY29F040 also features a sector unprotect mode, so that a protected sector may be unprotected to incorporate any changes in the code. All sectors should be protected prior to unprotecting any sector.

To activate this mode, the programming equipment must force V_{ID} on control pins $\overline{OE}$, $\overline{CE}$ and address pin A9. The address pins A6, A16 and A12 should be set to V_{IH}. The unprotection mechanism begins on the falling edge of the $\overline{WE}$ pulse and is terminated with the rising edge of the same.

It is also possible to determine if a sector is unprotected in the system by writing the autoselect command and A6 is set at V_{IH}. Performing a read operation at address location XXX2H, where the higher order addresses (A18, A17 and A16) define a particular sector address, will produce 00H at data outputs (DQ0 - DQ7) for an unprotected sector.

■ 4675088 0003853 9T5 ■

INTERNAL PROGRAMMING ALGORITHM

Program Command Sequence (Address/Command)

5555H/AAH

2AAAH/55H

5555H/A0H

Program Address/Program Data
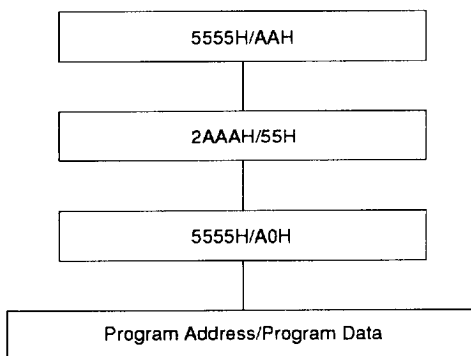
Figure 1. Internal Programming Algorithm

Table 6. Internal Programming Algorithm

Bus Operation	Command Sequence	Comments
Standby[1]		
Write	Program	Valid Address / Data Sequence
Read		Data Polling to Verify Programming
Standby[1]		Compare Data Output to Data Expected

Note :
1. Device is either powered-down, erase inhibit or program inhibit.

■ 4675088 0003854 831 ■

INTERNAL ERASE ALGORITHM

```
                        ┌─────────────────┐
                        │      START      │
                        └─────────────────┘
                                 │
              ┌──────────────────────────────────────┐
              │     Write Erase Command Sequence     │
              │             (See Below)              │
              └──────────────────────────────────────┘
                                 │
              ┌──────────────────────────────────────┐
              │      Data Polling or Toggle Bit      │
              │        Successfully Completed        │
              └──────────────────────────────────────┘
                                 │
                                 ▼
                 ┌──────────────────────────────┐
                 │      Erasure Completed        │
                 └──────────────────────────────┘
```

Chip Erase Command Sequence
(Address / Command) :

```
┌──────────────────┐
│    5555H/AAH     │
└──────────────────┘
┌──────────────────┐
│   2AAAH/55H      │
└──────────────────┘
┌──────────────────┐
│    5555H/80H     │
└──────────────────┘
┌──────────────────┐
│    5555H/AAH     │
└──────────────────┘
┌──────────────────┐
│   2AAAH/55H      │
└──────────────────┘
┌──────────────────┐
│    5555H/10H     │
└──────────────────┘
```

Individual Sector / Multiple Sector
Erase Command Sequence
(Address / Command) :

```
┌──────────────────┐
│    5555H/AAH     │
└──────────────────┘
┌──────────────────┐
│   2AAAH/55H      │
└──────────────────┘
┌──────────────────┐
│    5555H/80H     │
└──────────────────┘
┌──────────────────┐
│    5555H/AAH     │
└──────────────────┘
┌──────────────────┐
│   2AAAH/55H      │
└──────────────────┘
┌──────────────────┐
│ Sector Address /30H │
└──────────────────┘
┌──────────────────┐     ┐
│ Sector Address /30H │     │ Additional sector
└──────────────────┘     ├ erase commands
         ⋮               │ are optional
┌──────────────────┐     ┘
│ Sector Address /30H │
└──────────────────┘
```

Figure 2. Internal   Erase   Algorithm

Table 7. Internal Erase Algorithm

Bus Operations	Command Sequence	Comments
Standby		
Write	Erase	
Read		Data Polling to Verify Erasure
Standby		Compare Output to FFH

DATA POLLING ALGORITHM

VA=Byte address for programming
　=Any of the sector addresses within the
　　sector being erased during sector erase
　　operation
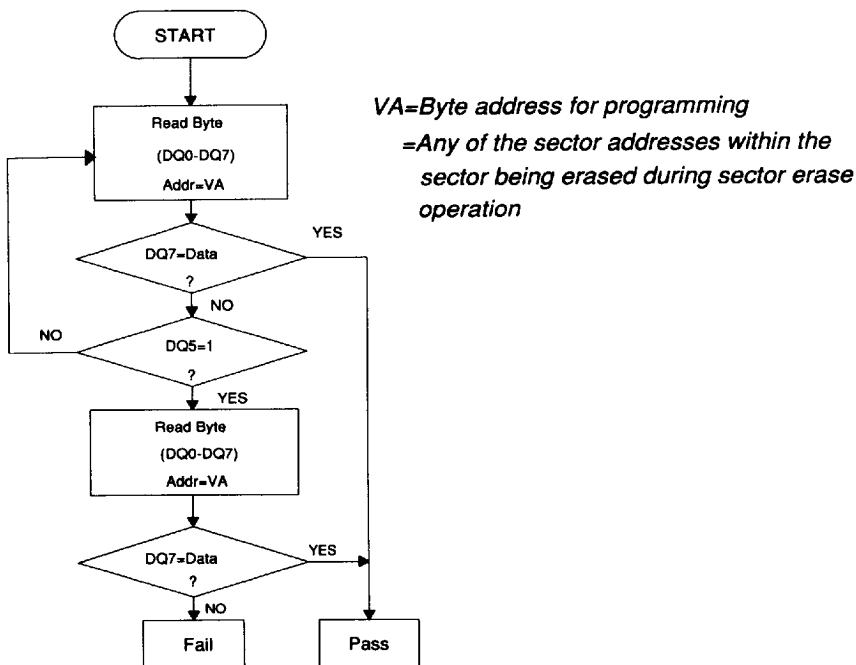
Note :
1. DQ7 is rechecked even if DQ5 = "1" because DQ7 may change simultaneously with DQ5.

Figure　3 . Data Polling Algorithm

■ 4675088 0003856 604 ■

TOGGLE BIT ALGORITHM

VA = Byte address for programming
   = any of the sector addresses within the
     sector being erased during sector erase
     operation
   = XXXXH during chip erase
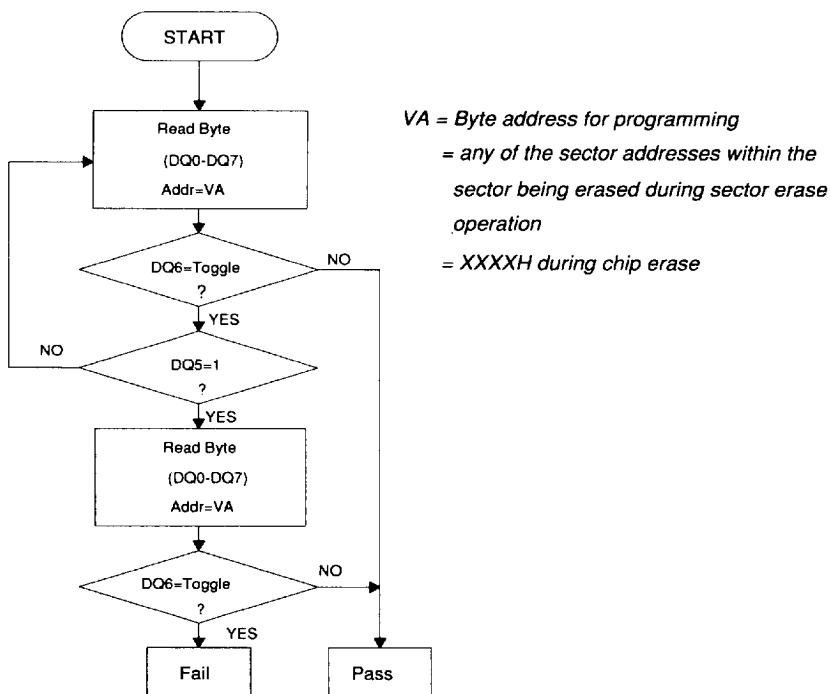
Note :
1. DQ6 is rechecked even if DQ5 = "1" because DQ6 may stop toggling at the same time as DQ5 changes to "1".

Figure 4. Toggle Bit Algorithm

4675088 0003857 540

SECTOR PROTECTION ALGORITHM

```
                          ┌─────────────┐
                          │    START     │
                          └──────┬──────┘
                                 ▼
                     ┌───────────────────────┐
                     │   Set Up Sector Addr.  │◄──────────┐
                     │    (A18,A17,A16)       │           │
                     └───────────┬───────────┘           │
                                 ▼                        │
                     ┌───────────────────────┐           │
                     │      PLSCNT = 1        │           │
                     └───────────┬───────────┘           │
                                 ▼                        │
                     ┌───────────────────────┐           │
          ┌──────────│    OE=Vid, A9=Vid      │           │
          │          └───────────┬───────────┘           │
          │                      ▼                        │
          │          ┌───────────────────────┐           │
          │          │    Activate WE Pulse    │           │
          │          └───────────┬───────────┘           │
          │                      ▼                        │
          │          ┌───────────────────────┐           │
          │          │     Time Out 100us      │           │
          │          └───────────┬───────────┘           │
          │                      ▼                        │
          │          ┌───────────────────────┐           │
 ┌────────┴────────┐ │     Power Down OE       │           │
 │ Increment PLSCNT │ │       WE = Vih          │           │
 └────────┬────────┘ │     CE = OE = Vil       │           │
          │          │   A9 shoud remain Vid   │           │
          │          └───────────┬───────────┘           │
          │                      ▼                        │
          │          ┌───────────────────────┐           │
          │          │     Read from Sector    │           │
          │          │    Addr=SA. A1A0=10,    │           │
          │          │        A6=0             │           │
          │          └───────────┬───────────┘           │
          │   NO                 ▼                        │
     ┌────┴─────┐      NO  ┌─────────────┐                │
     │ PLSCNT=25 │◄────────│   Data=01H   │                │
     │    ?      │         │      ?       │                │
     └────┬─────┘         └──────┬──────┘                │
          │ YES                  │ YES                    │
          ▼                      ▼                        │
  ┌──────────────┐       ┌─────────────┐   YES            │
  │ Device Failed │       │   Protect    │──────────────────┘
  └──────────────┘       │   Another    │
                          │   Sector?    │
                          └──────┬──────┘
                                 │ NO
                                 ▼
                     ┌───────────────────────┐
                     │   Remove Vid from A9    │
                     │   Write Reset Command   │
                     └───────────┬───────────┘
                                 ▼
                     ┌───────────────────────┐
                     │ Sector Protection Complete │
                     └───────────────────────┘
```
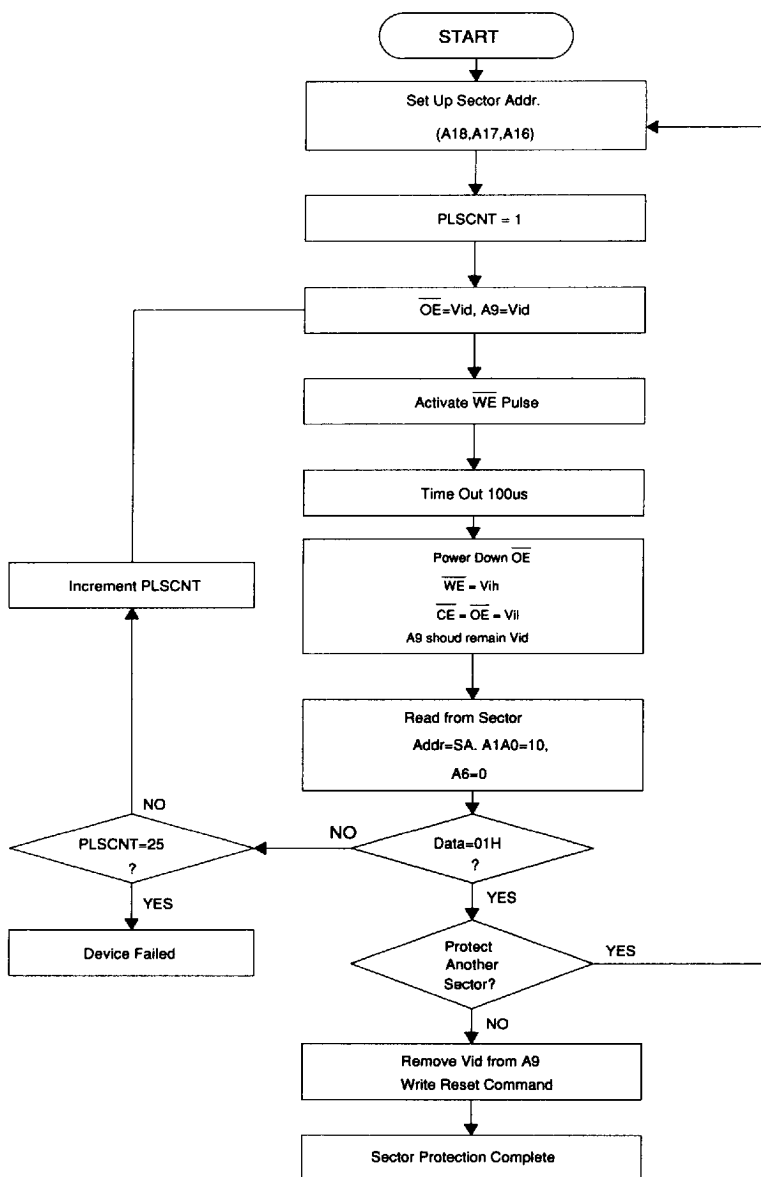
Figure 5. Sector Protection Algorithm

SECTOR UNPROTECT ALGORITHM

```
                              ┌──────────┐
                              │  START   │
                              └────┬─────┘
                                   │
                         ┌─────────▼─────────┐
                         │ Protect All Sectors│
                         └─────────┬─────────┘
                                   │
                         ┌─────────▼─────────┐
                         │    PLSCNT = 1     │
                         └─────────┬─────────┘
                                   │
                         ┌─────────▼─────────┐
                         │  Set Up Sector    │
                         │  Unprotect Mode   │◄──────────────┐
                         │  A6 = A12 = A16 = Vih│             │
                         └─────────┬─────────┘               │
                                   │                ┌────────┴────────┐
                         ┌─────────▼─────────┐      │ Increment PLSCNT│
                         │ Set OE = CE = A9 = Vld│  └────────▲────────┘
                         └─────────┬─────────┘               │
                                   │                         │
                         ┌─────────▼─────────┐               │
                         │ Activate WE Pulse │               │
                         └─────────┬─────────┘               │
                                   │                         │
                         ┌─────────▼─────────┐               │
                         │  Time Out 10ms    │               │
                         └─────────┬─────────┘               │
                                   │                         │
                         ┌─────────▼─────────┐               │
                         │ Set OE=CE=Vll, A9=Vld│            │
                         └─────────┬─────────┘               │
                                   │                         │
                         ┌─────────▼─────────┐               │
                         │ Set Up Sector Addr SA0│           │
                         │ Set A1,A0=10, A6=1 │               │
                         └─────────┬─────────┘               │
                                   │                         NO
          ┌───────────►┌─────────▼─────────┐                │
          │            │ Read Data from Device│              │
          │            └─────────┬─────────┘                │
          │                      │                           │
  ┌───────┴────────┐       ┌─────▼─────┐   NO     ┌──────────┴──────┐
  │Increment Sector│       │ Data=00H  ├─────────►│  PLSCNT=1000    │
  │     Addr       │       │    ?      │          │      ?          │
  └───────▲────────┘       └─────┬─────┘          └────────┬────────┘
          │                      │ YES                     │ YES
          │  NO          ┌───────▼───────┐        ┌────────▼────────┐
          └──────────────┤    Sector     │        │  Device Failed  │
                         │  Addr=SA7 ?   │        └─────────────────┘
                         └───────┬───────┘
                                 │ YES
                         ┌───────▼───────┐
                         │ Remove Vld from A9│
                         └───────┬───────┘
                                 │
                         ┌───────▼───────┐
                         │Sector Unprotect│
                         │   Completed    │
                         └───────────────┘
```
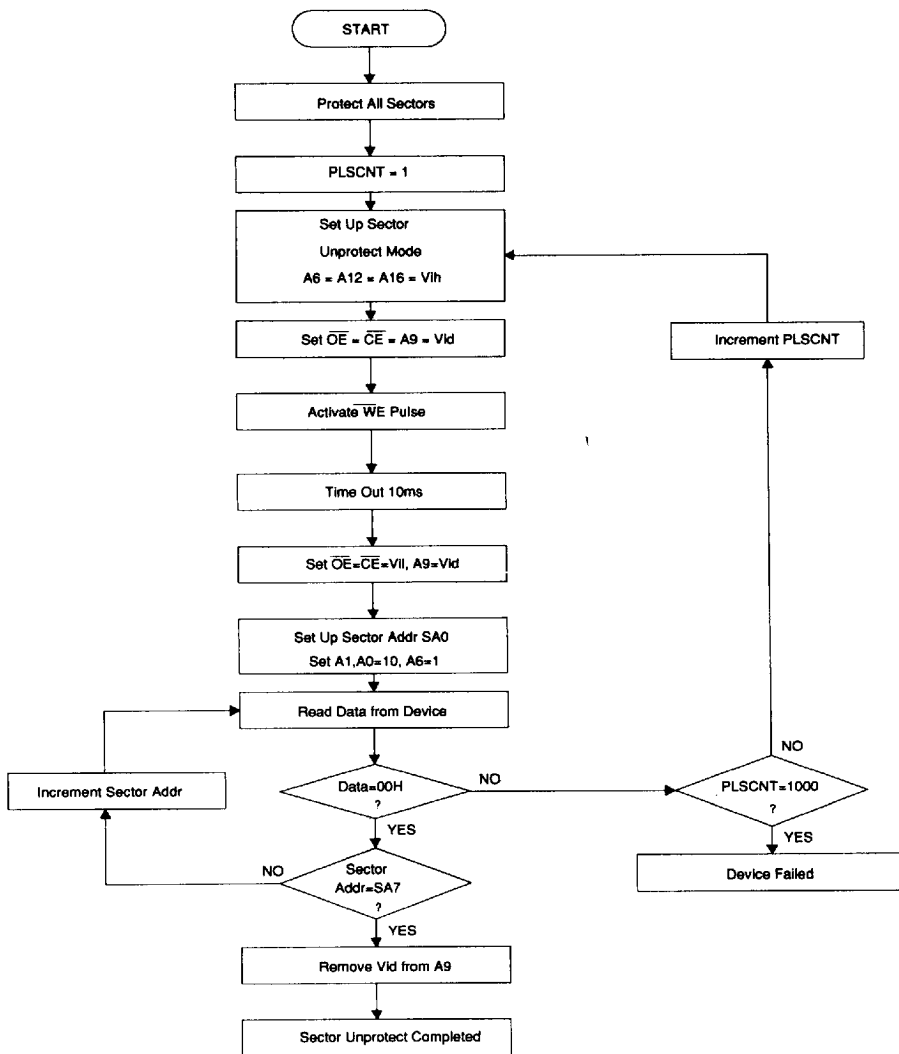
Figure 6. Sector Unprotect Algorithm

4675088 0003859 313

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
  Plastic Packages..................... -65°C to + 125°C

Ambient Temperature
  with Power Applied.................. -55°C to + 125°C

Voltage with Respect to Ground
  All pins except A9 (Note 1)......... -2.0V to + 7.0V
  V_{CC} (Note 1)........................... -2.0V to + 7.0V
  A9 (Note 2)............................. -2.0V to + 14.0V

Output Short Circuit Current (Note 3)...... 200 mA

Notes :
1. Minimum DC voltage on input or I/O pins is -0.5V.
During voltage trasitions, inputs may overshoot V_{SS} to
-2.0V for periods of up to 20 ns. Maximum DC voltage
on output and I/O pins is V_{CC} + 0.5V. During Voltage
transitions, outputs may overshoot to V_{CC} + 2.0V for
periods up to 20ns.

2. Minimum DC input voltage on A9 pin is -0.5V. During
voltage transitions, A9 may overshoot V_{SS} to -2.0V for
periods of up to 20ns. Maximum DC input voltage on
A9 is + 13.5V which may overshoot to 14.0V for periods
of up to 20ns.

3. No more than one output shorted at a time. Duration
of the short circuit should not be greater than one
second.

OPERATING RANGES

Commercial (C) Devices
  .... 0°C to + 70°C
Industrial (I) Devices
  .... -40°C to + 85°C
Extended (E) Devices
  .... -55°C to + 125°C
Vcc Supply Voltages
  .... 4.5V to + 5.5V

Operating ranges define those limits between which the
functionality of the device is guaranteed.

Stresses above those listed under "Absolute Maximum
Ratings" may cause permanent damage to the device.
This is a stress rating only ; functional operation of the
device at these or any other conditions above those
indicated in the operational sections of this specifica-
tion is not implied. Exposure of the device to absolute
maximum rating conditions for expected periods may
affect device reliability.

DC CHARACTERISTICS

Symbol	Description	Min.	Max.	Unit	Test Conditions
I_{LI}	Input Load Current		± 1.0	µA	V_{IN}= V_{SS} to V_{CC}, V_{CC}= VccMax
I_{LIT}	A9 Input Load Current		50	µA	V_{CC}= VccMax, A9= 12.5V
I_{LO}	Output Leakage Current		± 1.0	µA	V_{OUT}= V_{SS} to V_{CC}, V_{CC}= VccMax
I_{CC1}	Vcc Active Current [1]		40	mA	$\overline{CE}$= V_{IL}, $\overline{OE}$= V_{IH}
I_{CC2}	Vcc Active Current [2,3]		60	mA	$\overline{CE}$= V_{IL}, $\overline{OE}$= V_{IH}
I_{CC3}	Vcc Standby Current		1.0	mA	V_{CC}= VccMax, $\overline{CE}$= V_{IH}, $\overline{OE}$= V_{IH}
V_{IL}	Input Low Level	-0.5	0.8	V	
V_{IH}	Input High Level	2.0	VCC + 0.5	V	
V_{ID}	Voltage for Autoselect and Sector Protect	11.5	12.5	V	V_{CC}= 5.0V
V_{OL}	Output Low Voltage		0.45	V	I_{OL}= 12mA, V_{CC}= VccMin
V_{OH}	Output High Voltage	2.4		V	I_{OH}= -2.5mA, V_{CC}= VccMin
V_{LKO}	Low Vcc Lock-Out Voltage	3.2	4.2	V	

Notes :
1. The I_{CC} current listed includes both the DC operating current and the frequency dependent component (at
   6 MHz). The frequency component typically is less than 2 mA/MHz with $\overline{OE}$ at V_{IH}.
2. Icc Active while Internal Algorithm(Program or Erase) is in progress.
3. Not 100% tested.

■ 4675088 0003860 035 ■

AC CHARACTERISTICS

Read Only Operations

Parameter Symbols		Description	Test Setup		-70[1]	-90[2]	-120[2]	-150[2]	Unit
JEDEC	Standard								
t_{AVAV}	t_{RC}	Read Cycle Time [4]		Min.	70	90	120	150	ns
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE} = V_{IL}$ $\overline{OE} = V_{IL}$	Max.	70	90	120	150	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE} = V_{IL}$	Max.	70	90	120	150	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay		Max.	30	35	50	55	ns
t_{EHQZ}	t_{CF}	Chip Enable to Output High Z [3]		Max.	20	20	30	35	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z [3]			20	20	30	35	ns
t_{AXQX}	t_{OH}	Output Hold Time from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurs First		Min.	0	0	0	0	ns

Notes :
1. Test Conditions :
   Output Load : 1TTL gate and 30 pF
   Input rise and fall times : 5ns
   Input pulse levels : 0.0V to 3.0V
   Timing measurement reference level
      Input : 1.5V
      Output : 1.5V

2. Test Conditions :
   Output Load : 1TTL gate and 100 pF
   Input rise and fall times : 20ns
   Input pulse levels : 0.45V to 2.4V
   Timing measurement reference leve
      Input : 0.8V and 2.0V
      Output : 0.8V and 2.0V

3. Output driver disable time
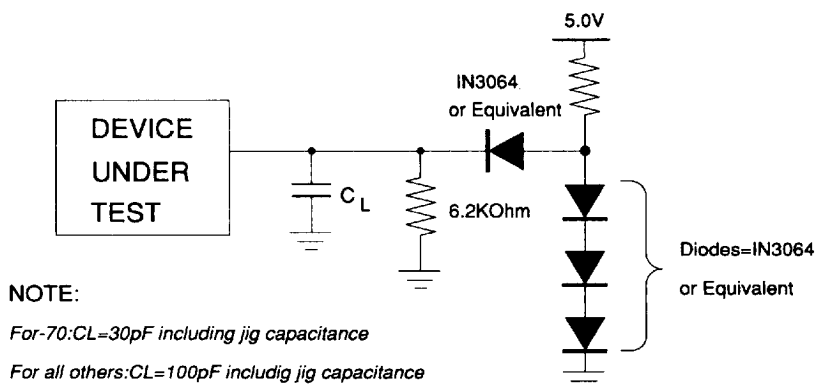4. Not 100% tested

NOTE:

For-70:CL=30pF including jig capacitance

For all others:CL=100pF includig jig capacitance

Figure 7. Test Condition

AC CHARACTERISTICS

Write / Erase / Program Operations

Parameter Symbols		Description		-70	-90	-120	-150	Unit
JEDEC	Standard							
tAVAV	tWC	Write Cycle Time [4]	Min.	70	90	120	150	ns
tAVWL	tAS	Address Setup Time	Min.	0	0	0	0	ns
tWLAX	tAH	Address Hold Time	Min.	45	45	50	50	ns
tDVWH	tDS	Data Setup Time	Min.	30	45	50	50	ns
tWLWH	tDH	Data Hold Time	Min.	0	0	0	0	ns
	tOES	Output Enable Setup Time	Min.	0	0	0	0	ns
	tOEH	Output Enable Read [4]	Min.	0	0	0	0	ns
		Hold Time Toggle and Data Polling	Min.	10	10	10	10	ns
tGHWL	tGHWL	Read Recover Time Before Write	Min	0	0	0	0	ns
tELWL	tCS	$\overline{CE}$ Setup Time	Min.	0	0	0	0	ns
tWHEH	tCH	$\overline{CE}$ Hold Time	Min.	0	0	0	0	ns
tWLWH	tWP	Write Pulse Width	Min.	35	45	50	50	ns
tWHWL	tWPH	Write Pulse Width High	Min.	20	20	20	20	ns
tWHWH1	tWHWH1	Byte Programming Operation	Typ.	16	16	16	16	μs
tWHWH2	tWHWH2	Erase Operation [1]	Typ.	1.5	1.5	1.5	1.5	sec
			Max.	30	30	30	30	sec
	tVCS	Vcc Setup Time [4]	Min.		50	50	50	μs
	tVLHT	Voltage Transition Time [2,4]	Min.		4	4	4	μs
	tWPP	Write Pulse Width [2]	Min.		100	100	100	μs
	tOESP	$\overline{OE}$ Setup Time to $\overline{WE}$ Active [2,4]	Min.		4	4	4	μs
	tCESP	$\overline{CE}$ Setup Time to $\overline{WE}$ Active [3,4]	Min.		4	4	4	μs

Notes :
1. The Erase Operation does not need programming time.
2. These timings are for Sector Protect/ Unprotect Operations.
3. This timing is only for Sector Unprotect.
4. Not 100% tested.

ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits			Unit	Comments
	Min	Typ	Max		
Chip and Sector Erase Time		1.5[1]	30	sec	Excludes 00H programming prior to erasure
Byte Programming Time		16	1000[2]	μs	Excludes system-level overhead
Chip Programming Time		8.5[1]	50	sec	Excludes system-level overhead
Erase/Program Cycles	100,000	100,000		Cycles	

Notes :
1. 25C, 5V Vcc, 100,000 cycles
2. The Internal Algorithms allow for 48 ms byte program time.

■ 4675088 0003862 908 ■