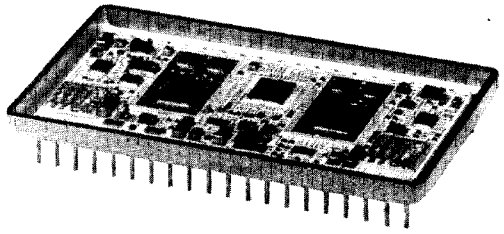
NATEL

HSD/HRD1606

2–Channel, Single Package, 16–Bit Synchro(Resolver)-to-Digital Converters Microprocessor Compatible, 5 V-dc Only

Features

- ✓ **2-Channels In One package** (40-Pin TDIP Hybrid)
- • **1.3 Arc-minute Accuracy**
- ✓ **Independent Tracking Converters** (Type-II servo loops)
- ✓ **True Single Supply . . . 5 Volts Only** (prevents ground loop problems)
- ✓ **100 mW Power Dissipation**
- ✓ **Analog Velocity Outputs** (use as tachometers)
- ✓ **Reference Synthesizers** (for improved dynamic accuracy)
- • **BIT Output (Built-In-Test)** (checks both converters)
- • **Very High Tracking Rate** (1800°/ second for high frequency option)
- • **8- and 16-Bit Microprocessor Compatible** (on-chip channel select)
- • **Hi-Rel MIL-STD-883B Processing**



ACTUAL SIZE

Applications

Avionics systems
Antenna monitoring
Servo systems
Coordinate conversion
Fire control systems
Axis rotation
Engine controllers
Industrial control systems
Simulation
Robotics
Machine tool control systems
Solar panel control systems

Description

The HSD/HRD1606 is the world's first 2-channel hybrid tracking Synchro(Resolver)-to-Digital converter. It contains two independent Type-II servo loop tracking converters in a single 40-pin TDIP while offering the industry's most advanced features. The 1606, like other high performance Natel converters, operates from a single 5 V-dc power supply and consumes only 20 mA of current. This amounts to only 50 mW of power dissipation per channel, which not only makes the Natel 1606 run cool, but results in less strain on the user's power supply and higher component and system MTBF. The 1606 is fully compatible with 8- and 16-bit microprocessors and has a high frequency option with higher tracking speed and wider bandwidth. Additional standard superior features include Built-In-Test, an anti-180° false lock-up circuit, reference synthesizer, and independent high-quality analog velocity outputs.

Each channel of the 1606 is a Type II tracking converter with zero velocity lag error. Internal reference synthesizers permit improved dynamic accuracy by reducing the effects of "speed voltages" at high rotational speeds. The accuracy of the converters are maintained with signal-to-reference phase shifts of up to ±45°. Anti-180° false lock-up circuits are used to assure that the converters do not get locked into an angle 180° from the true angle when a step function of 180° is applied.

Transferring data from the 1606 is eased through the use of a transparent latch with three-state outputs configured as two independently enabled 8-bit bytes. Not only does this allow data to be read without interrupting converter tracking, it also permits memory-mapped data interface and control with most popular 8- and 16-bit microprocessors and single-board computers. Each channel is selected onto the common data outputs by the use of a single "A/$\overline{B}$" control line.

Each converter in the Model 1606 uses an independent high-accuracy differential signal conditioner for the resolver input and a resistive scott-tee for the synchro input, providing common-mode rejection in excess of 70 dB. The input impedance remains constant and balanced independent of dc power to the converter. This feature prevents loading of the synchro and reference input lines when the converters are not powered.

Both independently "selected" and "or'd" Built-In-Test (BIT) outputs are available from the 1606. The BIT feature provides a logic "1" when the tracking error exceeds ±1°. Monitoring of converter dynamics is facilitated through the availability of analog signals corresponding to converter tracking velocity. The velocity outputs are high-quality characterized analog signals that can be used instead of a mechanical tachometer in many servo and control systems.

Theory of Operation

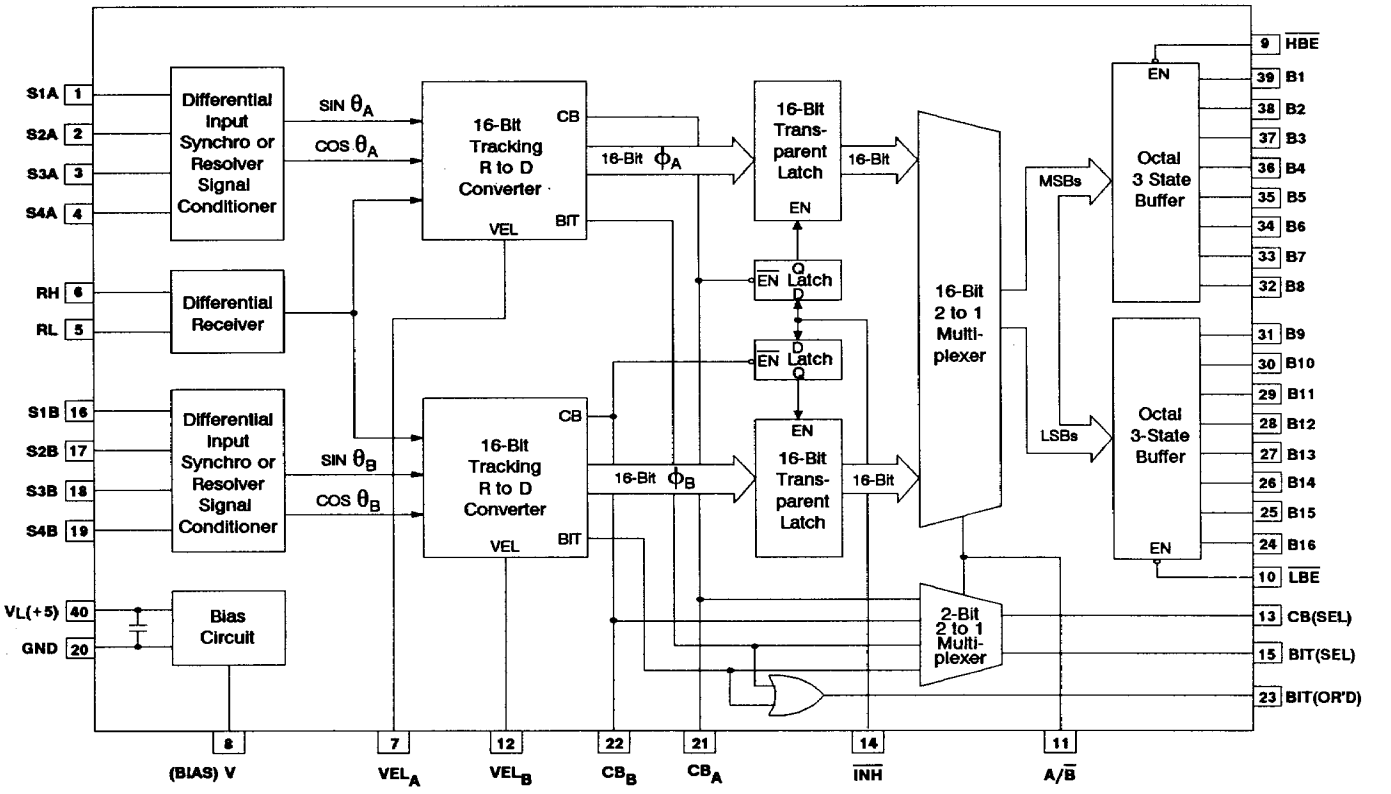


FIGURE 1 1606 Block Diagram

The operation of Model 1606 is illustrated in the functional Block Diagram of Figure 1. The 1606 consists of two independent high-gain Type II tracking converters exhibiting zero error for a constant velocity input. The basic conversion process consists of continuously comparing the digital output angle (ϕ) and the synchro (or resolver) input angle (θ). An up-down counter, containing the feed-back angle, is changed (increased or decreased) until the feed-back angle equals the input angle. The input and feed-back signals are combined in a solid state control transformer to obtain an error voltage according to the following trigonometric identity:

$$\text{"e"} = \sin(\theta - \phi) = \sin\theta\cos\phi - \cos\theta\sin\phi$$

When the error voltage goes to null, $\sin(\theta - \phi)$ is zero, which makes the angle θ equal to the angle ϕ. Thus, the digital output represents the input shaft angle. Once synchronized, the output angle always tracks the input shaft angle without any lag error for constant velocity input.

A description of the internal operation of the "16-Bit tracking R-to-D converter" follows:

The input "signal conditioner" accepts either a synchro or a resolver input and converts it into low level signals sin θ and cos θ, which are applied to a solid state control transformer. The output of the SSCT goes to an error amplifier. The output is applied to a phase-sensitive demodulator that is used to determine the polarity (phase) of the error signal with respect to reference signal. Instead of using the external reference signal (RH, RL) as applied to the converter, Model 1606 generates an improved reference internally. The reference synthesizer obtains this improved reference from sin θ and cos θ signals and uses the external reference for coarse phase determination only.

Use of the improved reference for demodulation allows the Model 1606 to better reject quadrature components in the error signal. The demodulated error signal is applied to an integrator/filter which, in addition to ripple and noise filtering, provides the first integration required for the Type II servo loop. The integrator/filter is also used for appropriate gain and phase compensation for loop stability (optimized for low over-shoot and fast settling time). A wide dynamic range bi-directional VCO performs a voltage-to-frequency conversion whose pulses or counts are accumulated in a 16-bit up-down counter. The up-down counter performs the second integration in the Type II loop. The input to the VCO inherently provides an analog indication of the digital output rate of change (velocity). A more detailed description of converter operation can be found in the data sheet for Natel Model HSD/HRD1046.

The "16-bit transparent latch" provides a means of holding the digital output steady during data transfer, while allowing the converter to continuously track the input angle. The CB output provides a nominal 700 ns pulse for every LSB of output change. It is also used as a gate for the inhibit $\overline{\text{INH}}$ "latches" to prevent attempted "data read" commands during converter data transitions.

The "16-Bit, 2-to-1 multiplexer" and "2-Bit, 2-to-1 multiplexer" select the digital outputs corresponding to either Channel A or Channel B in response to the A/$\overline{\text{B}}$ logic input. The "3-state buffer" output is split into two 8-bit bytes to allow interfacing on both 8- and 16-bit data bus systems. The BIT(SEL) output provides a fault indication for the selected channel.

Reference Synthesizer

To maintain the highest accuracy under both static and dynamic condition, the 1606 utilizes a "reference synthesizer" (one per channel) to correct for a phase difference between the signal and reference inputs of up to $\pm 45^{\circ}$.

Conventional tracking Synchro (Resolver)-to-Digital converters uses a phase-sensitive demodulator to detect the phase and amplitude of the error voltage, $\sin(\theta - \phi)$. One of the functions of the demodulator is to reject quadrature components in the error signal (e). A phase-sensitive demodulator rejects any quadrature signal (signal 90° out of phase) only if the synchro input and its reference are exactly in phase. Zero degree phase shift between reference and signal inputs is not practical in most applications using Synchro (Resolver)-to-Digital converters. Quadrature signal voltage can result from any of the following:

- dynamic synchro/resolver "speed voltages," a quadrature signal that is proportional to the shaft rotational speed
- synchro/resolver "null voltages"
- capacitive coupling between synchro lines
- differential phase shift in synchro/resolver lines

This quadrature voltage will cause angular error as a variable offset if there is a phase difference between input signals and reference. For example for a 60-Hz synchro with a 5° phase shift rotating at 2 rps (720°/sec), the dynamic error due to speed voltage would be 0.17° or 10 arc-minutes!

Natel's Model 1606 greatly reduces the effects of this error by creating a synthetic reference. The sine and cosine voltages from the signal conditioner are combined to obtain an in-phase internal reference. Together with the external reference voltage (to determine phase) this improved reference is used for demodulating the error voltage.

Built-In-Test (BIT)

A BIT signal (pins 15 and 23) provides an over-velocity or fault indication output signal. The error voltage of the converter is monitored continuously, and when the tracking error exceeds approximately 1° (over-velocity or failure), a logic "1" signal is generated to indicate invalid data. Under normal operation the BIT output is at logic "0". Possible conditions that will cause the BIT output to show fault indication are:

- Power-turn-on – BIT output will return to logic "0" when the converter synchronizes to correct input angle $\pm 1^{\circ}$
- Step-input – instantaneous input changes greater than $\pm 1^{\circ}$ until the converter synchronizes
- Over velocity condition
- Excessive shaft angle modulation
- Reference voltage disconnected
- Loss of signal – all signal lines are disconnected
- Converter malfunction – any converter failure which prevents synchronization to the input angle

Note that the BIT output has $\geq$50% duty cycle logic "1" when reference lines and/or signal lines are disconnected. The cycle frequency is synchronous with the carrier frequency when either the signal or reference (but not both) is missing. When both signal and reference lines are disconnected, the cycle frequency is $\geq$2 Hz. Either Channel A or Channel B BIT is selected depending on the $A/\overline{B}$ select input (pin 11). Pin 23 (OR'D BIT) provides a fault indication for Channel A or B regardless of the state of the $A/\overline{B}$ select input.

No 180° False Lock-up

An additional feature of the Model 1606 eliminates "false 180° digital output readings," during instantaneous 180° input step changes. "180° false lock-up" can occur in most Synchro-to-Digital converters whenever the synchro(resolver) input angle is "electronically switched" or stepped from one angle to another by 180°. This occurrence is most common in applications where the input is being supplied by a Digital-to-Synchro converter and the MSB (180° BIT) is turned "ON" or "OFF".

The reason this occurs in most Synchro-to-Digital converters is because the solid-state control transformer (SSCT) used in the conversion process can produce two (2) "nulls" at the error output "e" for a given digital feedback angle. This is easily understood by trignometric indentity

$$\sin[(\theta - \phi) + 180] = -\sin(\theta - \phi) = \sin(\theta - \phi)$$

when

$$(\theta - \phi) = \text{zero}$$

Since error output "e" is a sine function (see theory of operation) this creates a possibility of a second null and the converter locking-up 180° away from the true angle.

Natel's Model 1606 gets around this problem by continuously monitoring $\sin\theta$ and $\cos\theta$ signals and comparing the phase relationship with the digital output angle and reference input (RH, RL). When a 180° input step is applied, the internal BIT-detect circuit is activated, which forces an error in the converter loop to move the digital output angle to the correct reading. As soon as the digital output is properly phased with the shaft angle input, this "intentional error" is removed from the converter loop.

True Single-Supply 5 V-dc Operation

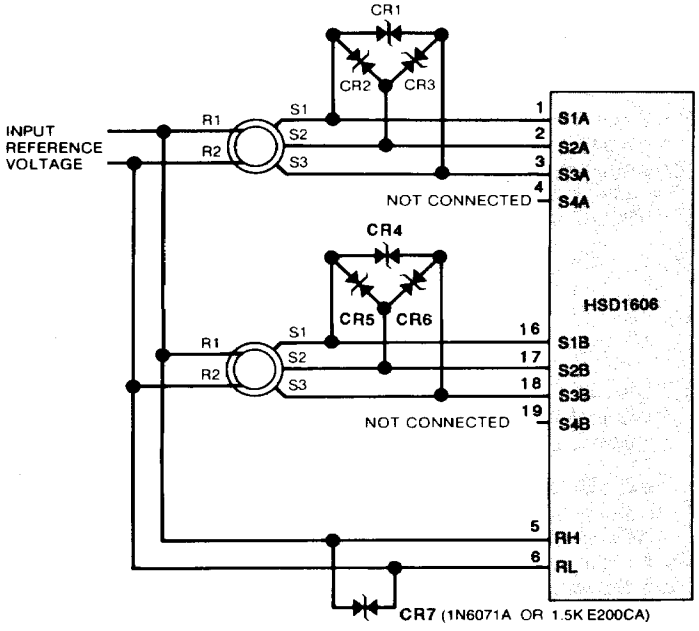
One of the most outstanding features of the Model 1606 is the single +5 V-dc power supply requirement. This feature simultaneously eliminates both unwanted "ground loop" problems and allows the elimination of $\pm$15 V-dc power supplies in all-digital systems.

Without the single supply operation, systems that use separate analog and digital grounds for $\pm$15 V-dc and +5 V-dc power, as many systems do, would be faced with potential ground loop problems. The result is usually excess noise on either the analog or digital supplies, which limits the effectiveness of single-point grounding schemes. These ground loops would be present with a converter that used both $\pm$15 V-dc and digital +5 V-dc power because the analog ($\pm$15 V-dc) and digital (+5 V-dc) power supplies are referenced to different grounds while multiple supply converters have only a single internal ground. The 1606 takes the agony out of these difficult systems problems by operating entirely within the digital power and ground rails of your system.

All internal circuitry is designed to operate with power supply voltage of as low as 4.5 V-dc. This is made possible by using high signal-to-noise ratio amplifiers and a unique design approach incorporated into a custom LSI chip. No performance specification is sacrificed due to the single 5 V-dc operation. In fact, the 1606 offers the most advanced design features ever available in any Synchro/Resolver-to-Digital converter.

Operating with a 5 V-dc supply, the dual converter typically requires only 20 mA of current. This low power operation results in a typical junction-to-ambient (no heat sink) temperature rise of only 4°C!

V_{L-L} INPUT	CR1-CR6
11.8 V-rms	1N6049A OR 1.5KE27CA
90 V-rms	1N6070A OR 1.5KE200CA



$$E_{S3-S1} = V_{max} \sin\theta$$
$$E_{S2-S3} = V_{max} \sin(\theta + 120°)$$
$$E_{S1-S2} = V_{max} \sin(\theta + 240°)$$

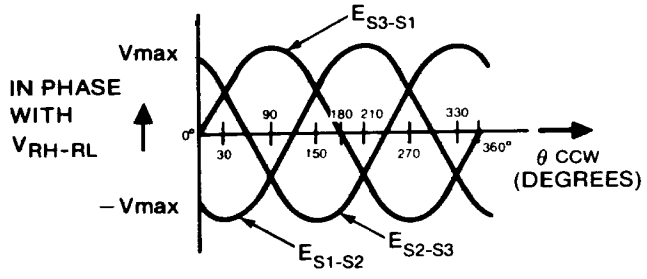
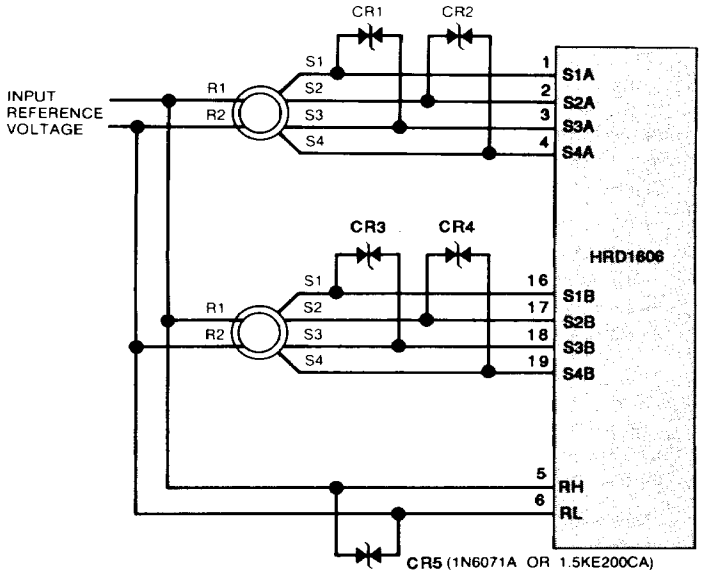


FIGURE 2 Synchro Inputs

V_{L-L} INPUT	CR1-CR4
11.8 V-rms	1N6049A OR 1.5KE27CA
26 V-rms	1N6057A OR 1.5KE56CA
90 V-rms	1N6070A OR 1.5KE200CA



$$E_{S3-S1} = V_{max} \sin\theta$$
$$E_{S2-S4} = V_{max} \cos\theta$$

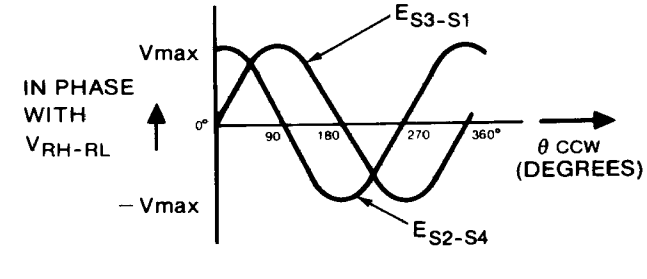


FIGURE 3 Resolver Inputs

The connections for synchro and resolver inputs are shown in Figure 2 and Figure 3. The input signal conditioners use differential amplifiers and matched precision resistors to provide a high common-mode rejection ratio. This eliminates the need for external transformers for most applications. The input signal conditioner performs two functions. For both synchro and resolver format inputs it serves as a precision attenuator reducing the amplitude of high level ac input signals to levels which can be processed by the converter. For a synchro input, this network transforms three wire synchro information into resolver format (sin θ and cos θ).

Both signal and reference inputs are true differential inputs and use precision thin film resistors for signal attenuation. If input voltages exceed the absolute maximum ratings, the thin-film resistors may be destroyed. To prevent this from happening, it is recommended that transient voltage suppressors be installed on both signal and reference lines. Synchros and resolvers are highly inductive and can generate or couple transients many times greater than their normal signal voltages and can easily exceed the absolute maximum ratings. This situation is particularly likely to occur in cases where the excitation or source voltage for the synchro (resolver) is switched on or off. Transients can also occur by other equipment being turned on or off. Figures 2 and 3 show recommended methods of connecting synchro and resolver inputs. Transient voltage suppressors given in the tables (or equivalent) must be used to assure input protection.

Pin Designations

V_L — Power Supply Voltage
Logic Voltage
5 V-dc ±10%

GND — Power Supply Ground
Digital Ground

B1 - B16 — Parallel Output Data Bits -
B1 is MSB = 180 degrees
B16 is LSB = 0.0055 degrees

S1A,B S2A,B Input Analog Signals
S3A,B S4A,B S4 is NC for synchro-input model
A = channel A inputs
B = channel B inputs

RH, RL — Reference Voltage Input

VEL A
VEL B — Velocity Output -
dc analog voltage proportional to rotational speed of the input shaft angle. Output is referenced to bias voltage (V)

BIAS (V) — Bias Voltage -
Internally generated reference voltage serves as reference ground for the velocity outputs.

A/$\overline{B}$ — Output Data Select Contol -
Selects desired data at B1 through B16 to represent "Channel A" or "Channel B" angle information, as well as the corresponding Built-In-Test and Converter Busy signals BIT(SEL) and CB(SEL) respectively. Logic "1" selects "Channel A," logic "0" selects Channel B."

$\overline{INH}$ — Inhibit Function -
A logic "0" freezes the digital angular output of both A and B channels. Internal loop keeps tracking the analog input. All other outputs keep following the input. For continuous operation this pin may be left unconnected. Internal pull-up will apply V_L to the pin.

CB (SEL) — Converter Busy (Selected) -
A 700 ns pulse which occurs during updating of the internal 16-bit data output latches. Output data transitions occur during the middle of the busy pulse (output data can be transferred at the trailing edge of a CB pulse). A positive pulse occurs whenever the corresonding converter changes by 1 LSB. CB pulses are NOT inhibited by the application of $\overline{INH}$, $\overline{LBE}$ or $\overline{HBE}$. The appropriate CB (CB_A or CB_B) is selected by using output select control input A/$\overline{B}$ (pin 11). Logic "1" selects CB_A, logic "0" selects CB_B.

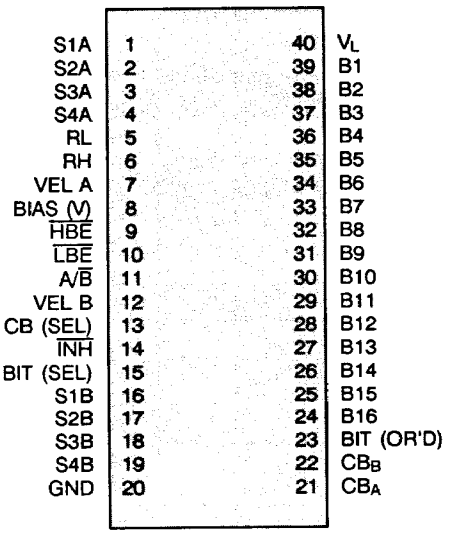


FIGURE 4 HSD/HRD1606 Pin Assignments

CB_A — Converter Busy A -
Internal converter update pulse for channel A [see CB(SEL)].

CB_B — Converter Busy B -
Internal converter update pulse for channel B [see CB(SEL)].

BIT (SEL) — Built-In-Test -
A "1" output indicates that output is not tracking the input analog signal within ±1°. When A/$\overline{B}$ is logic "1," BIT = BIT A. When A/$\overline{B}$ is logic "0," BIT = BIT B.

BIT (OR'D) — A logic "1" output indicates that either channel A or channel B output is not tracking the input analog signal within ±1°.

$\overline{HBE}$ — High Byte Enable -
Data bits B1 through B8 are enabled (low-impedance state of 3-state output) when $\overline{HBE}$ is set to a logic "0." When $\overline{HBE}$ is set to a logic "1," the data bits B1 through B8 are disabled (high-impedance state of 3-state output).

$\overline{LBE}$ — Low Byte Enable -
Data bits B9 through B16 are enabled when $\overline{LBE}$ is set to a logic "0." When $\overline{LBE}$ is set to logic "1," the data bits B9 through B16 are disabled.

Absolute Maximum Ratings

Signal Inputs . . . . . Twice Normal Voltage
Reference Input . . . . . 200 V-rms
Supply Voltage (V_L) . . . . . +6.5 V-dc
Digital Inputs . . . . . – 0.3 V-dc to V_L
Storage Temperature . . . . . – 65°C to +135°C

When installing or removing the converter from printed circuit boards or sockets, it is recommended that the power supplies and input signals be turned off. Decoupling capacitors are recommended on the power supply V_L. A 1 µF tantalum capacitor in parallel with 0.01 µF ceramic capacitor should be mounted as close to the supply pin (40) as possible.

Specifications

PARAMETER	VALUE	REMARKS	TEST LEVEL
Digital Output Resolution			
	16-bits (0.33 arc-minutes)		Note 2
Accuracy			
	± 5.2 arc-minutes (Option S) ± 2.6 arc-minutes (Option H) ± 1.3 arc-minutes (Option V)	Accuracy applies over the full operating temperature range, ±10% frequency varation and includes hysteresis	Note 1
Reference Input			
Voltage	20 to 130 V-rms		Note 2
Frequency	700 to 3000 Hz (Option 8) 360 to 1000 Hz (Option 4) 47 to 1000 Hz (Option 6)	800 Hz Models 400 Hz Models 60Hz Models	Note 3
Input Impedance (minimum)	250 K Ω Single Ended 500 K Ω Differential		Note 2
Common-Mode Range	±250 V peak maximum	dc plus recurrent ac peak	Note 3
Synchro/Resolver Inputs			
Input Voltages (line-to-line)	11.8 V-rms (Option 1) 26 V-rms (Option 2) 90 V-rms (Option 9)	Accuracy of the converter is maintained with ±10% variation in signal voltages	Note 1
Input Impedance (minimum)	30K Ω (60 K Ω) minimum 75K Ω (150 K Ω) minimum 250 K Ω (500 K Ω) minimum	Line-to-GND (differential), 11.8 V-rms L-L Models Line-to-GND (differential), 26V-rms L-L Models Line-to-GND (differential), 90V-rms L-L Models	Note 2
Impedance Unbalance	0.2% maximum	For all Models	Note 3
Common-Mode Range	± 25V peak ± 55V peak ±180V peak	11.8 V-rms Models 26 V-rms Models 90 V-rms Models	Note 3
Common-Mode Rejection	70 dB minimum	dc to 1000 Hz	Note 3
Harmonic Distortion	10% maximum	Without degradation in accuracy specification	Note 3
Reference Sysnthesizer			
Phase-shift allowed between Input signals and Input reference	±45° guaranteed ±65° typical	Without any degradation of converter accuracy	Note 2
Digital Inputs		**CMOS transient protected**	
$\overline{HBE}$	Logic "1" Logic "0"	8 MSB's are in the high impedance state of 3 state output 8 MSB's are enabled	Note 1
$\overline{LBE}$	Logic "1" Logic "0"	8 LSB's are in the high impedance state of 3-state output 8 LSB's are enabled	Note 1
$\overline{INH}$	Logic "1" Logic "0"	Digital output follows analog input signal Output data latched in holding register (does not interrupt converter tracking loop)	Note 1
A/$\overline{B}$	Logic "1" (Logic "0")	Channel A (Channel B) digital output selected. Affects B1 - B16, BIT (SEL), CB (SEL)	Note 1
Voltage Levels Logic "0" Logic "1"	 -0.3 V-dc to 0.8 V-dc 2.4 V-dc to 5.0 V-dc	For V_L = 5 V-dc	Note 2
Input Currents			
$\overline{HBE}$, $\overline{LBE}$	100 K Ω (typical) pull up to the power supply (V_L)		Note 3
$\overline{INH}$	100 K Ω (typical) pull up to the power supply (V_L)	When not used, may be left unconnected	Note 3

Specifications Continued

PARAMETER	VALUE	REMARKS	TEST LEVEL
Digital Outputs		**CMOS Outputs**	
Data Bits (B1-B16)	Natural Binary Angle	Positive logic	
CB (A,B,SEL)	Logic "0" Logic "1"	Output angle not changing Output angle changing (leading edge initiates output change - see figure 5) CB_A = Channel A CB output CB_B = Channel B CB output CB(SEL) = CB_A when $A/\overline{B}$ = Logic "1" CB(SEL) = CB_B when $A/\overline{B}$ = Logic "0"	Note 1
BIT (SEL,OR'D)	Logic "0" Logic "1"	Digital output tracking analog input Fault indication (tracking error > $\pm 1^\circ$ typical) BIT(SEL) = BIT (Channel A) when $A/\overline{B}$ = logic "1" BIT(SEL) = BIT (Channel B) when $A/\overline{B}$ = logic "0" BIT(OR'D) = BIT (Channel A) "or" BIT (Channel B)	Note 1
Drive Capability Data Bits (B1-B16), CB (SEL), BIT (SEL)	2 standard TTL minimum	For V_L = 4.5 V-dc, over full temp range	Note 3
Logic "0" sink current Logic "1" source current	3.2 mA (min) @ 0.40 V-dc -3.2 mA (min) @ 3.0 V-dc	See Figure 10 for typical drive currents	Note 3
CB_A, CB_B, BIT (OR'D)	1 standard TTL minimum	Typical drive currents are 1/2 that shown in fig. 10	Note 3
HI-Z Output Leakage Data Bits (B1-B16)	±10 µA maximum	Output capacitance = approximately 5 pF	Note 3
Analog Outputs	**Typical, unless specified**		
V (Bias Voltage)	1/2 (V_L-0.7) ±10%	2.15 V-dc ±10% for 5 V-dc supply	Note 3
Drive Capability	± 1 mA minimum	All analog outputs	Note 3
θA,θB Velocity Outputs	**Typical, unless specified**	**dc voltage referenced to V (bias)**	
Polarity	Negative for increasing angle		Note 3
Scale Factor (Gain) @ 25°C	0.835 mV/deg/sec typical 1.22 mV/deg/sec. typical 6.11 mV/deg/sec. typical	800 Hz Models 400 Hz Models 60 Hz Models	Note 2
Temperature Coefficient Power Supply Dependence	± 500 PPM/°C typical -1% per percent maximum		Note 3
Full Scale Output @ 25°C	1.5 V-dc @ 1800°/sec typical 1.1 V-dc @ 900°/sec typical 1.1 V-dc @ 180°/sec typical	800 Hz Models 400 Hz Models 60Hz Models	
Linearity @ 25°C	± 5% of full scale maximum ± 2% of full scale maximum ± 1% of full scale maximum	800 Hz Models 400 Hz Models 60Hz Models	Note 2
Temperature Coefficient Power Supply Dependence	± 200 PPM/°C typical 0.1% per percent typical		Note 3
Output Noise Static Input	3 mV-rms typical	All Models	Note 3
Maximum tracking rate	15 (30) mV-rms typical	For 800, 400 (60) Hz Models	Note 3
Output Offset @ 25°C	± 5 mV-dc typical ± 20 mV-dc maximum	All Models	Note 2
Temperature Coefficient Power Supply Dependence	± 30 µV/°C typical ± 20 µV per percent typical		Note 3
Δ Gain vs. Polarity	10% maximum	All Models	Note 2
Temperature Coefficient Power Supply Dependence	± 200 PPM/°C typical 0.1% per percent typical		Note 3

PARAMETER	VALUE	REMARKS	TEST LEVEL
Dynamic Characteristics	**Typical, unless specified**	**Specified for power supply = +5 V-dc**	
Velocity Constant (K_V)	∞	Type II servo loop	Note 3
Tracking Rate (minimum)	1800°/sec 900°/sec 180°/sec	800 Hz Models 400 Hz Models 60 Hz Models	Note 1
Maximum Acceleration (typical)	400,000°/sec^2 100,000°/sec^2 4,000°/sec^2	800 Hz Models 400 Hz Models 60 Hz Models	Note 3
Acceleration Constant (nominal)	192,000°/sec^2 48,000°/sec^2 1,920°/sec^2	800 Hz Models 400 Hz Models 60 Hz Models	Note 3
Acceleration for 1 LSB error (LSB = 0.0055°)	1,055°/sec^2 264°/sec^2 11°/sec^2	800 Hz Models 400 Hz Models 60 Hz Models	Note 3
Settling time to 1 LSB (for 179° step change)	150 ms maximum 300 ms maximum 1350 ms maximum	800 Hz Models 400 Hz Models 60 Hz Models	Note 2
Settling time to 1 LSB (small signal step < 1.4°)	25 ms maximum 50 ms maximum 250 ms maximum	800 Hz Models 400 Hz Models 60 Hz Models	Note 2
Converter Bandwidth	200 Hz typical 100 Hz typical 20 Hz typical	800 Hz Models 400 Hz Models 60 Hz Models	Note 3
Power Supply			
Voltage	5 V-dc ±10%	Without degradation in accuracy specification	Note 3
Current	60 mA typical, 90 mA maximum 20 mA typical, 40 mA maximum	800 Hz Models 400, 60 Hz Models	Note 1
Thermal Characteristics			
Junction Temperature Rise Above Case	2°C typical, 4°C maximum	For component with highest temperature rise	Note 3
Case Temperature Rise Above Ambient	4°C typical, 8°C maximum 16°C maximum (800 Hz Models)	Without any heat sink	Note 3
Power Dissipation	100 mW typical, 200 mW maximum 450 mW maximum (800 Hz Models)	For V_L = 5 V-dc	Note 3
Physical Characteristics			
Type	40-pin Hermetic Triple Dip		
Size	1.14 X 2.14 X 0.21 inch (29 X 54.4 X 5.3 mm)	3 Standoffs are added to the package to insulate it from the printed circuit board traces (Standoffs included in 0.21 inch height dimension)	Note 3
Weight	0.9 oz (26 g) maximum		Note 3

NOTE 1: Compliance of each component to this specification is 100% guaranteed by Natel. To assure compliance, this key parameter is 100% tested.

NOTE 2: Compliance of each component to this specification is 100% guaranteed by Natel. To assure compliance, AQL levels are verified using a lot sample level in the range of one to five percent.

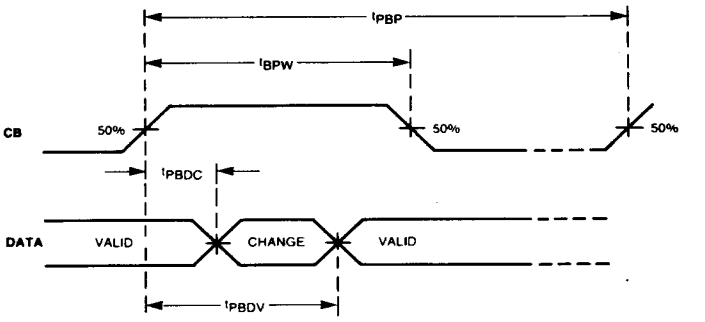
NOTE 3: Compliance of each component to this specification is 100% guaranteed by Natel. To assure compliance, AQL levels are verified using a lot sample level of less than one percent. Note 3 parameters are maximum design limits.

If your application requires 100% testing of any additional parameters of this specification or requires non-standard input or output characteristics, please contact a Natel Applications Engineer or the Sales Department.

R_L = 200 K Ω Input t_r t_f = 20 ns V_L = 5 V-dc C_L = 50 pF

(Specifications apply over full operating temperature range)

CHARACTERISTIC	LIMITS			UNITS	FIG.
	MIN	TYP	MAX		
Busy Pulse Width (t_{BPW})	0.4	0.7	1.2	μs	5
Busy Period (t_{PBP})	2.0	Note 1	Inf	μs	5
Busy to Data Change (t_{PBDC})	100	350	–	ns	5
Busy to Data Valid (t_{PBDV})	–	350	600	ns	5
Inhibit to Data Stable (t_{PIDS})	0	400	700	ns	6, 7
Inhibit to Data Update (t_{PIDU})	10	–		ns	6, 7
Inhibit Update Pulse Width (t_{IPW})	1.3	8	–	μs	7
3-State High Z to Low Z (t_{PHZL})	3	10	30	ns	8
3-State Low Z to High Z (t_{PLZH})	3	10	30	ns	8
Channel Select Time (t_{ABS})	–	15	40	ns	9
Output Transition Time (10%-90%)					
B1-B16 CB(SEL) BIT (SEL)	–	6	20	ns	–
CB_A CB_B BIT(OR'D)	–	12	40	ns	–



NOTE 1: **Busy Period (t_{PBP})** = $\frac{K \cdot 10^6}{2^N \cdot R}$ (μs)

Where,

N = Converter Resolution (16)

K = 360 (For Degrees) or = 2π (For Radians)

and

R = Rate (Degrees / Second) or = Rate (Radians / Second)

For Reference:

Busy Frequency = $\frac{2^N \cdot R}{K}$ (Hz)

Rate (R) = $\frac{K \cdot \text{Busy Frequency}}{2^N}$

FIGURE 5 Converter Busy and Data Timing

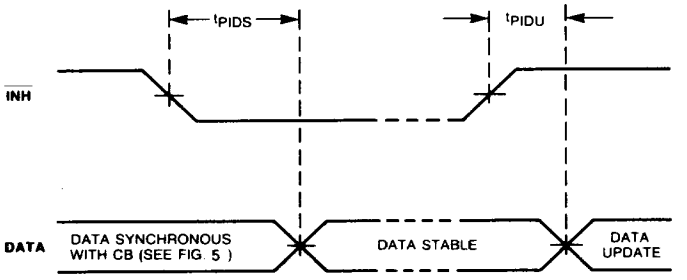


FIGURE 6 Inhibiting Output Data Update

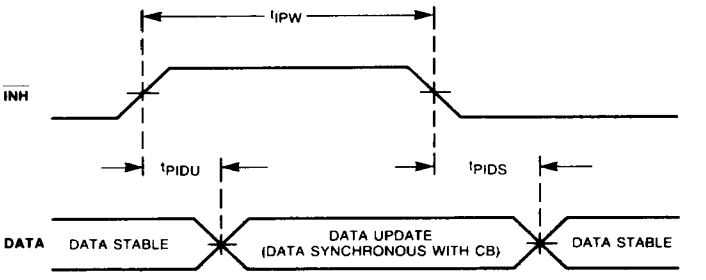


FIGURE 7 Enabling Output Data Update

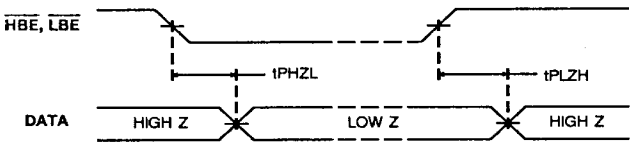


FIGURE 8 3-State Output Timing

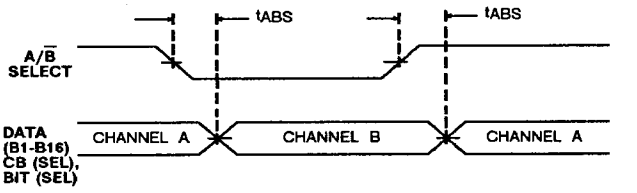
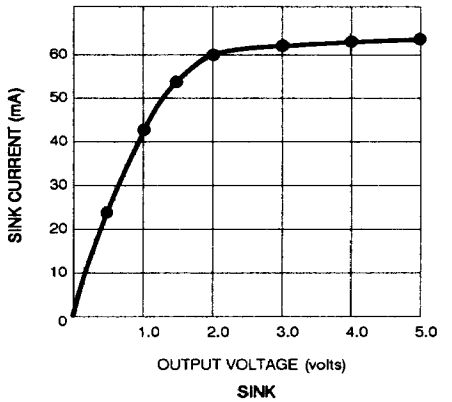


FIGURE 9 Channel Select Time



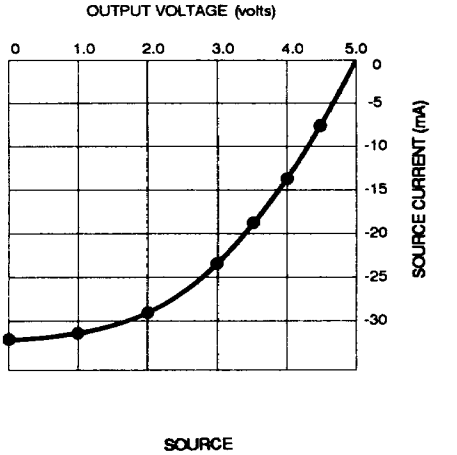


FIGURE 10 Output Drive Current (Typical @ V_L = 5 V-dc, Ta = 25°C)

Data Transfer

Due to the nature of the Type II servo conversion mechanism incorporated in the 1606, the output data angle always tracks the synchro (resolver) input shaft angle within the converter's rated maximum tracking rate (angular velocity) and bandwidth. Theoretically, for every 0.0055 degree of input angle change there will be a corresponding data output change of one LSB. To prevent reading data during an output change or transition, the following methods of data transfer can be used.

1) Synchronous transfer with shaft angle change.

   Use CB (Converter Busy) pulse to clock data into an external register. Use the falling edge of CB as an edge triggered clock. (Rising edge of CB could be used but data would have an additional error of ±1 LSB.) Data changes within 600 ns after the rising edge of the CB pulse.

2) Asynchronous transfer with shaft angle change (using CB).

   Monitor the CB (Converter Busy) during a data transfer attempt. If CB is at logic "1," (the data will be void) . . . try another data transfer attempt. If CB is at logic "0" the data will be good. Note that the longest CB pulse width and therefore the longest wait period is 1.2 μsec. The pulse can essentially be used to gate an external data clock enable since the converter updates within the CB logic "1" duration (1.2 μs maximum).

3) Asynchronous transfer with shaft angle change (using $\overline{INH}$).

   The simplest method of data transfer (which is completely independent of input shaft angle change) is to use the inhibit ($\overline{INH}$) function to hold or freeze the current data output angle. Set the $\overline{INH}$ input to logic "0" . . . wait a minimum of 700 ns . . . transfer the data . . . return $\overline{INH}$ to logic "1" for a minimum of 1.3 μs. This method of asynchronous data transfer from the 1606 is shown in Figure 11.

It should be noted that the $\overline{INH}$ control does not affect the conversion process . . . it only affects the transparent output latches. If the synchro (resolver) angle input changes while an inhibit is applied ($\overline{INH}$ = "0"), the internal data angle (up-down counter output) will still track the input. Fresh output data (B1-B16) will be available within 1.3 μs after the $\overline{INH}$ input returns to logic "1" (un-inhibit), regardless of the previous $\overline{INH}$ logic "0" duration.

Note: The CB output (Converter Busy) will always produce a pulse for every LSB of internal output angle change, regardless the state of the $\overline{INH}$ (inhibit) input.

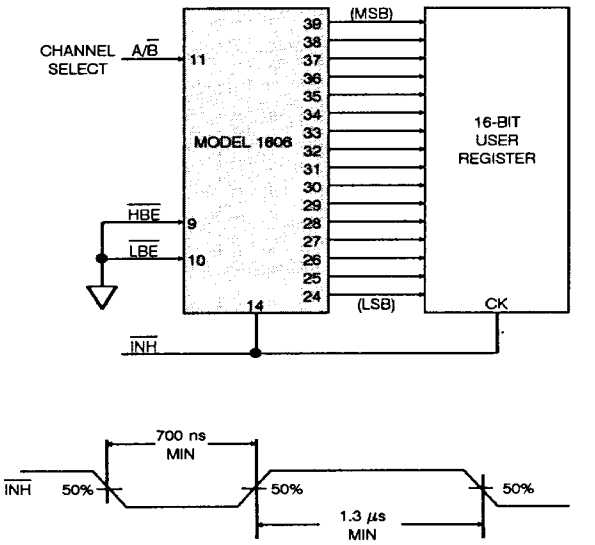


FIGURE 11 Asynchronous Data Transfer

Single-Byte Data Transfer on 16-Bit Data Bus

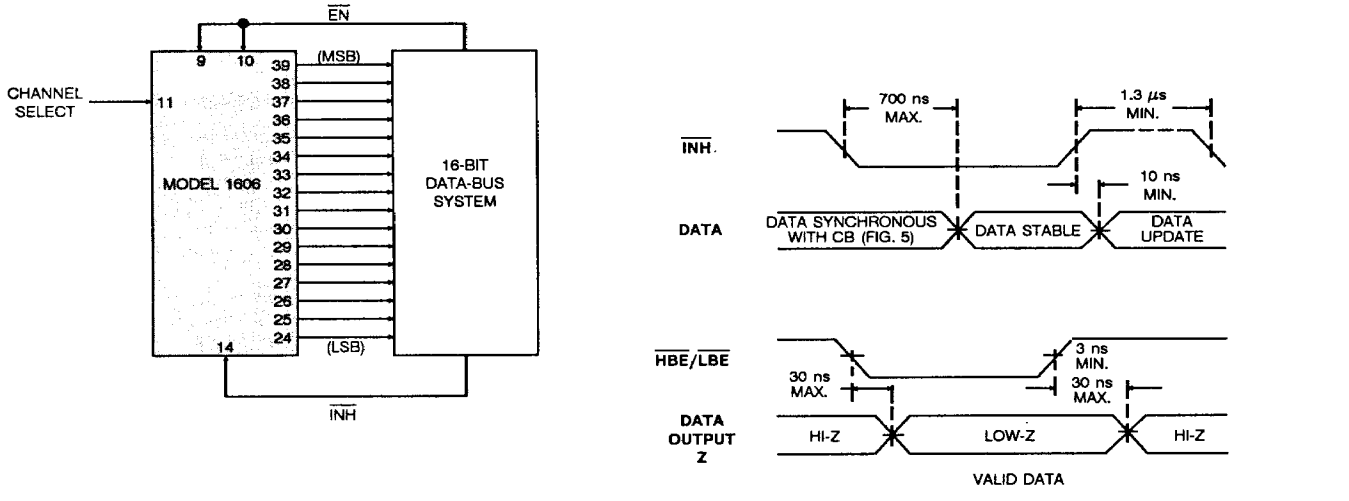


FIGURE 12 Digital Connections and Timing for Single-Byte Data Transfer

The circuit configuration and timing diagram for transferring data from the Model 1606 to a 16-bit 3-state data-bus system is shown in Figure 12. A typical sequence of events would be as follows:

1) Apply the $\overline{INH}$ input for a minimum of 700 ns before transferring valid data.
2) Set A/$\overline{B}$ (Channel Select) to logic "1" (Channel A) for a minimum of 40 ns before transferring valid data.
3) Set $\overline{HBE}$/$\overline{LBE}$ to logic "0" (3-state enables) for a minimum of 30 ns before transferring valid data.
4) Transfer Channel "A" Data.
5) Set A/$\overline{B}$ (Channel Select) to logic "0" (Channel B) for a minimum of 40 ns before transferring valid data.
6) Transfer Channel "B" Data.
7) Return $\overline{HBE}$/$\overline{LBE}$ to logic "1" at least 30 ns before the next device is put on the data bus.
8) Return $\overline{INH}$ to logic "1" no earlier than 10 ns before valid data is transferred. The $\overline{INH}$ input may remain at logic "0" indefinitely . . . but must return to logic "1" for a minimum of 1.3 µs to allow update of fresh accurate output data.

Notes:

- $\overline{INH}$ (inhibit) and A/$\overline{B}$ (Channel Select) input function are independent from $\overline{HBE}$ and $\overline{LBE}$ (3-state) inputs.
- The CB output (Converter Busy) will always produce a pulse for every LSB of converter angle change, regardless the state of the $\overline{INH}$ (Inhibit) input or $\overline{HBE}$/$\overline{LBE}$ (3-state enable) inputs.
- Converter "Channel Selection" (A or B) can be done in any sequence with repect to $\overline{INH}$ (Inhibit) and $\overline{HBE}$/$\overline{LBE}$ (3-state) controls.

Two-Byte Data Transfer on 8-Bit Data Bus

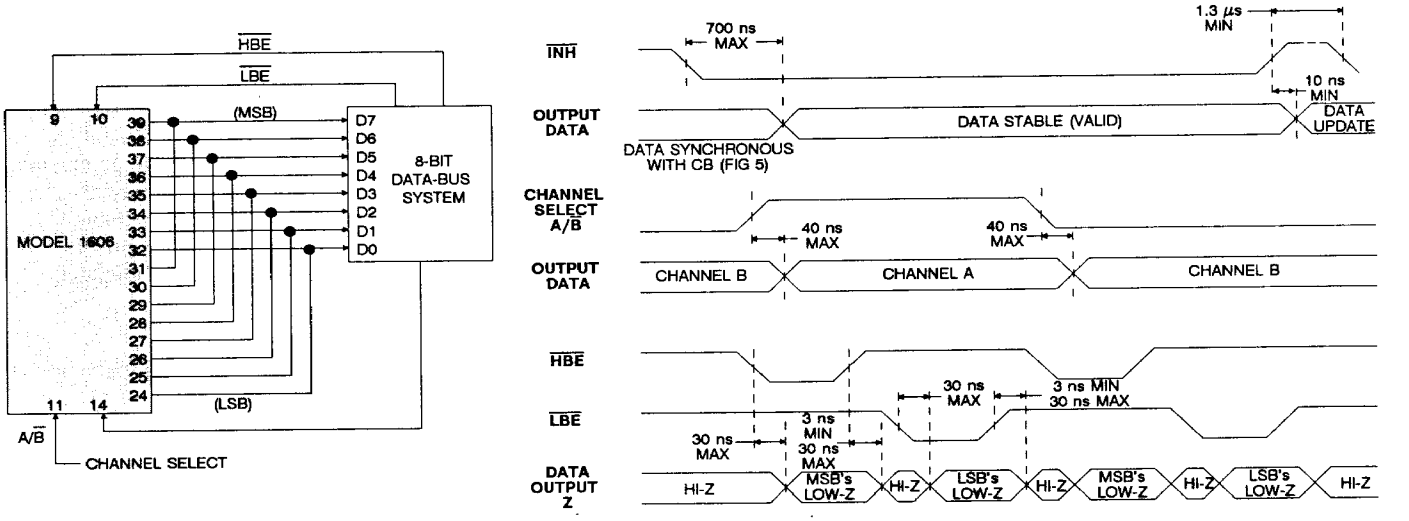


FIGURE 13 Digital Connections And Timing For Two-byte Data Transfer

The circuit configuration and timing diagram for transferring data from Model 1606 to an 8-bit 3-state data-bus system is shown in Figure 13. A typical sequence of events would be as follows:

1) Apply the $\overline{INH}$ input for a minimum of 700 ns before transferring valid data.
2) Set A/$\overline{B}$ (Channel Select) to logic "1" (Channel A) for a minimum of 40 ns before transferring valid data.
3) Set $\overline{HBE}$ (high-byte-enable) to logic "0" for a minimum of 30 ns before transferring valid data (MSB's).
4) Transfer MSB's.
5) Return $\overline{HBE}$ to logic "1".
6) Set $\overline{LBE}$ (low-byte-enable) to logic "0" for a minimum of 30 ns before transferring valid data (LBS's).
7) Transfer LSB's.
8) Return $\overline{LBE}$ to logic "1".
9) Set A/$\overline{B}$ (Channel Select) to logic "0" (Channel B) for a minimum of 40 ns before transferring valid data.
10) Repeat steps 3 through 8.
11) Return $\overline{INH}$ to logic "1" no earlier than 10 ns before valid data is transferred. The $\overline{INH}$ input may remain at logic "0" indefinitely . . . but must return to logic "1" for a minimum of 1.3 µs to allow update of fresh accurate output data.

Notes:

$\overline{HBE}$ and $\overline{LBE}$ data bytes can be transferred in any sequence ($\overline{HBE}$ or $\overline{LBE}$ first). The timing requirements are the same for both $\overline{HBE}$ and $\overline{LBE}$ data byte enables.

$\overline{INH}$ (inhibit) and A/$\overline{B}$ (channel select) input functions are independent from $\overline{HBE}$ and $\overline{LBE}$ (3-state) inputs.

The CB output (Converter Busy) will always produce a pulse for every LSB of converter angle change, regardless of the state of the $\overline{INH}$ (inhibit) input or $\overline{HBE}$/$\overline{LBE}$ (3-state enable) inputs.

Converter "Channel Selection" (A or B) can be done in any sequence with respect to $\overline{INH}$ (inhibit) and $\overline{HBE}$/$\overline{LBE}$ (3-state) controls.

Interfacing With a 16-Bit Microprocessor

Interface between the Synchro-to-Digital converter (Model 1606 and a 16-bit microprocessor is illustrated in Figure 14. To simplify the system interface to peripherals and memory devices with varying access times, the microprocessor communicates with a system via an asynchronous bus. The address decoder generates the $\overline{INH}$ chip select for the converter. When the converter returns the CB signal, the microprocessor reads the data and terminates the bus cycle. Data strobes $\overline{UDS}$ and $\overline{LDS}$ enable the converter for 16-bit word transfers. If the interface software attempts an 8-bit read (i.e., the microprocessor generates only one data strobe), then a bus error ($\overline{BERR}$) is generated. $\overline{BERR}$ terminates the bus cycle and automatically generates an exception call to the operating system. Data could be transferred from the converter using the instruction MOVE.W 1606, EA, which moves a 16-bit data word from the peripheral to an effective address - either in a register on the microprocessor chip or in a system memory location.

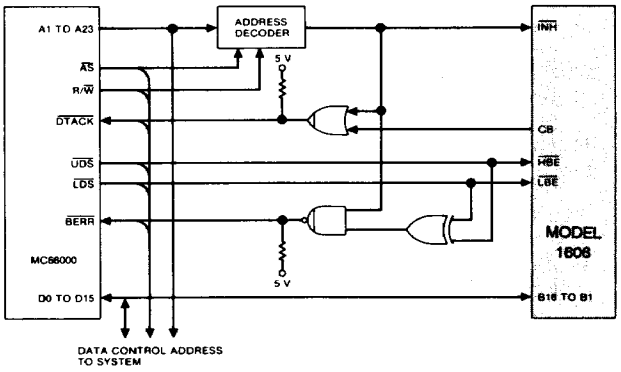


FIGURE 14 Interfacing 1606 Converter with 16-bit Microprocessor (MC68000) Via Asynchronous Bus

Velocity Outputs

As a by-product of the conversion process, the Model 1606 produces analog velocity signals. These analog signals have proven useful in various applications and are therefore brought out. The absolute value of these analog outputs is not critical to the overall conversion process. Therefore, unless otherwise specified, they are not closely controlled or characterized functions These outputs are:

- V (pin 8), Internal analog ground (Bias)
- VEL_A (pin 7), velocity output channel A
- VEL_B (pin 12) velocity output channel B

VEL_A/VEL_B is a dc voltage proportional to the velocity of the digital output angle (thereby the input shaft angle). The voltage goes negative for increasing digital angle and goes positive for decreasing digital angle. At maximum tracking velocity, the output voltage is 1.1 volts-dc (1.5 volts-dc for 800 Hz model). Detailed specification for velocity functions are provided on page 7. Dynamic characteristics including open loop and closed loop transfer functions are provided on the following pages.

"V," internal analog ground, also referred to as the "bias voltage" provides a reference point for all analog functions. The typical value of the bias voltage, V, is:

$V = 1/2\ (V_L - 0.7\ \text{V-dc})$

$= 2.15\ \text{V-dc} \pm 10\%\ (\text{for } V_L = +5\ \text{V-dc})$

All analog outputs have a minimum output drive of ± 1 mA with respect to V (bias). For a power supply of +5 V-dc, the minimum output swing is ± 1.1 V peak (± 1.5 V peak for 800 Hz model) with respect to V (bias).

If a bipolar signal, with respect to power supply ground, is required for any analog output, a difference circuit, as shown in Figure 15, may be used. The output can be scaled to a desired value by selecting the gain of the circuit. Also if reverse polarity output is desirable, the bias and signal connections to the difference amplifier should be reversed.

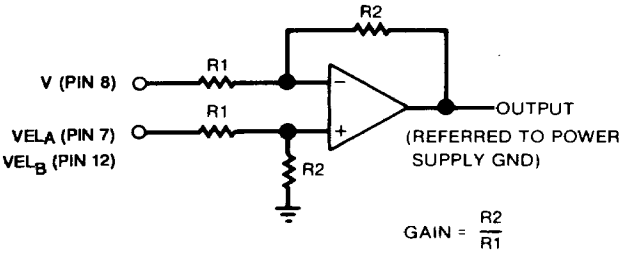


FIGURE 15 Difference Circuit for Bipolar Analog Outputs

Dynamic Performance

HSD/HRD1606 incorporates a high gain, Type II, servo loop to provide accurate real-time Synchro (Resolver)-to-Digital conversion. The converter is characterized for the following dynamic input angle conditions:

(1) Static Input Angle

(2) Constant Rate of Change of Input Angle Position (Constant Velocity)

(3) Constant Rate of Change of Input Angular Velocity (Constant Acceleration)

(4) Variable Rate of Change of Angular Velocity (Sinusoidal Modulation)

(5) Infinite Rate of Change of Angular Velocity (Step Input)

The 1606 accuracy specification applies for **Static (1)** and **Constant Velocity (2)** input conditions, as long as the maximum converter tracking rate is not exceeded.

For **Constant Acceleration (3)** of input angle, the digital output will lag the input by the following amount:

$$\text{Acceleration Lag (error)} = \frac{\text{Input Angle Acceleration}}{K_A}$$

The values of maximum tracking rate and acceleration constant (K_A) for different frequency options are given in the specification table (page 8). Note that the specified K_A is typical and is not a tightly controlled parameter (converter K_A is analogous to the open-loop gain of an operational amplifier).

For **Sinusoidal Shaft Angle Modulation (4)**, the digital angle output will lag the input by the following amount:

$$\text{Sinusoidal lag (error p-p)} = \frac{2 \times \pi^2 \times \text{Amp (p-p)} \times Fo^2}{K_A}$$

Where: Amp (p-p) = peak-peak angle modulation level
Fo = modulation frequency (Hz)
K_A = converter acceleration constant

The Peak Rate (Velocity) for a given sinusoidal modulation is:

Rate (degrees/sec) = π x Amp (degrees p-p) x Fo (Hz)

For **Step Inputs (5)**, the digital angle output will respond as a function of the converter's Large Signal and Small Signal transient response.

The **Large Signal** transient response is dependent solely on the maximum velocity (ω_{max}) and the maximum acceleration (α_{max}) of which the converter is capable. The large signal parameters are defined in Figure 16. The synchronizing time (t_{SYNC}) for large signals can be partitioned into three distinct intervals. Acceleration time (t_{ACC}) Slew time (t_{SLEW}) and Overshoot time (t_{OS}).

Acceleration time is the time interval from application of the step-input to the point at which the converter reaches its maximum velocity.

Slew time is the time interval from the point at which maximum velocity is obtained to the point at which the output angle is first equal to the input angle.

Overshoot time is the time interval from the point at which the converter output angle first equals the input angle (and applies constant acceleration in the opposite direction) to the point at which the output angle again reaches the input angle.

At the end of overshoot time, the small signal response becomes dominant and the converter will settle to the final value according to its small signal transient response function.

The **Small Signal** settling time (t_S) is specified for step inputs of less than 1.4 degrees. For small signal steps, the settling time is a function of the transient response of the converter.

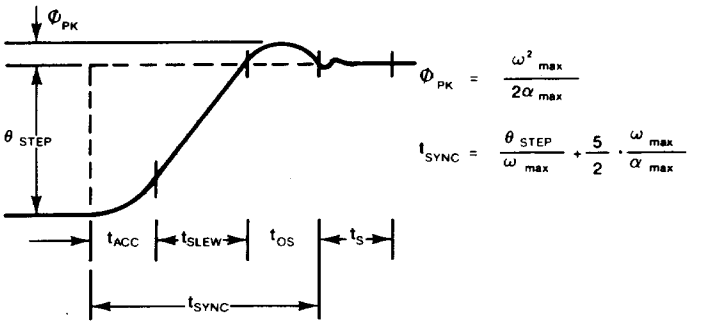


FIGURE 16 Large Signal ($\geq 1.4^\circ$) Response Parameters

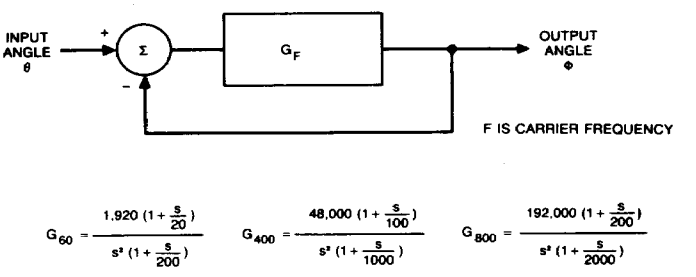


FIGURE 17 Transfer Functions for 1606

Transfer Function

The basic control loop model and transfer functions for 60-Hz, 400-Hz and 800-Hz models are shown in Figure 17. A more detailed model with corresponding transfer functions for both position and velocity output is shown in Figure 19. Typical values for transfer function parameters for different frequency options are shown in the table of Figure 18.

Transfer function parameters are determined by the specified frequency option of the converter. When a converter is operated at a frequency higher than that specified, these parameters remain the same. For some applications it may be advantageous to use a lower bandwidth converter operating at a higher carrier frequency.

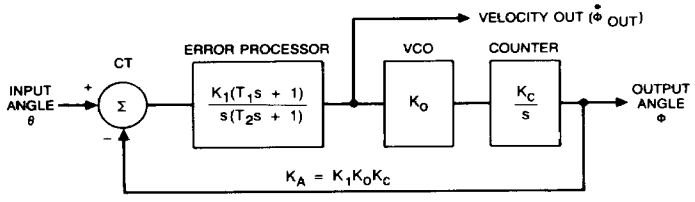
For example, to improve the position noise rejection, velocity output noise/ripple and velocity linearity, a 60-Hz frequency (option 6) could be used and operated at higher carrier frequencies such as 400-Hz.

For a better understanding of the dynamics of the 1606, bode plots for converter gain and output phase for 60-Hz, 400-Hz and 800-Hz options are shown in Figures 20 and 21.

Results of actual performance of step responses for both large and small signal inputs performed on typical converters are shown in Figure 22.

PARAMETER	UNITS	FREQUENCY OPTION		
		60 Hz	400 Hz	800 Hz
K_A	sec^{-2}	1,920	48,000	192,000
K_O	$\frac{Counts}{Volt \cdot Sec}$	29,800	149,000	218,000
K_C	$\frac{Radians}{Count}$	9.587×10^{-5}	9.587×10^{-5}	9.587×10^{-5}
K_1	$\frac{Volts}{Radian}$	672	3360	9187
T_1	ms	50.0	10.0	5.0
T_2	ms	5.0	1.0	0.5
$K_O K_C$	$\frac{Radians}{Volt \cdot Sec}$	2.857	14.28	20.90

FIGURE 18 Transfer Function Parameters (Typical Values)



POSITION GAIN (OPEN LOOP) $\frac{\Phi_{OUT}}{\theta_{IN}} = \frac{K_A(T_1s + 1)}{s^2(T_2s + 1)}$

VELOCITY GAIN (OPEN LOOP) $\frac{\Phi_{OUT}}{\theta_{IN}} = \frac{K_1(T_1s + 1)}{s(T_2s + 1)}$

POSITION GAIN (CLOSED LOOP) $\frac{\Phi_{OUT}}{\theta_{IN}} = \frac{T_1s + 1}{\frac{T_2s^3}{K_A} + \frac{s^2}{K_A} + T_1s + 1}$

VELOCITY GAIN (CLOSED LOOP) $\frac{\Phi_{OUT}}{\theta_{IN}} = \frac{T_1s^2 + s}{\frac{T_2s^3}{K_1} + \frac{s^2}{K_1} + T_1K_OK_Cs + K_OK_C}$

FIGURE 19 Detailed Transfer Function Model

Bode Plots

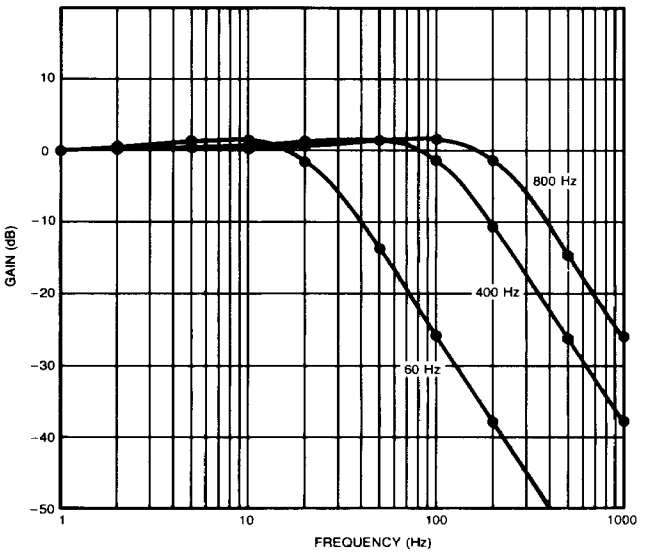


FIGURE 20 Gain Plot

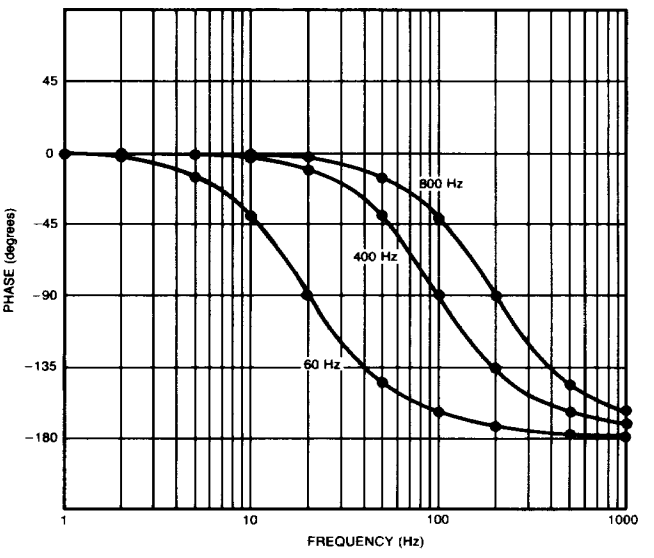
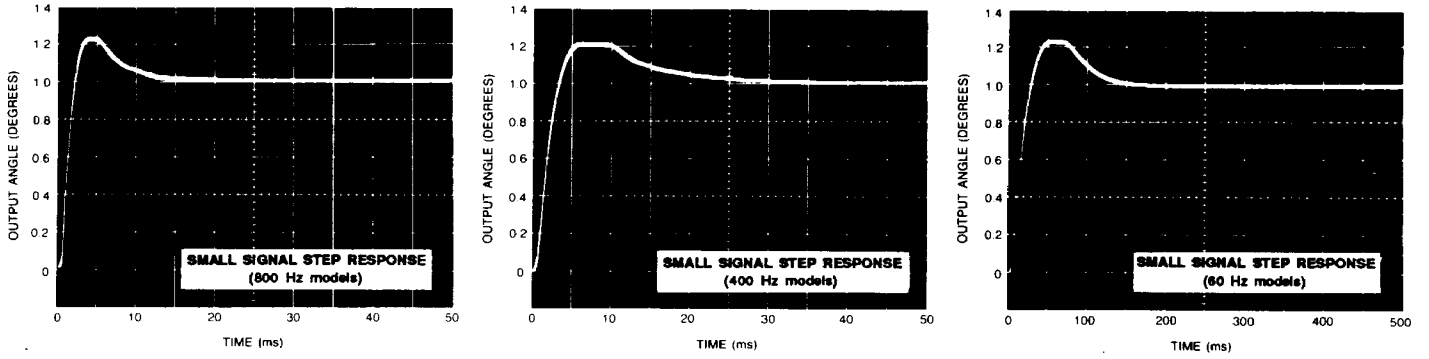


FIGURE 21 Phase Plot

Step Response

V_L = +5 V-dc, T_a = 25°C

Small Signal Input Step = 1.0 Degree



Large Signal Input Step = 179 Degrees

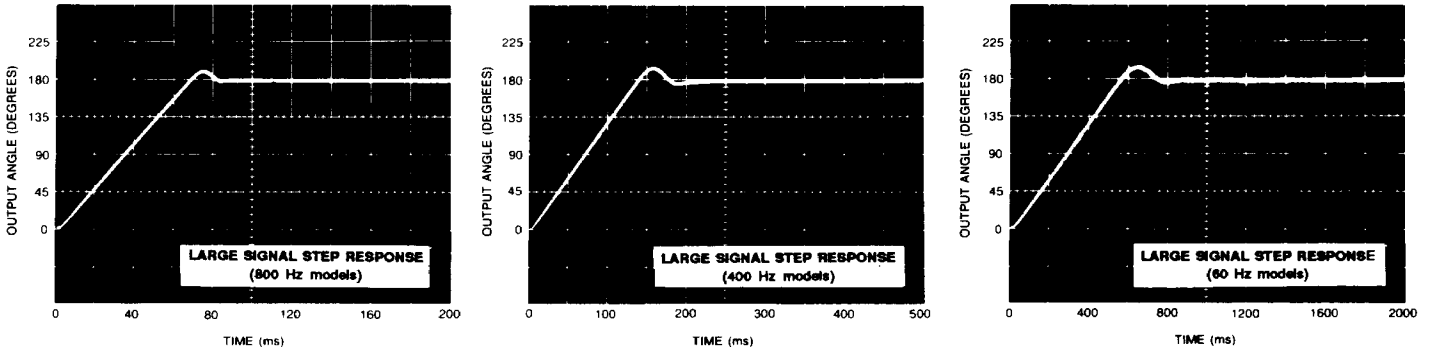
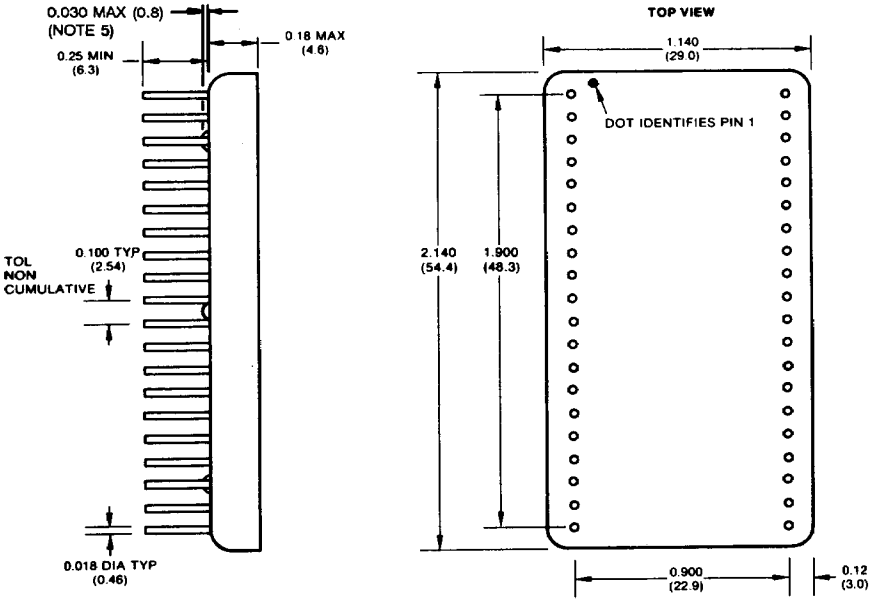


FIGURE 22 Small Signal and Large Signal Step Response



MECHANICAL OUTLINE (40 PIN TRIPLE DIP)

TOLERANCES:
.XX = ± .01 (±.25)
.XXX = ±.005 (±.13)

NOTES:
1. CASE IS ELECTRICALLY FLOATING.
2. PINS ARE KOVAR WITH GOLD PLATING: (50 μINCH MIN.)
3. PACKAGE IS KOVAR WITH ELECTROLESS NICKEL PLATING.
4. DIMENSIONS SHOWN IN INCHES AND (MM).
5. STANDOFFS (3) CERAMIC OR GLASS.

Ordering Information

HSD1606 – T F I A

Temperature Range

1 = 0°C to + 70°C
2 = –25°C to + 85°C
3 = –55°C to +125°C

Frequency

4 = 400 Hz
6 = 60 Hz
8 = 800 Hz

Accuracy

S = ±5.2 arc-minutes
H = ±2.6 arc-minutes
V = ±1.3 arc-minutes

Input Signal

1 = 11.8 V-rms
2 = 26 V-rms
9 = 90 V-rms
0 = Ext. Signal XFMRS
5 = Ext. Signal and Reference XFMRS

SPECIFY **HRD1606** FOR DUAL RESOLVER INPUT

As a standard practice, all converters are built in accordance with requirements of MIL-STD-883, rev. B including 168 hours of active burn-in.

Other products available from NATEL

- **3 arc-second accurate,** Programmable Dynamic Angle Simulator that includes 4 Related Instruments and is totally A.T.E. Programmable (L200).
- Hybrid (36-pin DDIP size) Synchro(Resolver)-to-Digital converters that operate from a **single +5V power supply** and offer excellent features such as BIT, AGC, low power dissipation and more (Models 1006, 1056, 1046 and 1044).
- 1.3 arc-minute accuracy, high power, Digital-to-Synchro converters that **do not require any DC power supplies** (Models 5031 and 5131).
- Second generation Four Quadrant Multiplying Sin/Cos DAC (HDSC2026).
- **2-channel** Digital-to-Sin/Cos Converter in a single 36-pin hybrid (HDSC2036)
- 2 VA output, Digital to Resolver Converter in a 32-pin package (HDR2116).
- Resolver Control Differential Transmitter in a single 36-pin package (HCDX3106).

A wide range of applications assistance is available from Natel. Application notes can be requested when available . . . and Natel's applications engineers are at your disposal for solving specific problems.

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